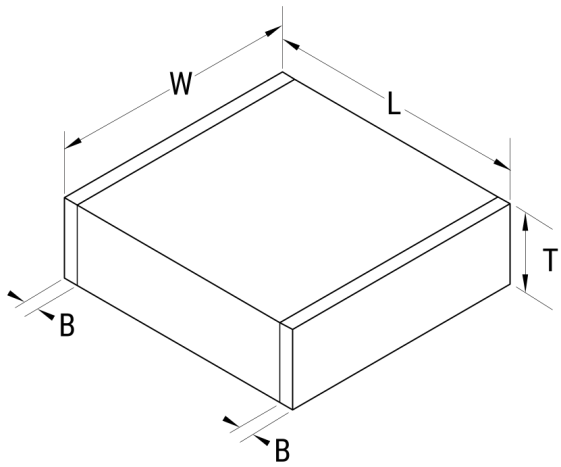
LDBCB2180JC5N0

Aliases (DBCB2180JC5N0)

LDB, Film, Metallized PPS Stacked, General Purpose, 0.018 uF, 5%, 50 VDC, 125°C, 1210, 1.5mm



Click here for the 3D model.

Dimensions	
Chip Size	1210
L	3.3mm +0.3/-0.1mm
W	2.5mm +/-0.3mm
T	1.5mm MAX
B	0.4mm +0.5/-0.3mm

Packaging Specifications	
Packaging	T&R
Packaging Quantity	2250

General Information	
Series	LDB
Dielectric	Metallized PPS Stacked
Style	SMD Chip
RoHS	Yes
AEC-Q200	No
Component Weight	0.089 g
Shelf Life	104 Weeks
MSL	3

Specifications	
Capacitance	0.018 uF
Capacitance Tolerance	5%
Voltage DC	50 VDC
Temperature Range	-55/+125°C
Rated Temperature	125°C
Dissipation Factor	0.6% 1kHz
Insulation Resistance	3 GOhms

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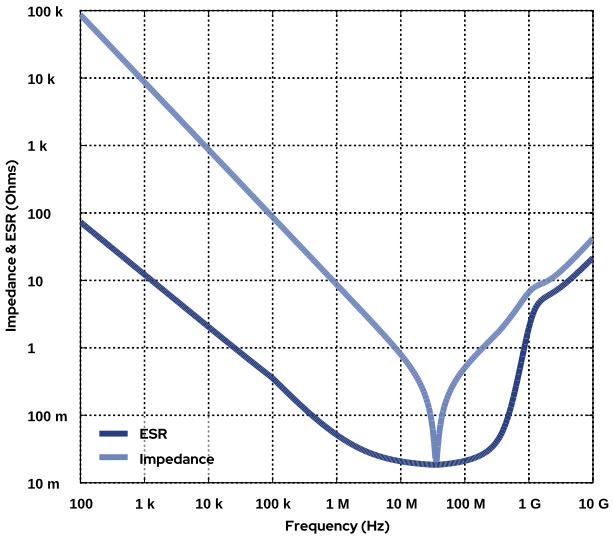
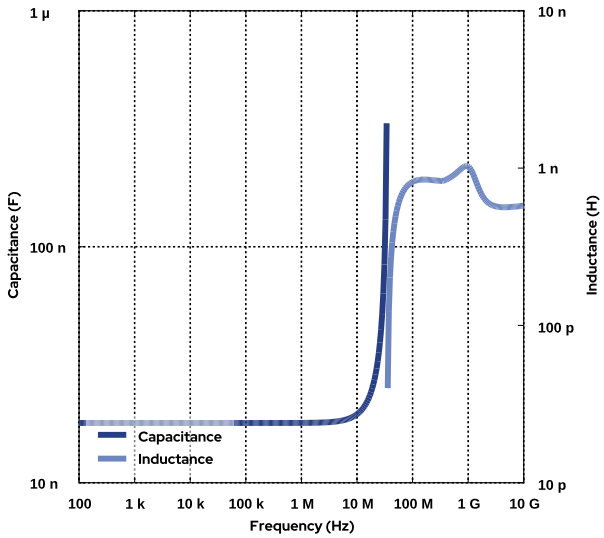
Simulations

For the complete simulation environment please visit K-SIM.

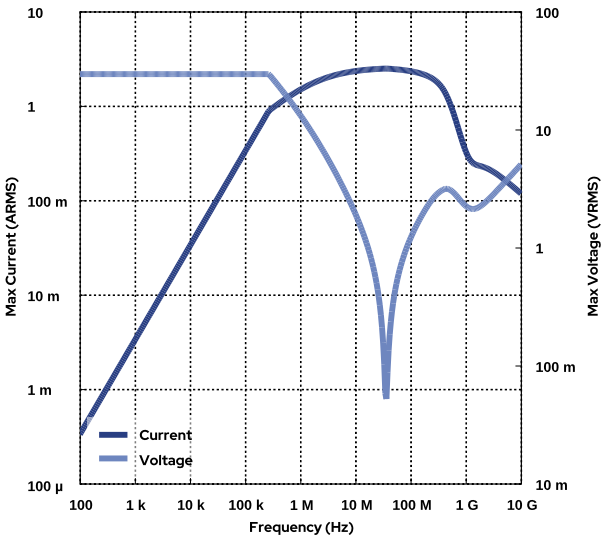
Impedance and ESR



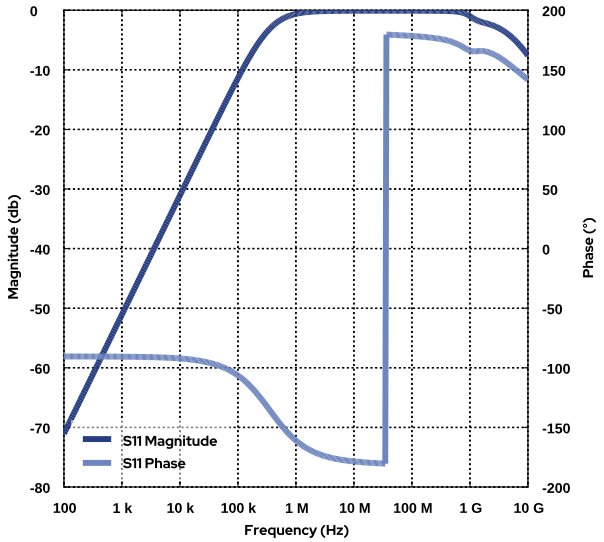
Capacitance and Inductance



Current and Voltage



S11



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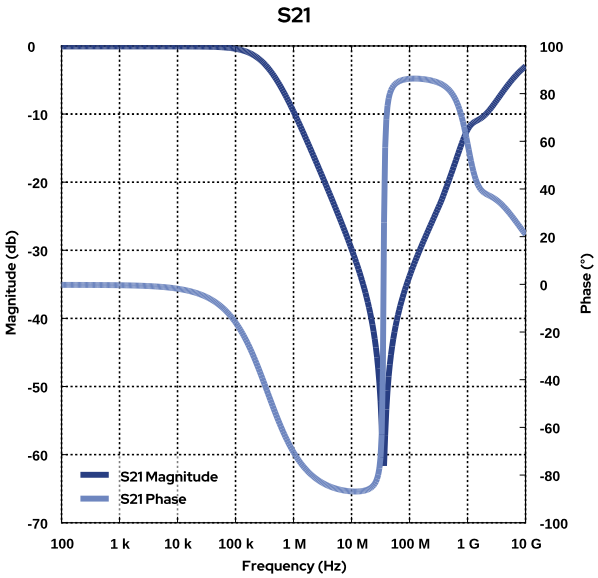

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These are simulations.

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.