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A

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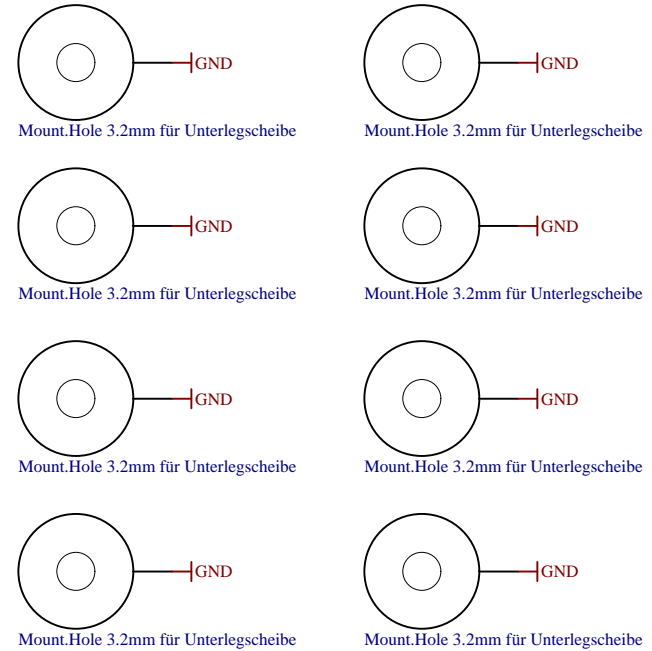
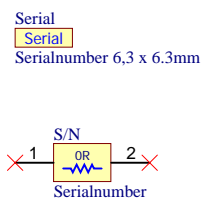
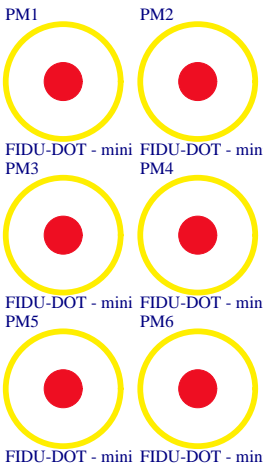
D

D

U\_J1  
J1.SchDoc  
U\_J2  
J2.SchDoc  
U\_J3  
J3.SchDoc  
U\_J4  
J4.SchDoc  
U\_DDR4-TERM  
DDR4-TERM.SchDoc  
U\_B64  
B64.SchDoc  
U\_B65  
B65.SchDoc  
U\_B66  
B66.SchDoc  
U\_B\_GT  
B\_GT.SchDoc

U\_B\_PS\_GT  
B\_PS\_GT.SchDoc  
U\_PS\_DDR  
PS\_DDR.SchDoc  
U\_B\_MIO  
B\_MIO.SchDoc  
U\_B\_HD  
B\_HD.SchDoc  
U\_Clock  
Clock.SchDoc  
U\_CONFIG  
CONFIG.SchDoc  
U\_DDR4-RAM  
DDR4-RAM.SchDoc  
U\_DDR4-RAM\_2  
DDR4-RAM\_2.SchDoc  
U\_DDR4-RAM\_3  
DDR4-RAM\_3.SchDoc  
U\_DDR4-RAM\_4  
DDR4-RAM\_4.SchDoc

U\_DDR4-TERM  
DDR4-TERM.SchDoc  
U\_ZU\_POWER  
ZU\_POWER.SchDoc  
U\_ZU\_PS\_POWER  
ZU\_PS\_POWER.SchDoc  
U\_POWER  
POWER.SchDoc  
U\_POWER\_2  
POWER\_2.SchDoc  
U\_POWER\_4  
POWER\_4.SchDoc  
U\_REV\_CH  
Revision\_Changes.SchDoc



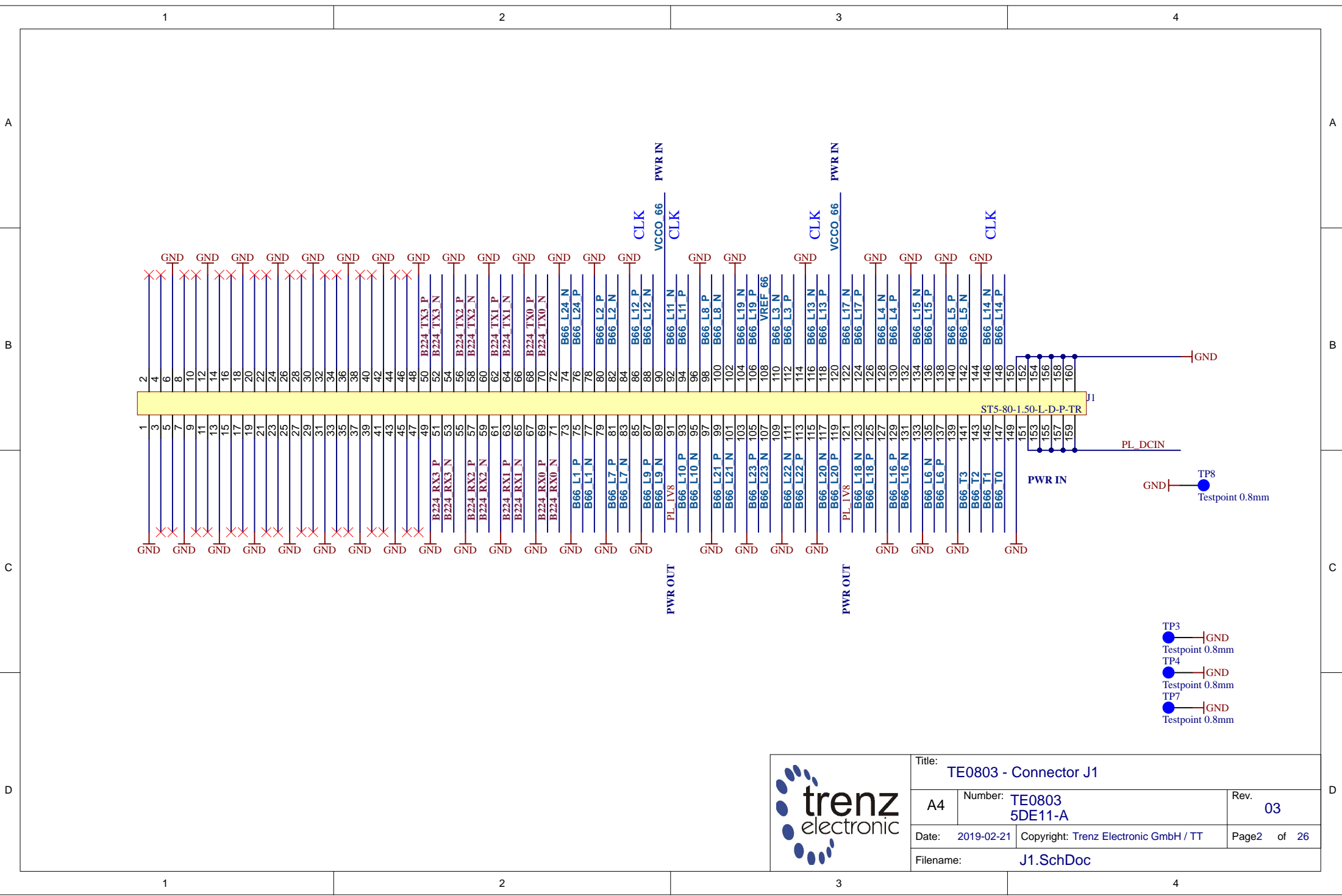
Title: TE0803		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

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Title: TE0803 - Connector J1		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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A

A

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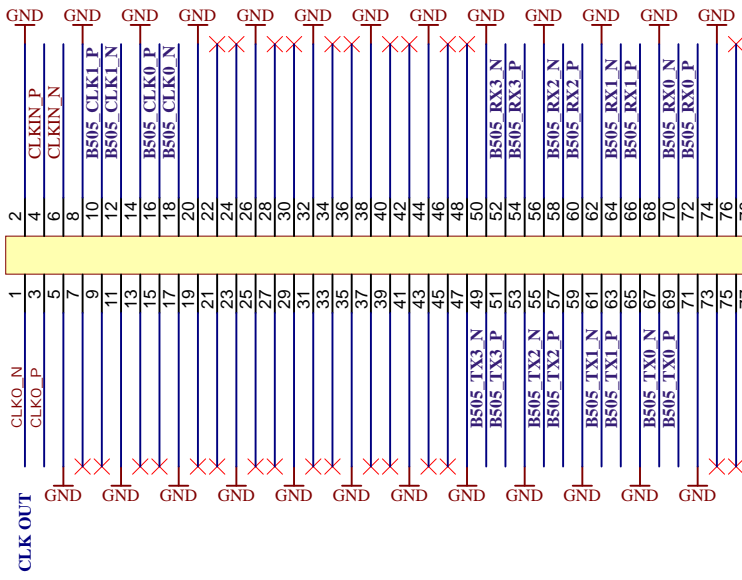
C

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CLKIN  
CLKIN  
CLKIN



(External pull-up R required)

(External pull-up R required)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

(On board pull-up R)

(1.2..1.5V)

PWR IN

PWR IN

LP\_DCDC

DCDCIN

PS\_IV8

GND

TP14

TP15

Testpoint 0.8mm

Testpoint 0.8mm

GND

TP5

Testpoint 0.8mm



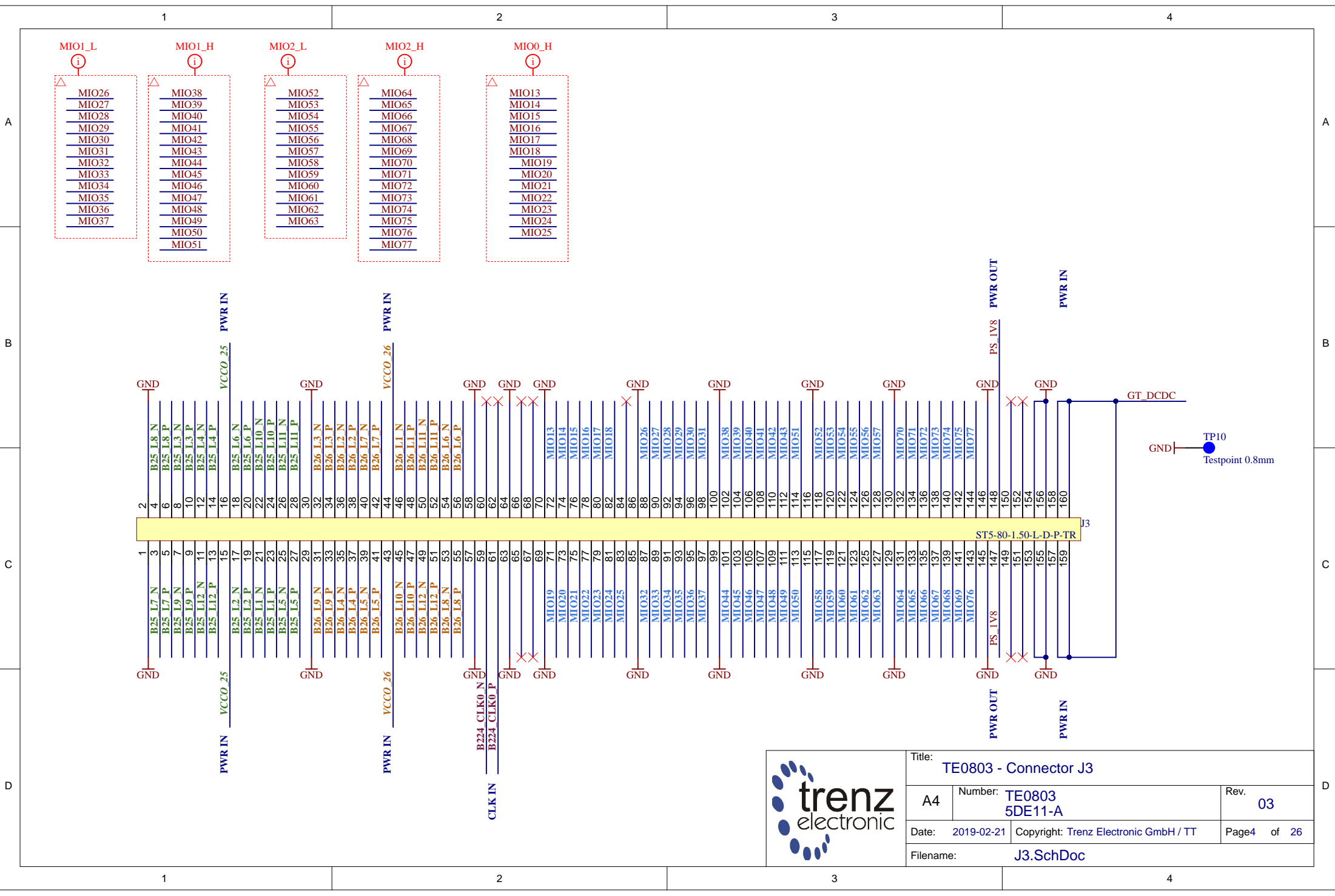

Title: TE0803 - Connector J2		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page3 of 26
Filename: J2.SchDoc		

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Title: TE0803 - Connector J3		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		



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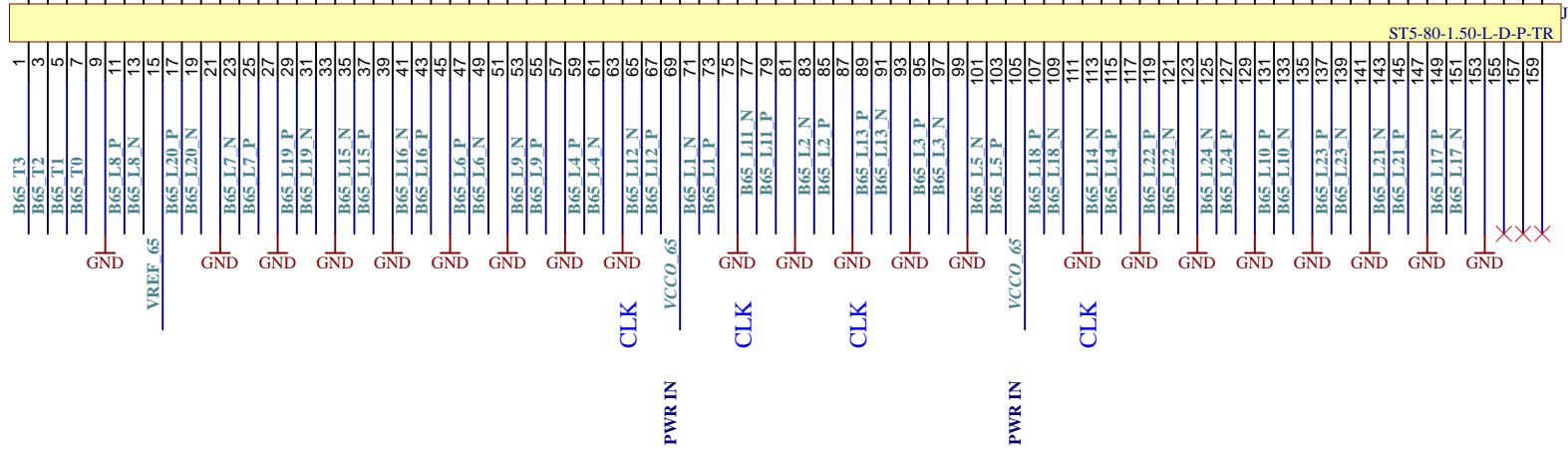
B

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D

D



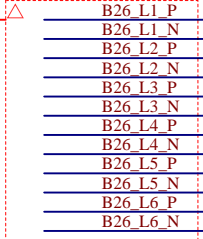
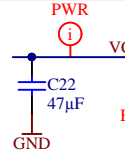
Title: TE0803 - Connector J4		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		

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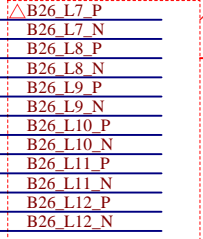
4



**U1C XCZU5EV-1SFVC784E**

**BANK 46 HD (ZU2/3 BANK 26 HD)**

F14	VCCO_46		
C15	VCCO_46		
B15	IO_L1P_AD11P_46	IO_L7P_HDGC_AD5P_46	G13
A15	IO_L1N_AD11N_46	IO_L7N_HDGC_AD5N_46	F13
B14	IO_L2P_AD10P_46	IO_L8P_HDGC_AD4P_46	F15
A14	IO_L2N_AD10N_46	IO_L8N_HDGC_AD4N_46	E15
B13	IO_L3P_AD9P_46	IO_L9P_AD3P_46	G15
A13	IO_L3N_AD9N_46	IO_L9N_AD3N_46	G14
C14	IO_L4P_AD8P_46	IO_L10P_AD2P_46	H14
C13	IO_L4N_AD8N_46	IO_L10N_AD2N_46	H13
D15	IO_L5P_HDGC_AD7P_46	IO_L11P_AD1P_46	K14
D14	IO_L5N_HDGC_AD7N_46	IO_L11N_AD1N_46	J14
E14	IO_L6P_HDGC_AD6P_46	IO_L12P_AD0P_46	L14
E13	IO_L6N_HDGC_AD6N_46	IO_L12N_AD0N_46	L13



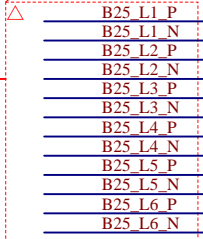
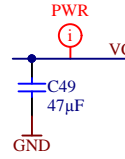
**BANK 43 HD (ZU2/3 BANK 44 HD)**

<del>AC10</del>	<del>VCCO_43</del>		
<del>AG12</del>	<del>VCCO_43</del>		
<del>AG10</del>	<del>IO_L1P_AD11P_43</del>	<del>IO_L7P_HDGC_AD5P_43</del>	<del>AD11</del>
<del>AH10</del>	<del>IO_L1N_AD11N_43</del>	<del>IO_L7N_HDGC_AD5N_43</del>	<del>AD10</del>
<del>AF11</del>	<del>IO_L2P_AD10P_43</del>	<del>IO_L8P_HDGC_AD4P_43</del>	<del>AB11</del>
<del>AG11</del>	<del>IO_L2N_AD10N_43</del>	<del>IO_L8N_HDGC_AD4N_43</del>	<del>AC11</del>
<del>AH12</del>	<del>IO_L3P_AD9P_43</del>	<del>IO_L9P_AD3P_43</del>	<del>AA11</del>
<del>AH11</del>	<del>IO_L3N_AD9N_43</del>	<del>IO_L9N_AD3N_43</del>	<del>AA10</del>
<del>AE10</del>	<del>IO_L4P_AD8P_43</del>	<del>IO_L10P_AD2P_43</del>	<del>W10</del>
<del>AF10</del>	<del>IO_L4N_AD8N_43</del>	<del>IO_L10N_AD2N_43</del>	<del>Y10</del>
<del>AE12</del>	<del>IO_L5P_HDGC_AD7P_43</del>	<del>IO_L11P_AD1P_43</del>	<del>Y9</del>
<del>AF12</del>	<del>IO_L5N_HDGC_AD7N_43</del>	<del>IO_L11N_AD1N_43</del>	<del>AA8</del>
<del>AC13</del>	<del>IO_L6P_HDGC_AD6P_43</del>	<del>IO_L12P_AD0P_43</del>	<del>AB10</del>
<del>AD12</del>	<del>IO_L6N_HDGC_AD6N_43</del>	<del>IO_L12N_AD0N_43</del>	<del>AB9</del>

**U1B**

**BANK 44 HD (ZU2/3 BANK 24 HD)**

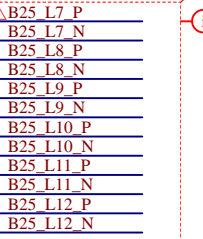
<del>AA14</del>	<del>VCCO_44</del>		
<del>AD13</del>	<del>VCCO_44</del>		
<del>AE15</del>	<del>IO_L1P_AD15P_44</del>	<del>IO_L7P_HDGC_44</del>	<del>AA13</del>
<del>AE14</del>	<del>IO_L1N_AD15N_44</del>	<del>IO_L7N_HDGC_44</del>	<del>AB13</del>
<del>AG14</del>	<del>IO_L2P_AD14P_44</del>	<del>IO_L8P_HDGC_44</del>	<del>AB15</del>
<del>AH11</del>	<del>IO_L2N_AD14N_44</del>	<del>IO_L8N_HDGC_44</del>	<del>AB14</del>
<del>AG13</del>	<del>IO_L3P_AD13P_44</del>	<del>IO_L9P_AD11P_44</del>	<del>W14</del>
<del>AH13</del>	<del>IO_L3N_AD13N_44</del>	<del>IO_L9N_AD11N_44</del>	<del>W13</del>
<del>AE13</del>	<del>IO_L4P_AD12P_44</del>	<del>IO_L10P_AD10P_44</del>	<del>Y14</del>
<del>AF13</del>	<del>IO_L4N_AD12N_44</del>	<del>IO_L10N_AD10N_44</del>	<del>Y13</del>
<del>AD15</del>	<del>IO_L5P_HDGC_44</del>	<del>IO_L11P_AD9P_44</del>	<del>W12</del>
<del>AD14</del>	<del>IO_L5N_HDGC_44</del>	<del>IO_L11N_AD9N_44</del>	<del>W11</del>
<del>AC14</del>	<del>IO_L6P_HDGC_44</del>	<del>IO_L12P_AD8P_44</del>	<del>Y12</del>
<del>AC13</del>	<del>IO_L6N_HDGC_44</del>	<del>IO_L12N_AD8N_44</del>	<del>AA12</del>



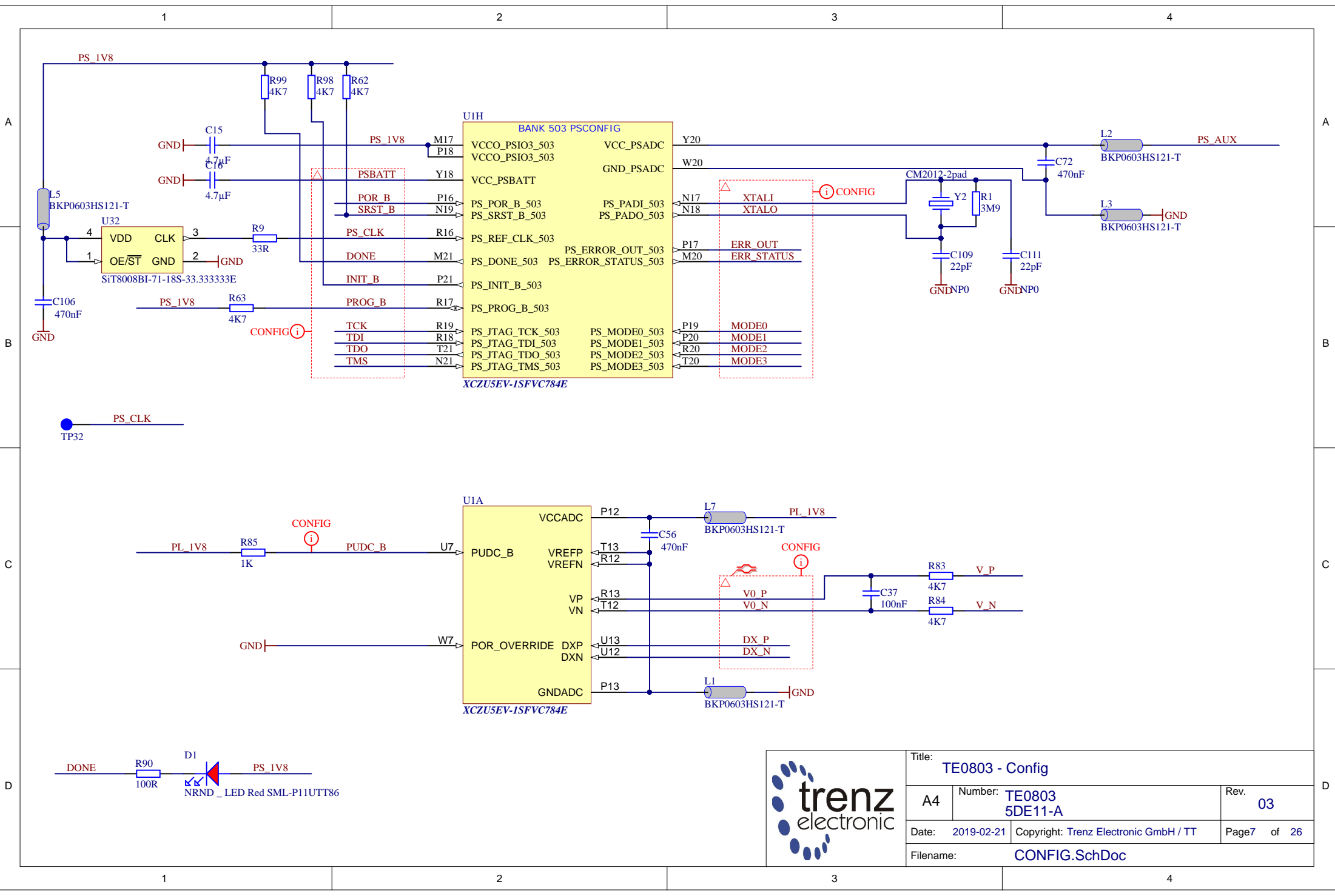
**XCZU5EV-1SFVC784E**

**BANK 45 HD (ZU2/3 BANK 25 HD)**

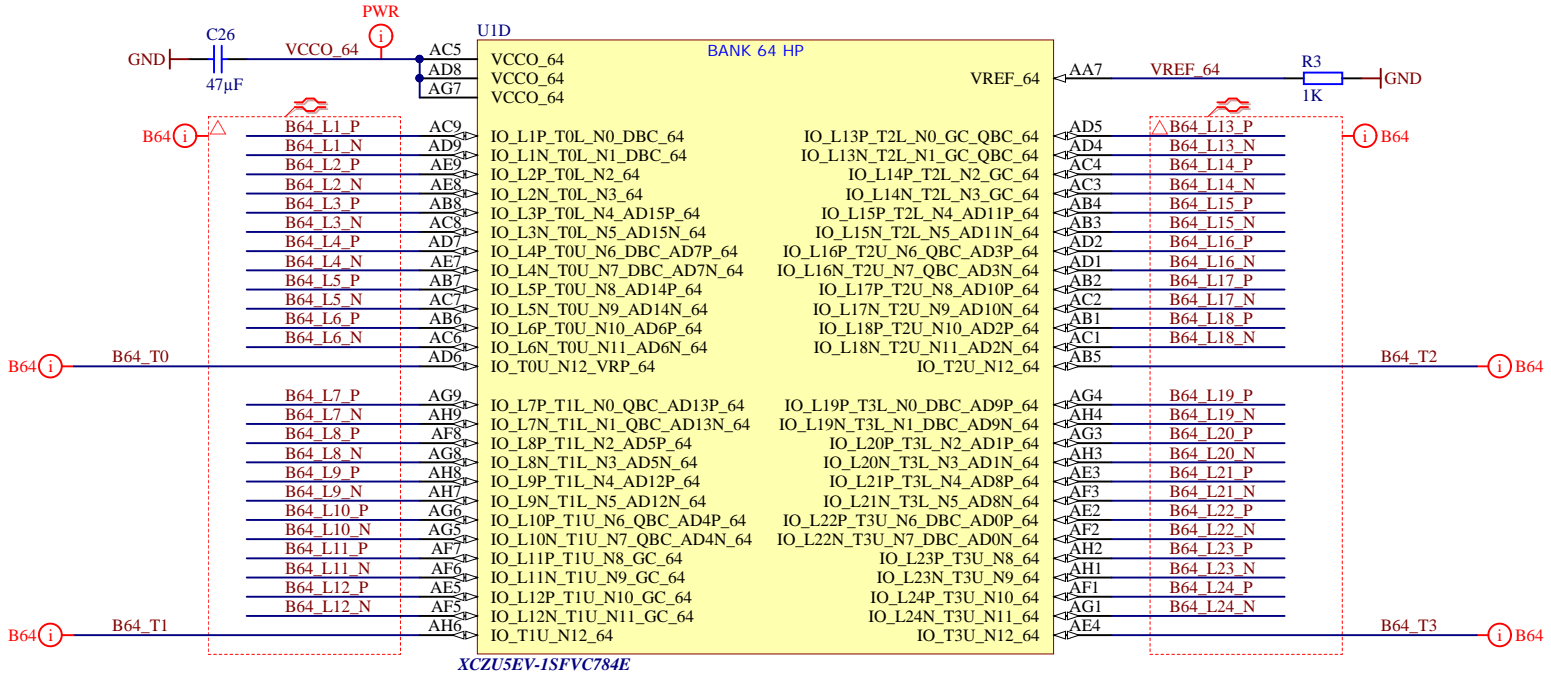
B12	VCCO_45		
E11	VCCO_45		
J11	IO_L1P_AD15P_45	IO_L7P_HDGC_45	E10
J10	IO_L1N_AD15N_45	IO_L7N_HDGC_45	D10
K13	IO_L2P_AD14P_45	IO_L8P_HDGC_45	E12
K12	IO_L2N_AD14N_45	IO_L8N_HDGC_45	D11
H11	IO_L3P_AD13P_45	IO_L9P_AD11P_45	C11
G10	IO_L3N_AD13N_45	IO_L9N_AD11N_45	B10
J12	IO_L4P_AD12P_45	IO_L10P_AD10P_45	B11
H12	IO_L4N_AD12N_45	IO_L10N_AD10N_45	A10
G11	IO_L5P_HDGC_45	IO_L11P_AD9P_45	A12
F11	IO_L5N_HDGC_45	IO_L11N_AD9N_45	A11
F12	IO_L6P_HDGC_45	IO_L12P_AD8P_45	D12
F11	IO_L6N_HDGC_45	IO_L12N_AD8N_45	C12



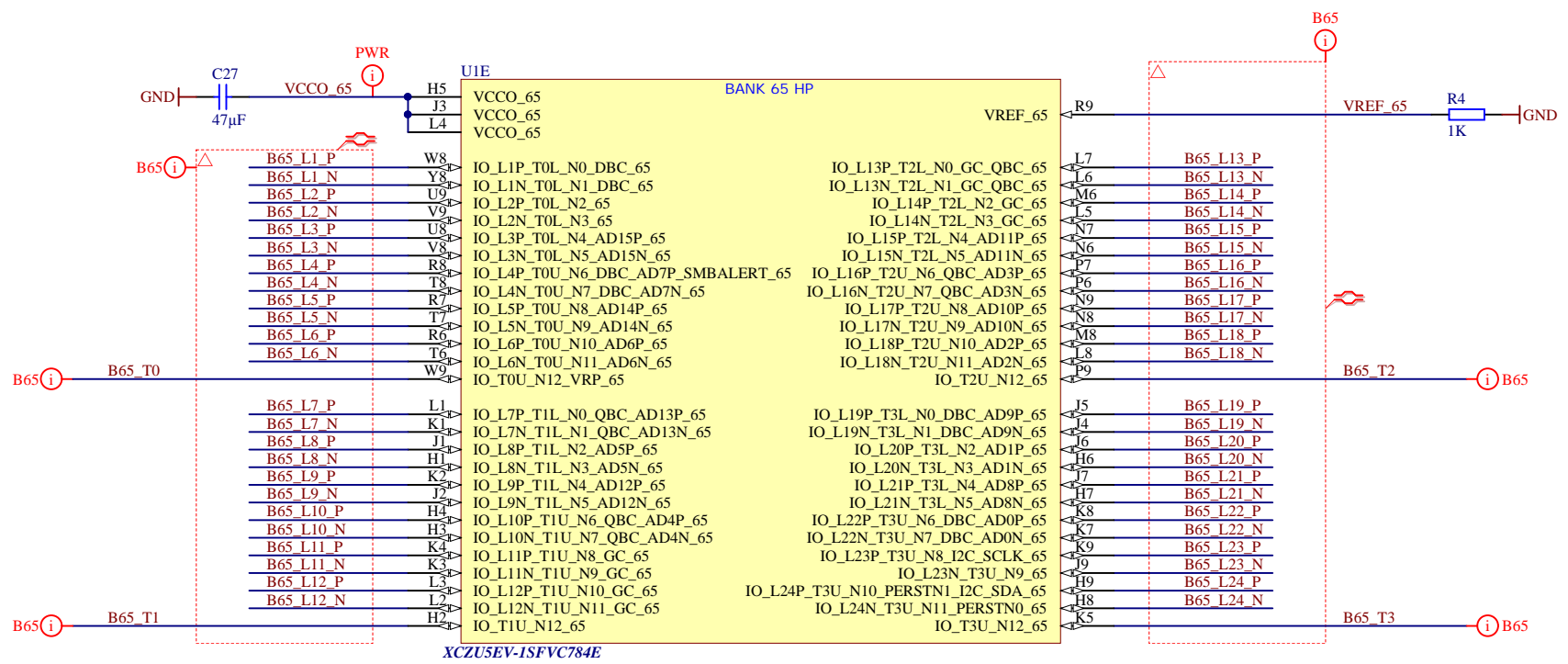
Title: <b>TE0803 - HD Banks</b>		
A4	Number: <b>TE0803 5DE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>6</b> of <b>26</b>
Filename: <b>B_HD.SchDoc</b>		



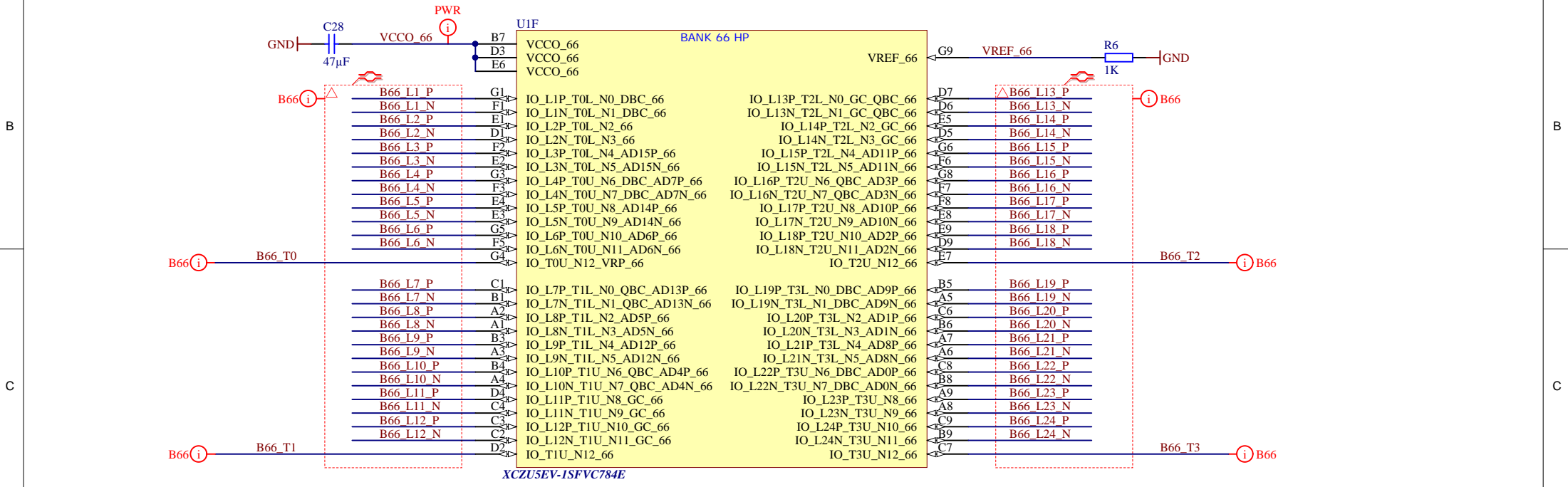
Title: TE0803 - Config		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



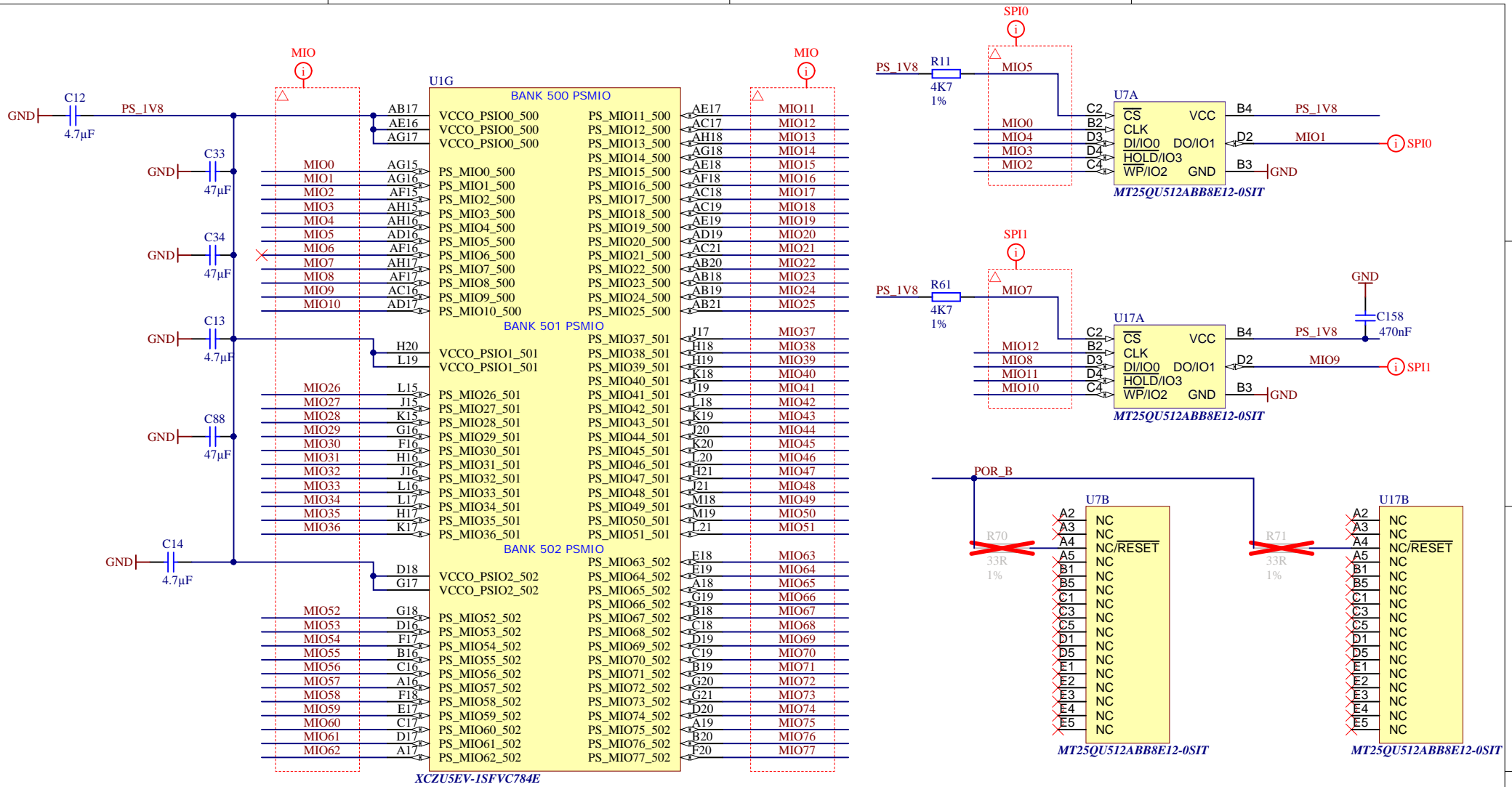
Title: <b>TE0803 - B64</b>		
A4	Number: <b>TE0803 5DE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>8</b> of <b>26</b>
Filename: <b>B64.SchDoc</b>		



Title: <b>TE0803 - B65</b>		
A4	Number: <b>TE0803 5DE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>9</b> of <b>26</b>
Filename: <b>B65.SchDoc</b>		

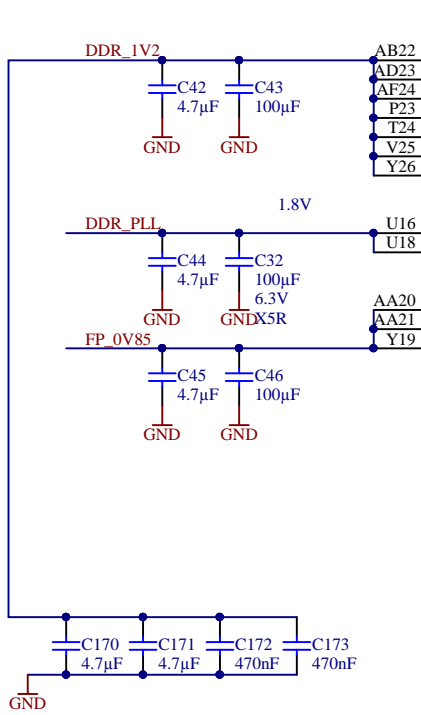


Title: <b>TE0803 - B66</b>		
A4	Number: <b>TE0803 5DE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>10</b> of <b>26</b>
Filename: <b>B66.SchDoc</b>		



			Title: TE0803 - MIO Banks	
			A4	Number: TE0803 5DE11-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page 11 of 26
Filename: B_MIO.SchDoc				





U11		BANK 504 PSDDR		XZU5EV-1SFVC784E	
VCCO_PSDDR_504	PS_DDR_CK0_504	W25	DDR4-CLK0_P	D80	
VCCO_PSDDR_504	PS_DDR_CK_N0_504	W26	DDR4-CLK0_N	D80	
VCCO_PSDDR_504	PS_DDR_CKE0_504	V28	DDR4-CKE0		
VCCO_PSDDR_504	PS_DDR_CK1_504	Y24			✗
VCCO_PSDDR_504	PS_DDR_CK_N1_504	Y25			✗
VCCO_PSDDR_504	PS_DDR_CKE1_504	V27			✗
VCC_PSDDR_PLL	PS_DDR_A0_504	W28	DDR4-A0		
VCC_PSDDR_PLL	PS_DDR_A1_504	Y28	DDR4-A1		
VCC_PSDDR_PLL	PS_DDR_A2_504	AB28	DDR4-A2		
	PS_DDR_A3_504	AA28	DDR4-A3		
	PS_DDR_A4_504	Y27	DDR4-A4		
VCC_PSINTFP_DDR	PS_DDR_A5_504	AA27	DDR4-A5		
VCC_PSINTFP_DDR	PS_DDR_A6_504	Y22	DDR4-A6		
VCC_PSINTFP_DDR	PS_DDR_A7_504	AA23	DDR4-A7		
	PS_DDR_A8_504	AA22	DDR4-A8		
	PS_DDR_A9_504	AB23	DDR4-A9		
	PS_DDR_A10_504	AA25	DDR4-A10		
	PS_DDR_A11_504	AA26	DDR4-A11		
	PS_DDR_A12_504	AB25	DDR4-A12		
	PS_DDR_A13_504	AB26	DDR4-A13		
	PS_DDR_A14_504	AB24	DDR4-A14		
	PS_DDR_A15_504	AC24	DDR4-A15		
	PS_DDR_A16_504	AC23	DDR4-A16		
	PS_DDR_A17_504	AC22	DDR4-A17		
	PS_DDR_CS_N0_504	W27	DDR4-CS		
	PS_DDR_CS_N1_504	V26			✗
	PS_DDR_BA0_504	V23	DDR4-BA0		
	PS_DDR_BA1_504	W22	DDR4-BA1		
	PS_DDR_BG0_504	W24	DDR4-BG0		
	PS_DDR_BG1_504	V22	DDR4-BG1		
	PS_DDR_PARITY_504	V24	DDR4-PAR		
	PS_DDR_RAM_RST_N_504	U23	DDR4-RESET		
	PS_DDR_ACT_N_504	Y23	DDR4-ACT		
	PS_DDR_ALERT_N_504	U25	DDR4-ALERT		
	PS_DDR_ZQ_504	U24		R2 240R	GND
	PS_DDR_ODT0_504	U28	DDR4-ODT0		
	PS_DDR_ODT1_504	U26			✗

XZU5EV-1SFVC784E

U1J		BANK 504 PSDDR		XZU5EV-1SFVC784E	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504	T22	DQ32
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504	R22	DQ33
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504	P22	DQ34
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504	N22	DQ35
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504	T23	DQ36
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504	P24	DQ37
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504	R24	DQ38
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504	N24	DQ39
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504	H24	DQ40
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504	J24	DQ41
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504	M24	DQ42
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504	K24	DQ43
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504	J22	DQ44
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504	H22	DQ45
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504	K22	DQ46
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504	J22	DQ47
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504	M25	DQ48
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504	M26	DQ49
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504	L25	DQ50
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504	L26	DQ51
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504	K28	DQ52
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504	L28	DQ53
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504	M28	DQ54
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504	N28	DQ55
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504	J28	DQ56
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504	K27	DQ57
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504	H28	DQ58
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504	H27	DQ59
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504	G26	DQ60
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504	G25	DQ61
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504	K25	DQ62
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504	J25	DQ63
		PS_DDR_DQ64_504	PS_DDR_DQ64_504	T28	
DDR4-DQS0_P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ65_504	R28	
DDR4-DQS0_N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ66_504	P28	
DDR4-DQS1_P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ67_504	P27	
DDR4-DQS1_N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ68_504	P26	
DDR4-DQS2_P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ69_504	R25	
DDR4-DQS2_N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ70_504	P25	
DDR4-DQS3_P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ71_504	T25	
DDR4-DQS3_N	AF27	PS_DDR_DQS_N3_504			
DDR4-DQS4_P	N23	PS_DDR_DQS_P4_504			
DDR4-DQS4_N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM0_504	AG20	DDR4-DM0
DDR4-DQS5_P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM1_504	AE23	DDR4-DM1
DDR4-DQS5_N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM2_504	AE25	DDR4-DM2
DDR4-DQS6_P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM3_504	AE28	DDR4-DM3
DDR4-DQS6_N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM4_504	R23	DDR4-DM4
DDR4-DQS7_P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM5_504	H23	DDR4-DM5
DDR4-DQS7_N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM6_504	L27	DDR4-DM6
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM7_504	H26	DDR4-DM7
	T27	PS_DDR_DQS_N8_504	PS_DDR_DM8_504	T26	

XZU5EV-1SFVC784E



Title: TE0803 - PS_DDR		
A4	Number: TE0803 5DE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		



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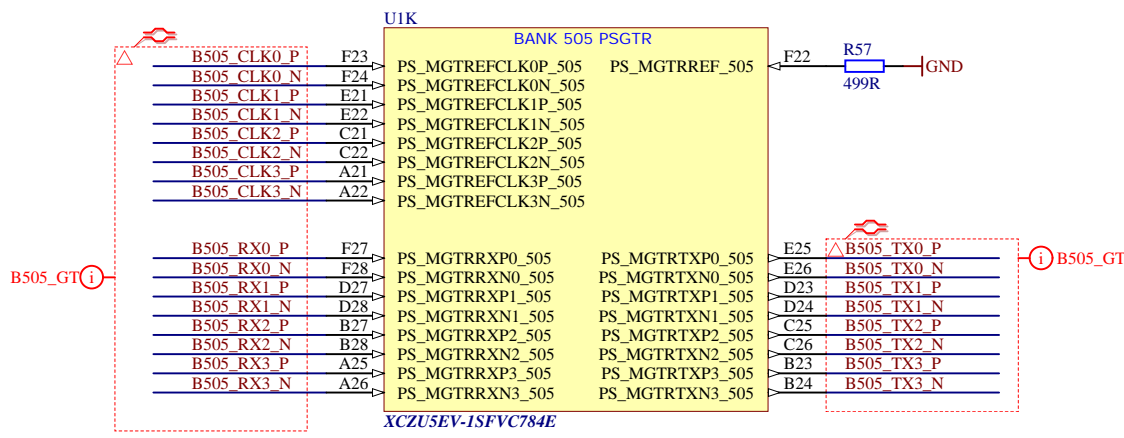
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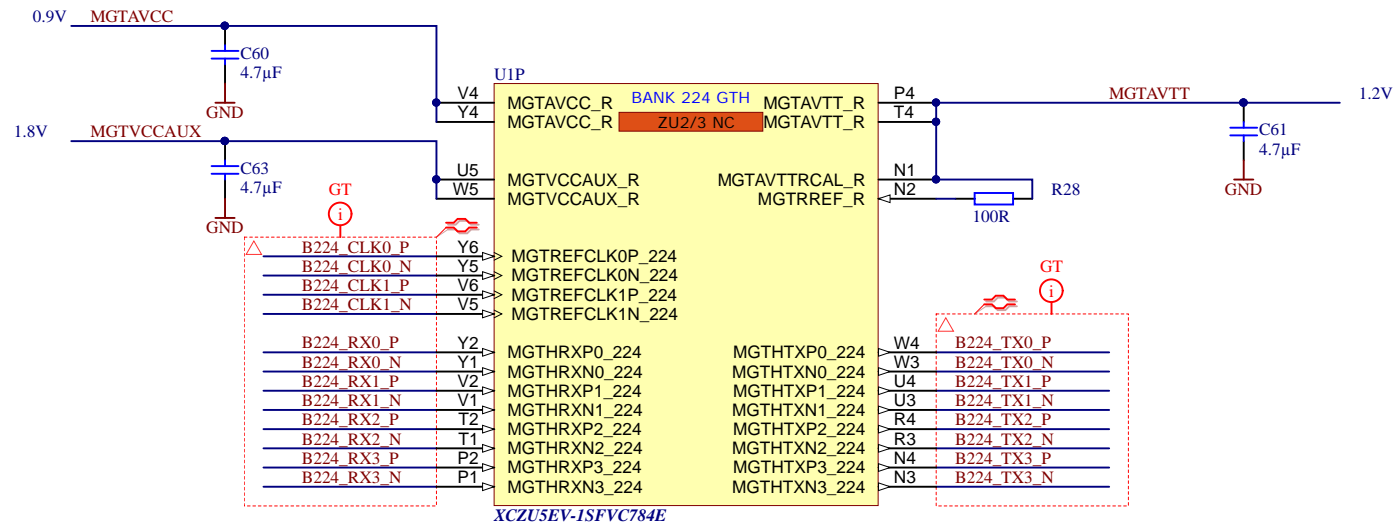
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A4	Number: <b>TE0803 5DE11-A</b>	Rev. <b>03</b>
Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>13</b> of <b>26</b>
Filename: <b>B_PS_GT.SchDoc</b>		


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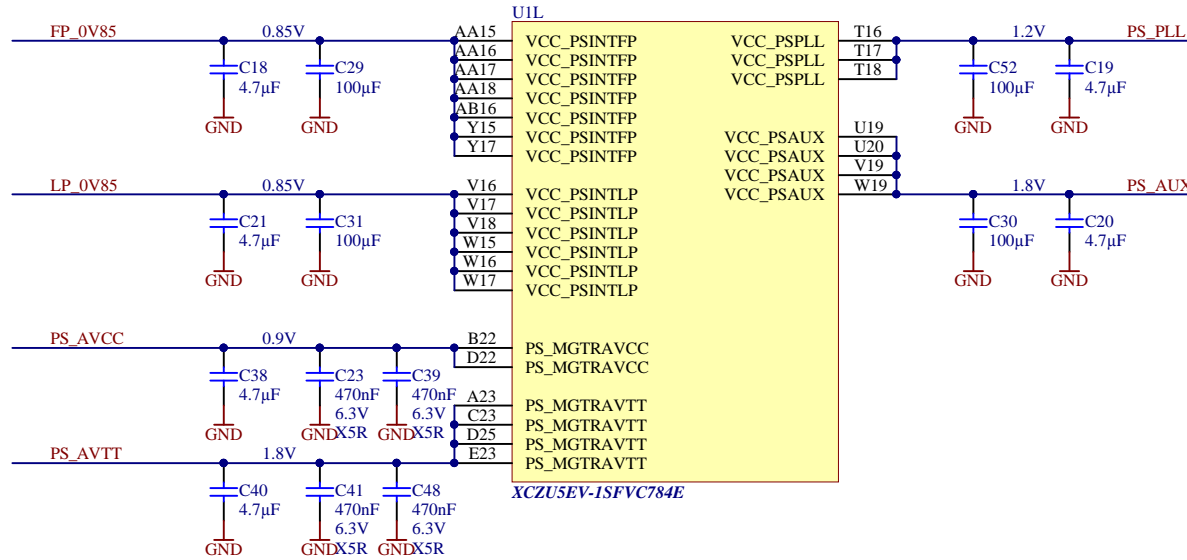
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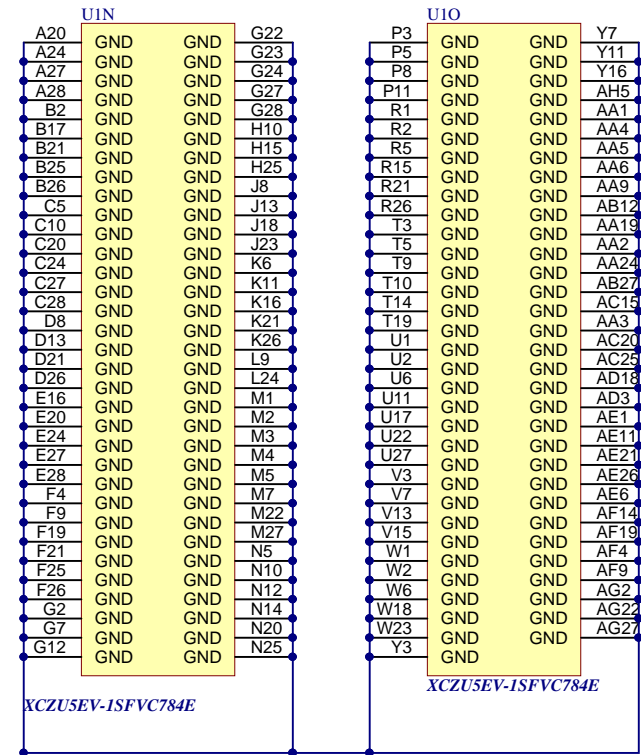
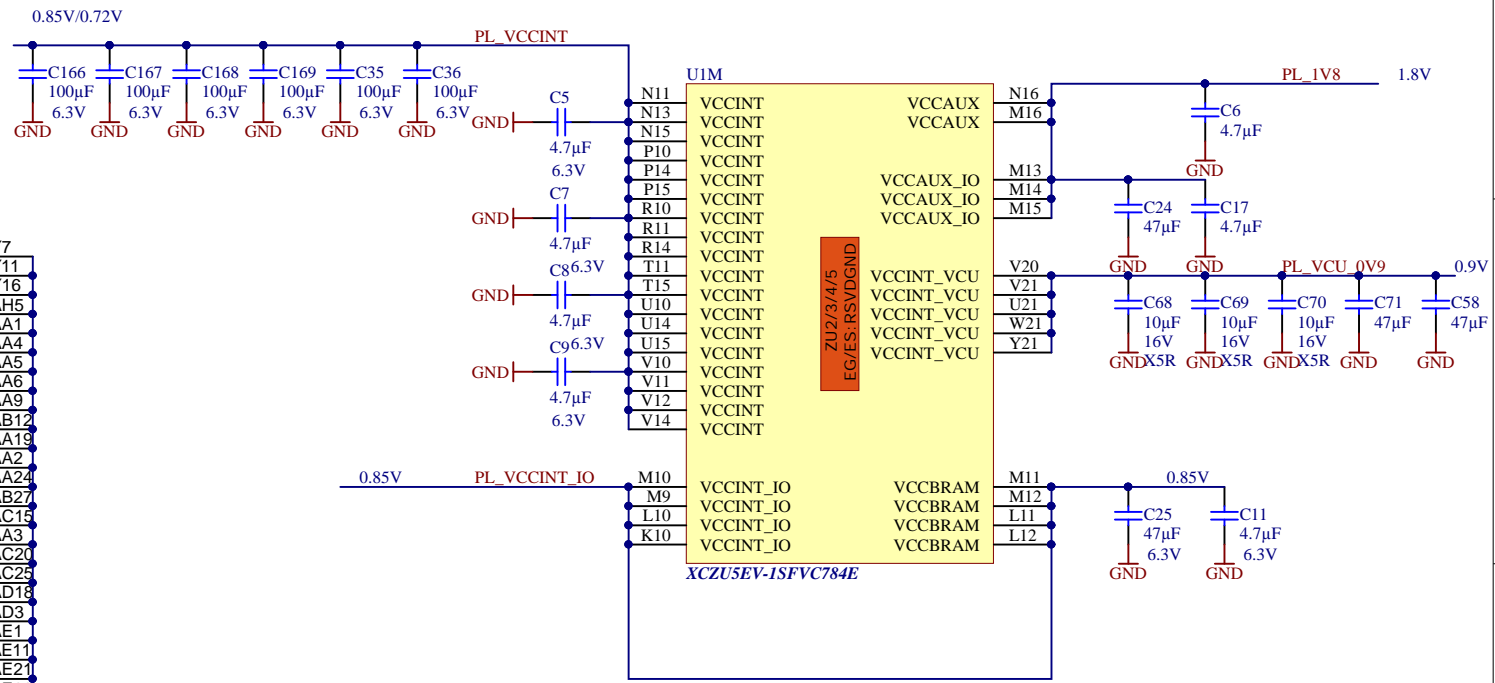
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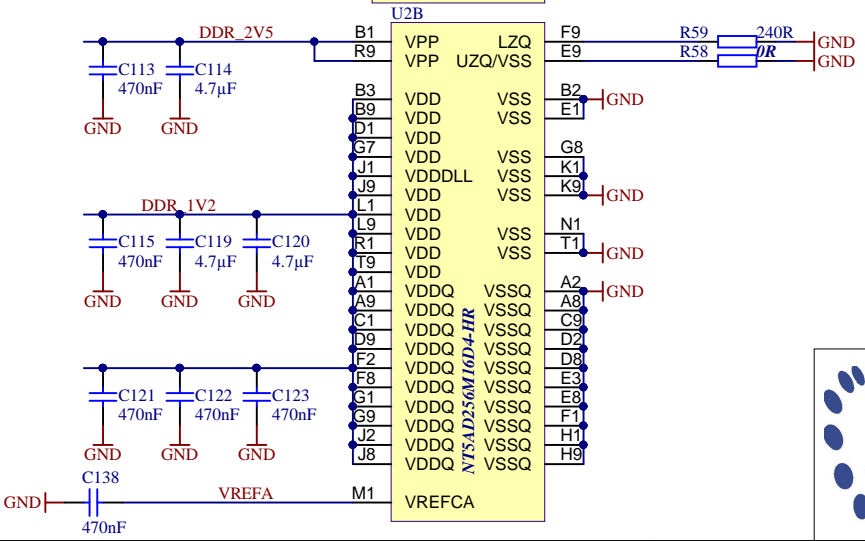
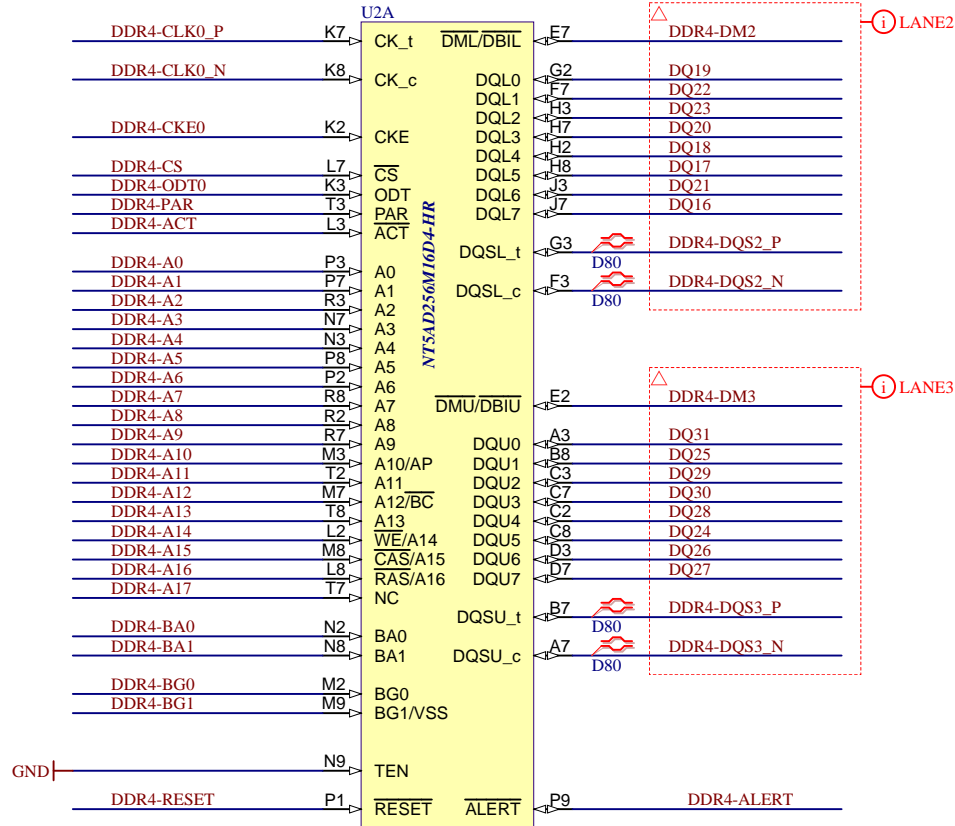
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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: B_GT.SchDoc		Page 14 of 26	



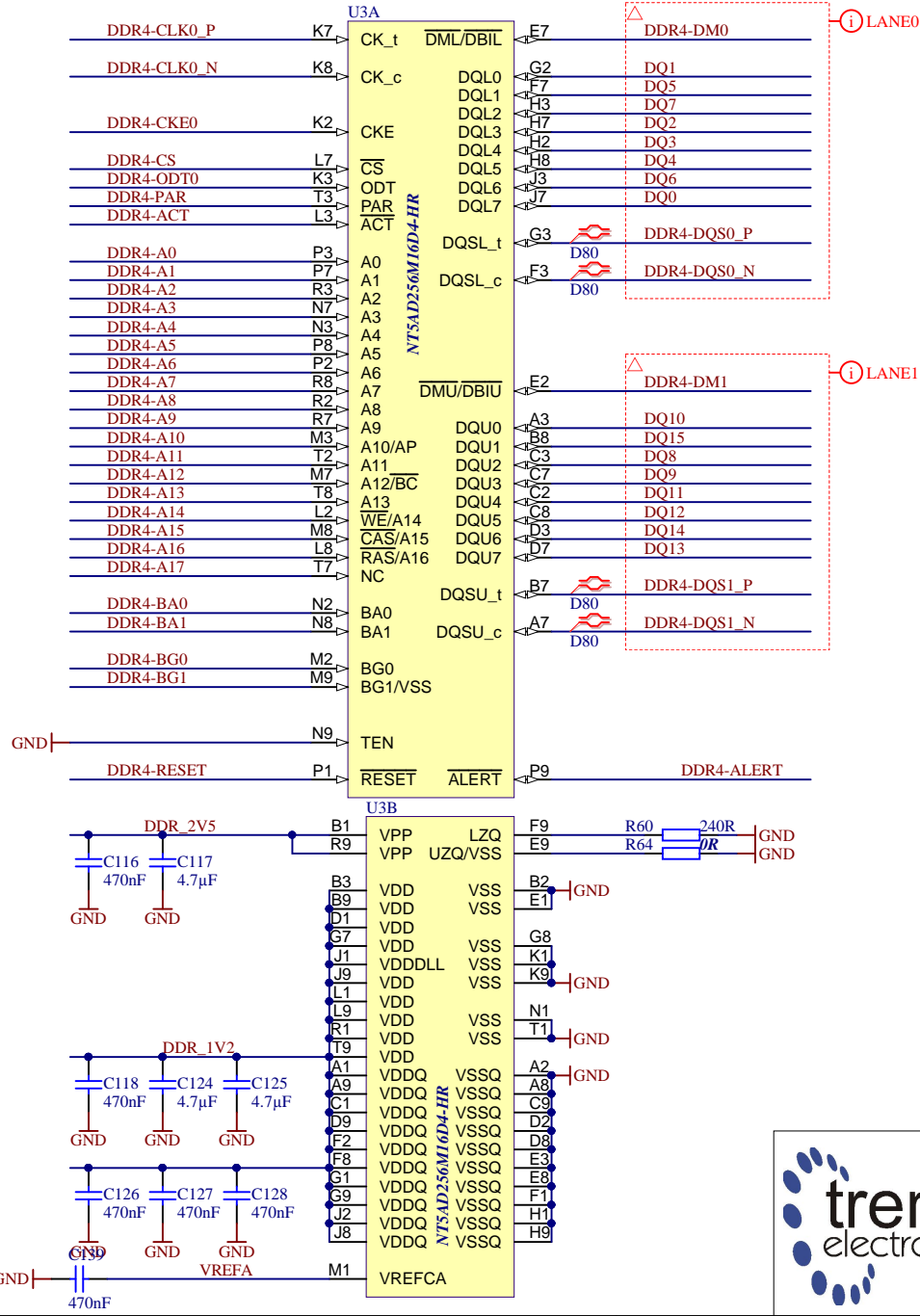
	Title: TE0803 - ZU_PS_POWER		
	A4	Number: TE0803 5DE11-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 15 of 26
	Filename: ZU_PS_POWER.SchDoc		



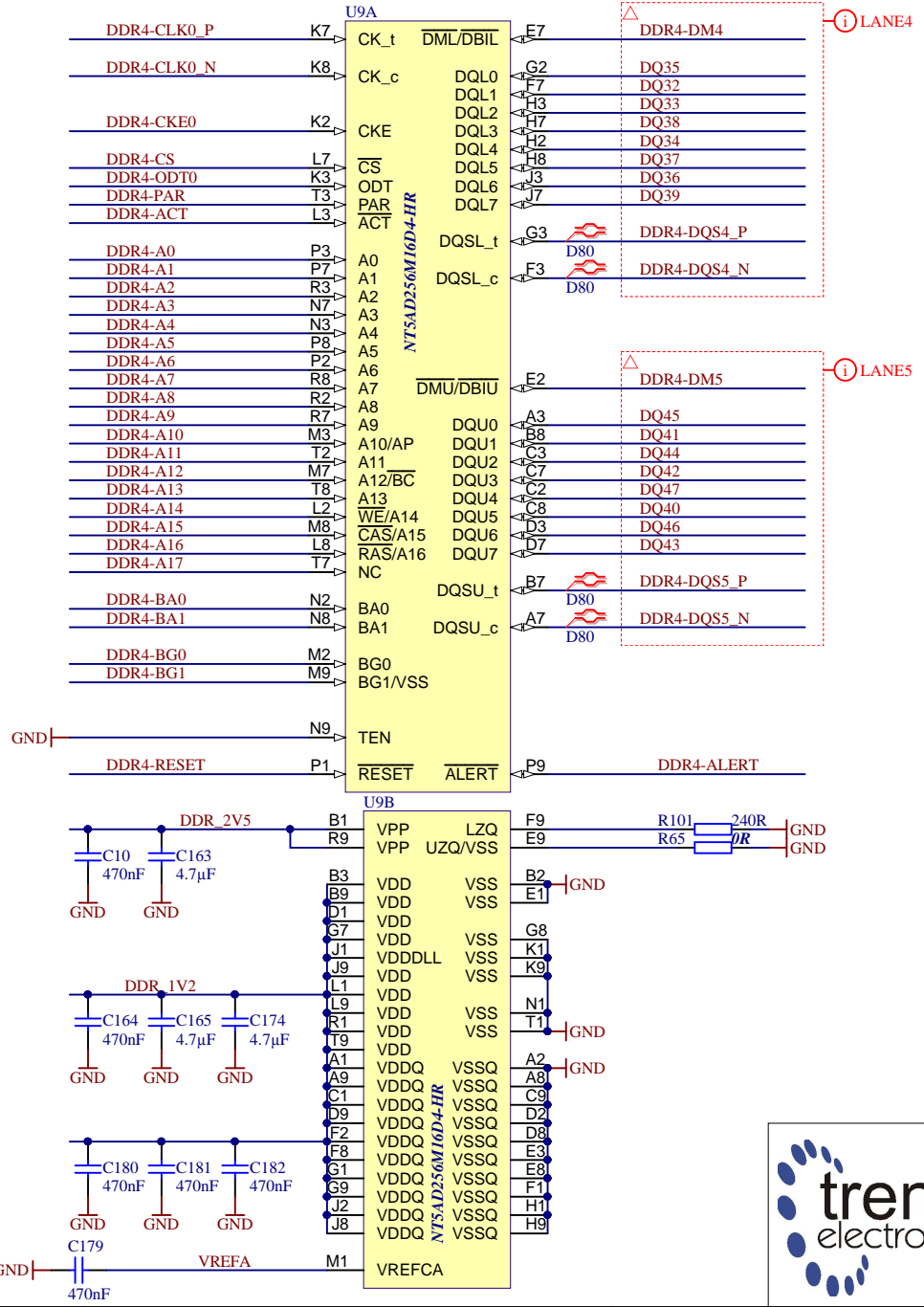
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	Date: <b>2019-02-21</b>	Copyright: <b>Trenz Electronic GmbH / TT</b>	Page <b>16</b> of <b>26</b>
	Filename: <b>ZU_POWER.SchDoc</b>		



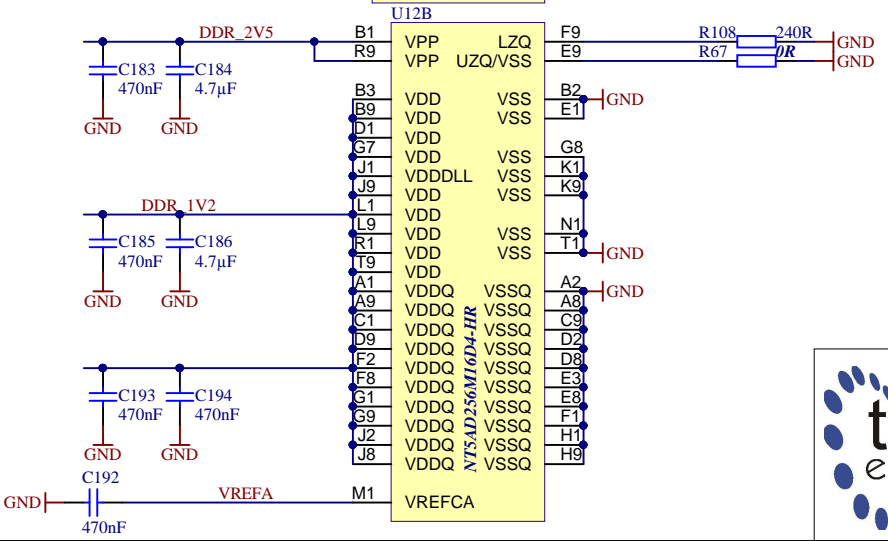
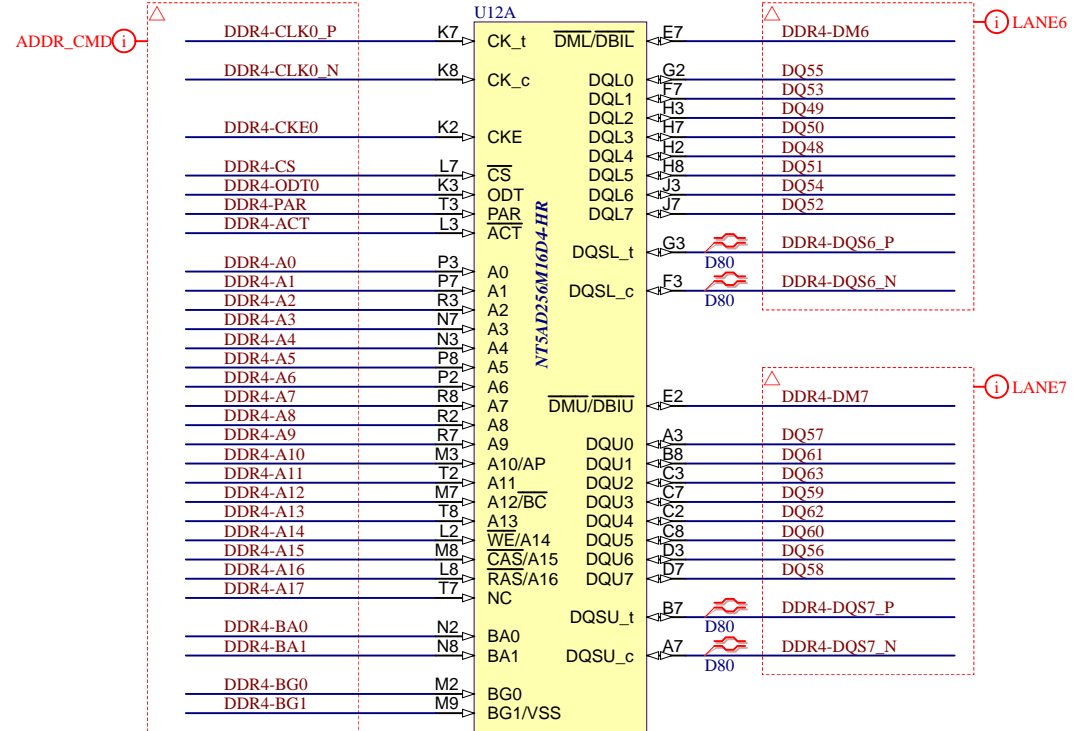
Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 5DE11-A	Rev. 03
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Filename: DDR4-RAM.SchDoc		



Title: TE0803 - DDR4_2_RAM		
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Filename: DDR4-RAM_2.SchDoc		

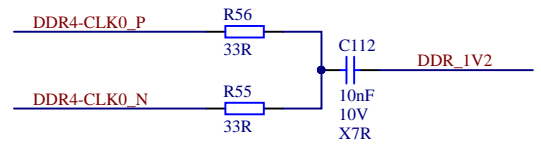
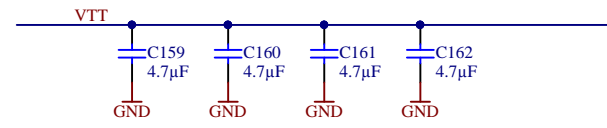
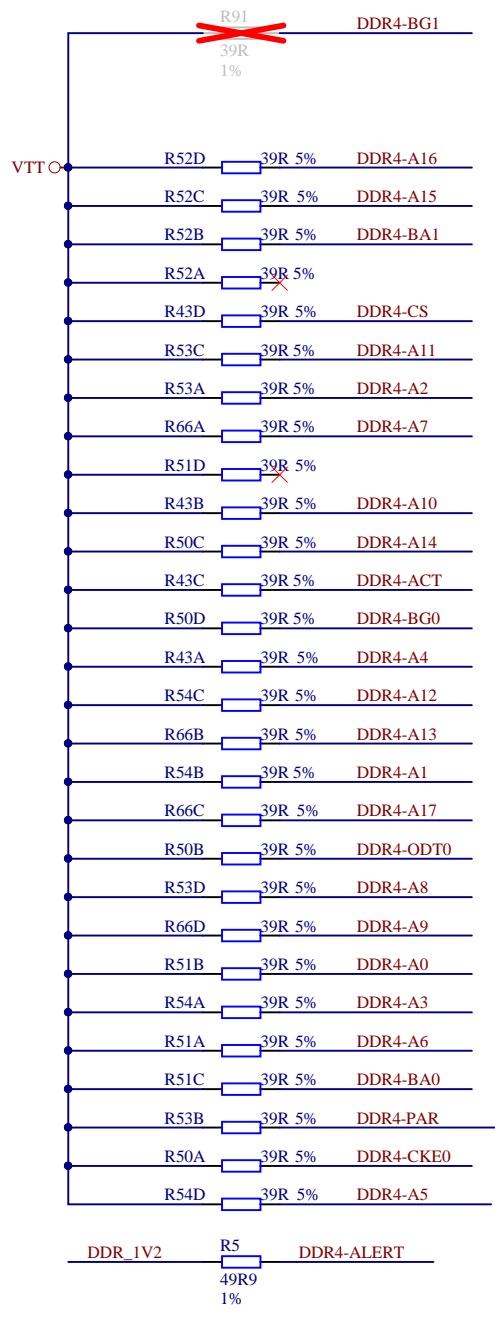


Title: TE0803 - DDR4_3_RAM		
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Filename: DDR4-RAM_3.SchDoc		

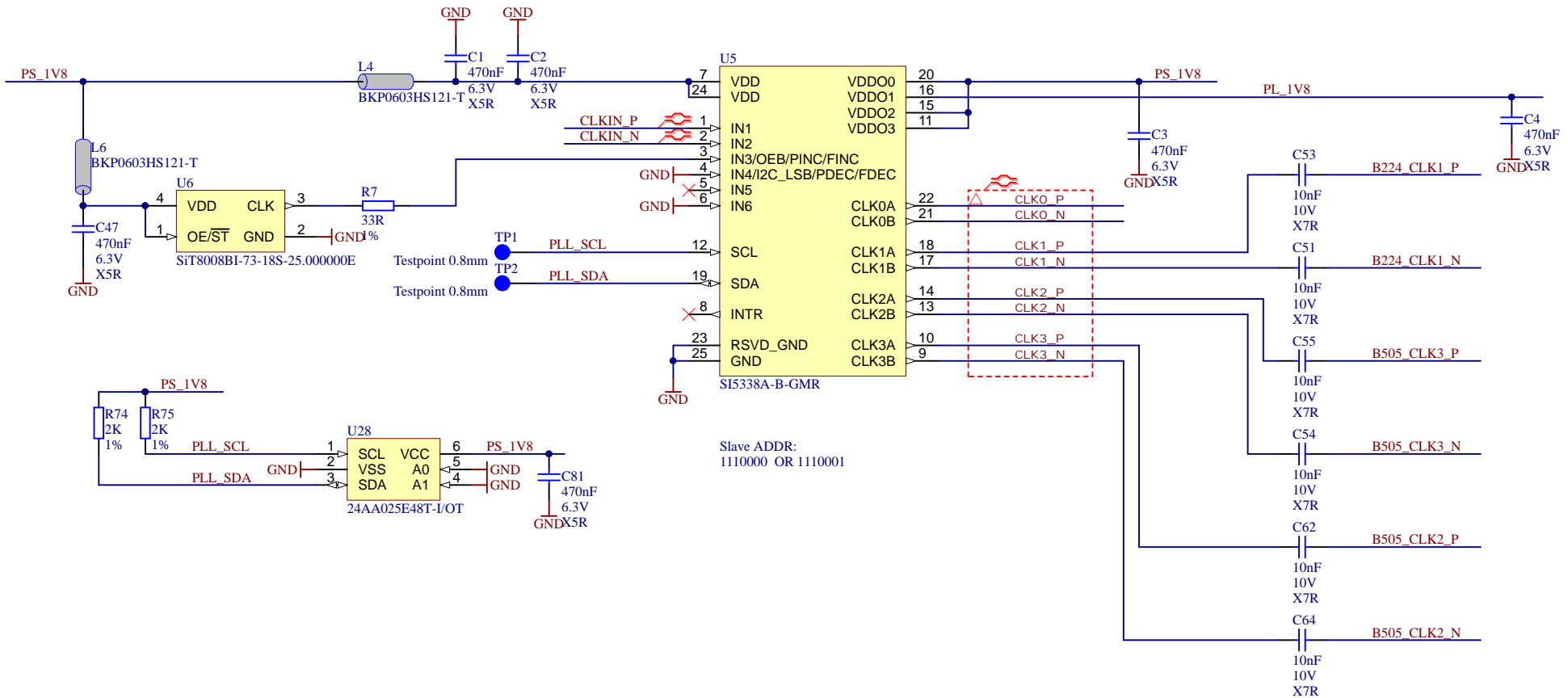



Title: TE0803 - DDR4_4_RAM		
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page20 of 26
Filename: DDR4-RAM_4.SchDoc		

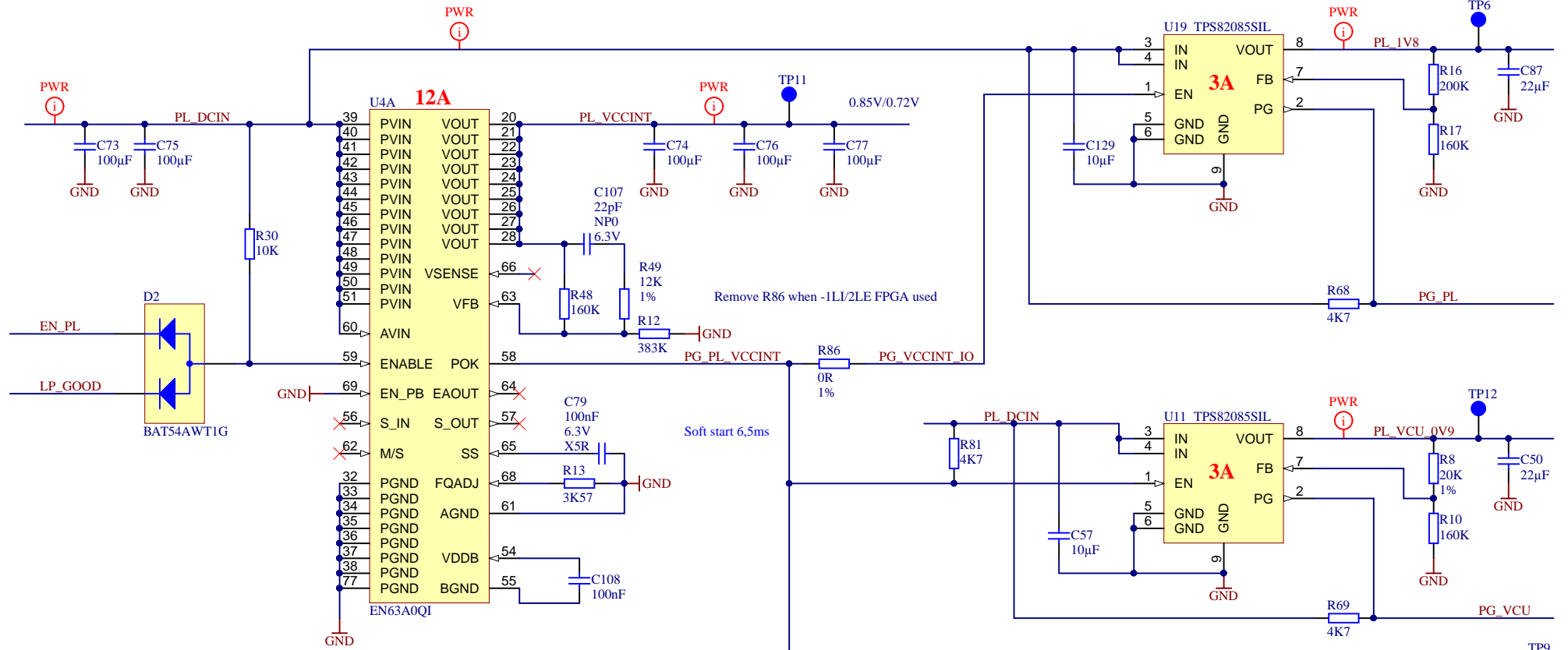




Title: TE0803 - DDR4_TERM		
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 21 of 26
Filename: DDR4-TERM.SchDoc		



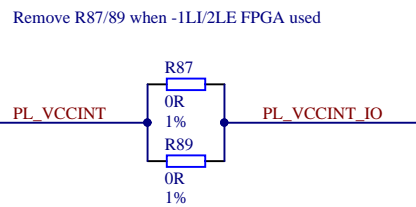
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		A4	Number: TE0803 5DE11-A
Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Page 22 of 26		Filename: Clock.SchDoc	



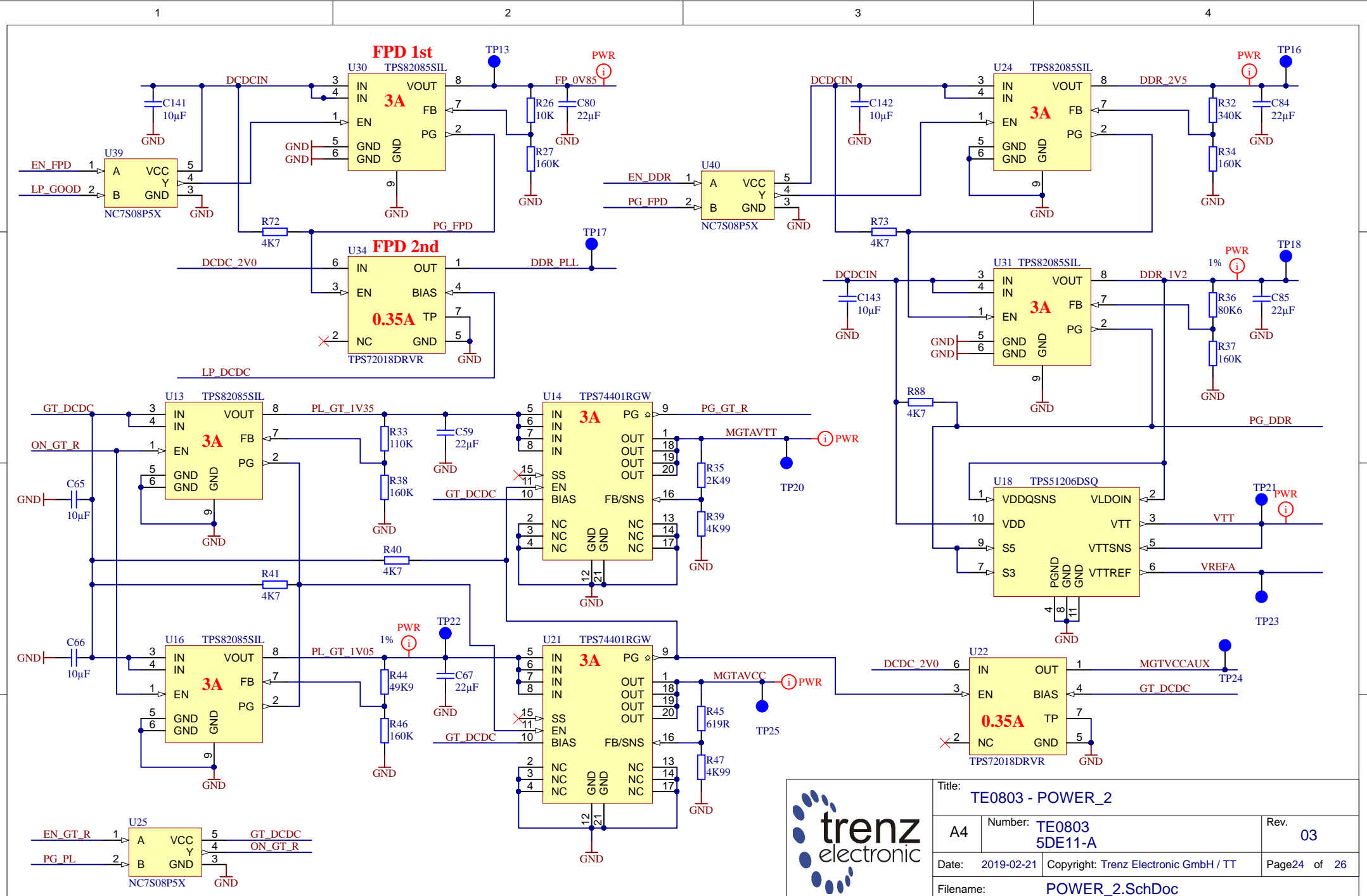
U4B

1	NC	NC	17
2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

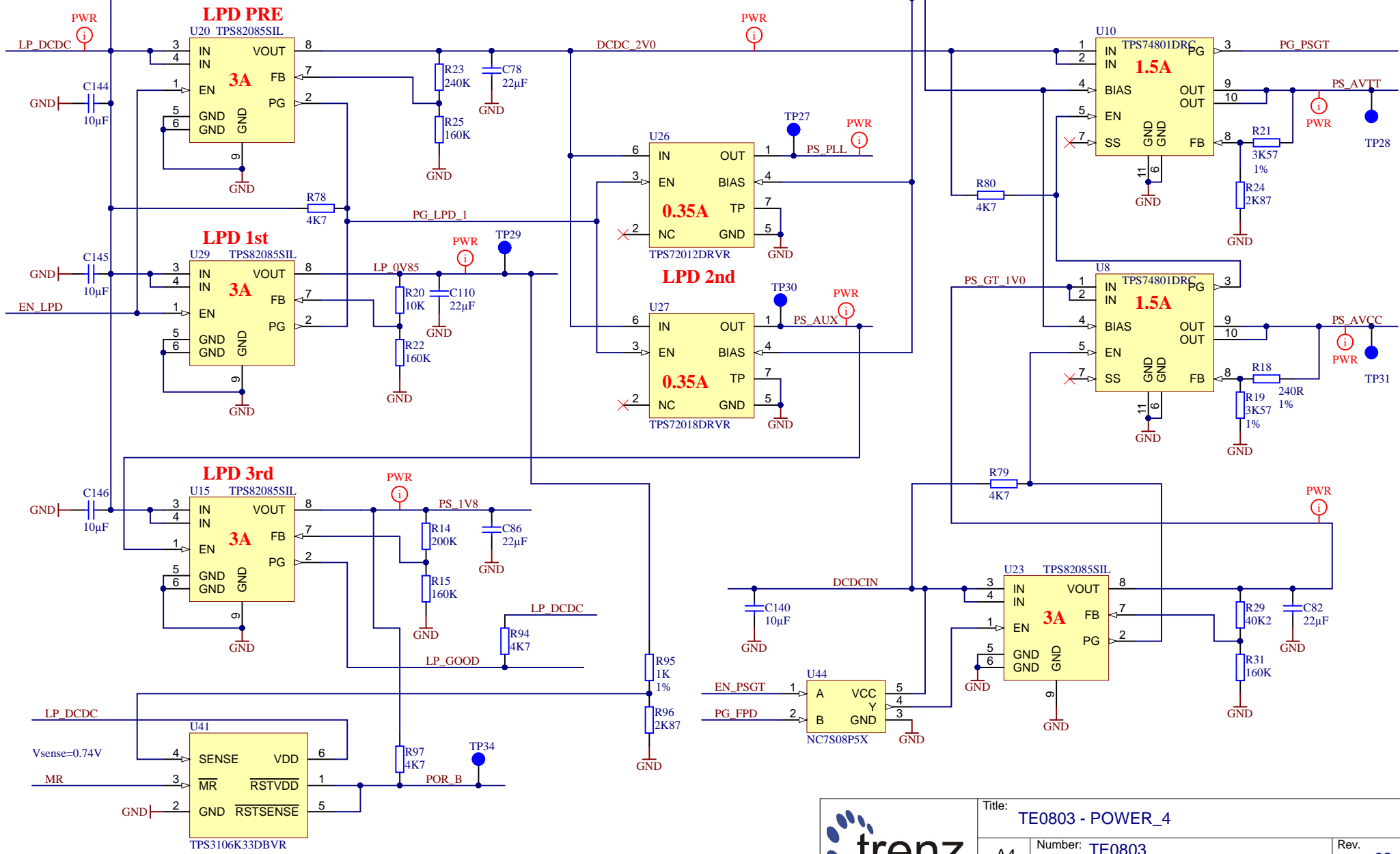
EN63A0QI



Title: TE0803 - POWER		
A4	Number: TE0803 5DE11-A	Rev. 03
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Filename: POWER.SchDoc		



Title: TE0803 - POWER_2		
A4	Number: TE0803 5DE11-A	Rev. 03
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Title: TE0803 - POWER_4		
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CHANGES REV01a (20.11.2017):

1) VCU voltage set to 0.9V, R20 changed to 40K , PL\_VCU\_1V0 renamed to PL\_VCU\_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR\_PLL
- 2) All differential pairs with length matched with tolerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS\_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

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		Title: TE0803 - Changes list		
		A4	Number: TE0803 5DE11-A	Rev. 03
		Date: 2019-02-21	Copyright: Trenz Electronic GmbH	Page 26 of 26
		Filename: Revision_Changes.SchDoc		

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