Arria V SoC Development Board

Reference Manual

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Chapter 3. Board Components Reference

Additional Information

1. Overview

This document describes the hardware features of the Arria® V SoC development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Arria V SoC development board provides a hardware platform for developing and prototyping low-power, high-performance, and logic-intensive designs using Altera's Arria V SoC. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Arria V SoC designs.

For more information about the Arria V device family, refer to the *Arria V Device Handbook*.

Board Component Blocks

The development board features the following major component blocks:

- One Arria V SoC (5ASTFD5K3F40I3) in a 1517-pin FBGA package
- FPGA configuration circuitry
  - Active Serial (AS) x1 or x4 configuration (EPCQ256SI16N)
  - MAX® V CPLD (5M2210ZF256) in a 256-pin FBGA package as the System Controller
  - Flash fast passive parallel (FPP) configuration
  - MAX II CPLD (EPM570GF100) as part of the on-board USB-Blaster™ II for use with the Quartus® II Programmer
- Clocking circuitry
  - Si570, Si571, and Si5338 programmable oscillators
  - 50-MHz, 66-MHz, 100-MHz, 125-MHz programmable oscillators
  - SMA input (LVCMOS)

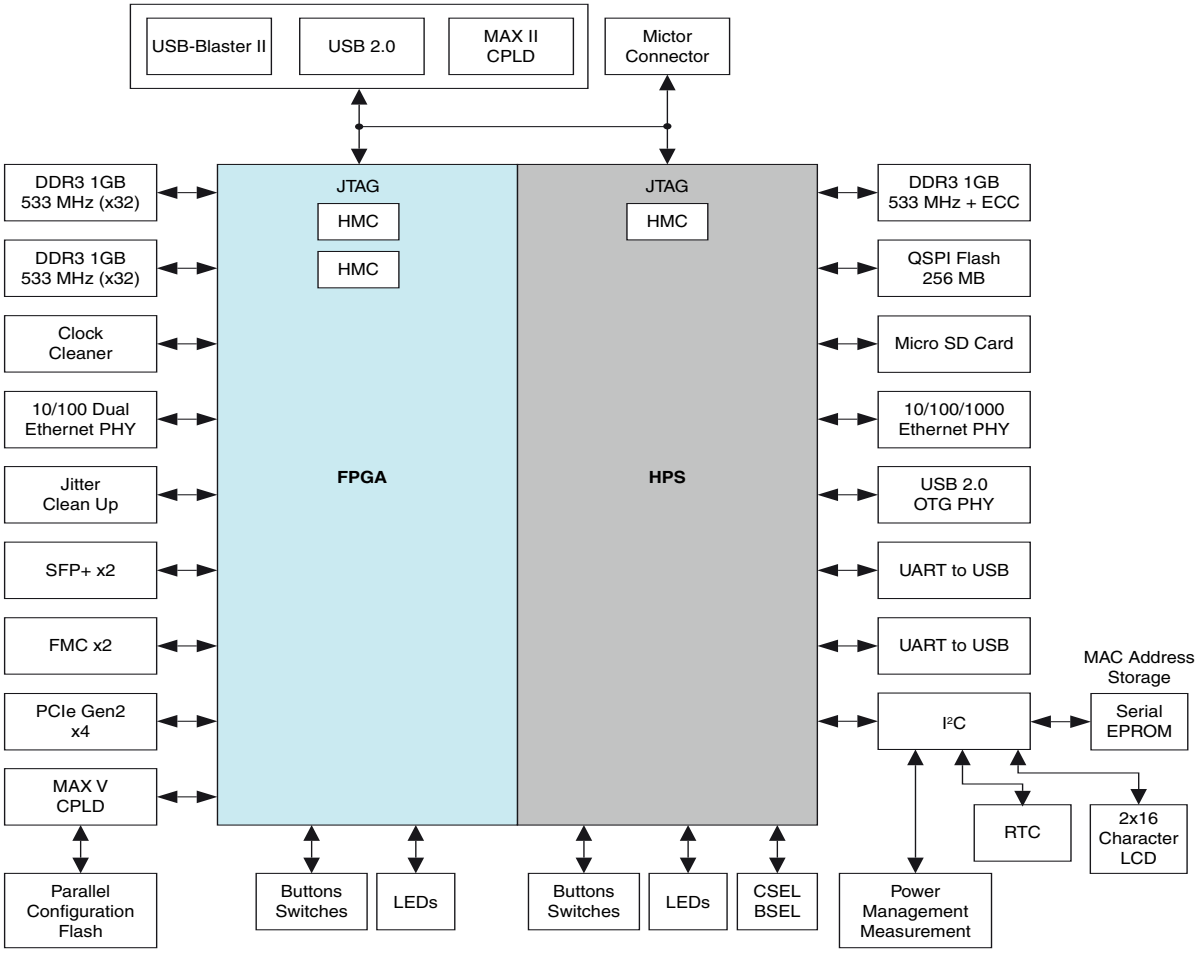
- Memory
  - One 1,024-Mbyte (MB) HPS DDR3 SDRAM with error correction code (ECC) support
  - Two 1,024-MB FPGA DDR3 SDRAM
  - One 512-Megabit (Mb) quad serial peripheral interface (QSPI) flash
  - One 512-Mb CFI synchronous flash
  - One 256-Mb NOR flash (EPCQ device)
  - One 32-Kilobit (Kb) I^2C serial electrically erasable PROM (EEPROM)
  - One Micro SD flash memory card
- Communication Ports
  - One PCI Express x4 Gen1/Gen2 socket
  - Two FPGA mezzanine card (FMC) ports
  - One USB 2.0 on-the-go (OTG) port
  - One Gigabit Ethernet port
  - Two 10/100 Ethernet ports
  - Two SFP+ ports
  - Two RS-232 UART (through the mini-USB port)
  - One real-time clock

- General user input/output
  - LEDs and displays
    - Eight user LEDs
    - One configuration load LED
    - One configuration done LED
    - One error LED
    - Three configuration select LEDs
    - Four on-board USB-Blaster II status LEDs
    - Two FMC interface LEDs
    - Two UART data transmit and receive LEDs
    - One power on LED
    - One two-line character LCD display
  - Push buttons
    - One CPU reset push button
    - One MAX V reset push button
    - One program select push button
    - One program configuration push button
    - Eight general user push buttons
  - DIP switches
    - One JTAG chain control DIP switch
    - One board settings DIP switch
    - One FPGA configuration mode DIP switch
    - One general user DIP switch
- Power supply
  - 14–20 V (laptop) DC input
- Mechanical
  - 7.175" × 9" rectangular form factor

Development Board Block Diagram

Figure 1–1 shows a block diagram of the Arria V SoC development board.

Figure 1–1. Arria V SoC Development Board Block Diagram



Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces the major components on the Arria V SoC development board. Figure 2–1 illustrates the component locations and Table 2–1 provides a brief description of all component features of the board.

A complete set of schematics, a physical layout database, and fabrication files for the development board reside in the Arria V SoC development kit board design files directory.

For information about powering up the board and installing the demonstration software, refer to the *Arria V SoC Development Kit User Guide.*

This chapter consists of the following sections:

Board Overview

This section provides an overview of the Arria V SoC development board, including an annotated board image and component descriptions. Figure 2–1 shows an overview of the board features.

Figure 2–1. Overview of the Arria V SoC Development Board

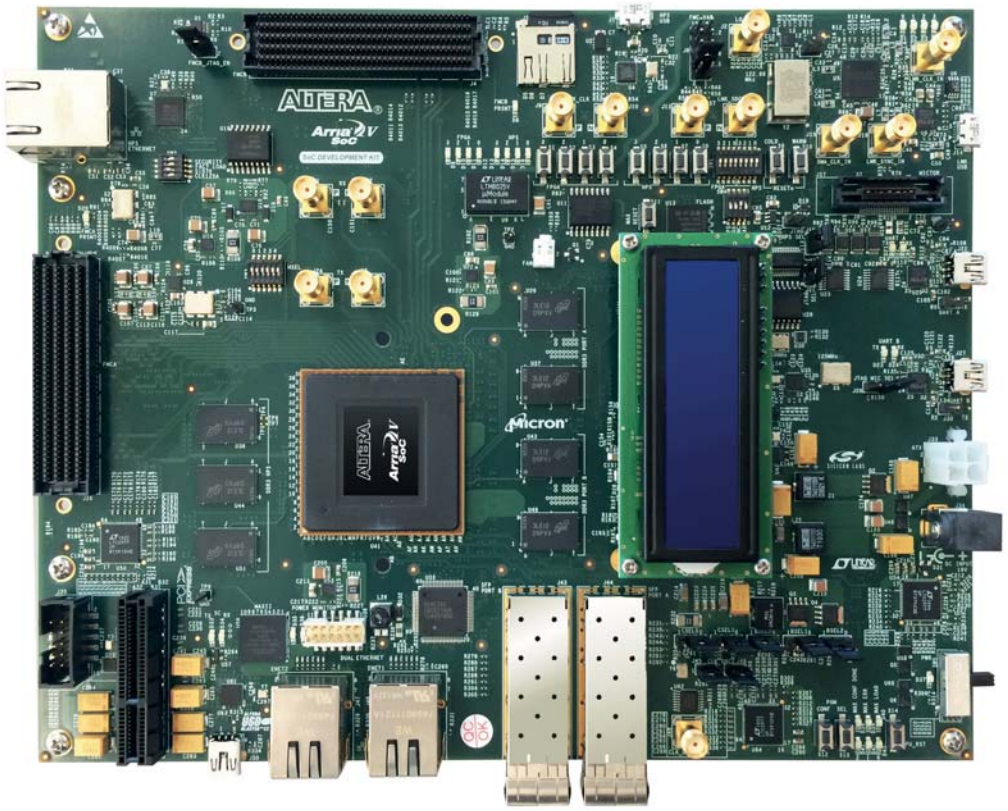


Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Board Components (Part 1 of 3)

Board Reference	Type	Description
Featured Devices		
U41	FPGA	Arria V SoC, 5ASTFD5K3F40I3, 1517-pin FBGA.
U27	CPLD	MAX V CPLD, 5M2210ZF256, 256-pin FBGA.
Configuration, Status, and Setup Elements		
J35	JTAG chain header	Provides access to the JTAG chain and disables the On-board USB-Blaster II when using an external USB-Blaster cable.
SW4	JTAG chain control DIP switch	Remove or include devices in the active JTAG chain.
J50	Mini-USB header	USB interface for FPGA programming and debugging through the On-board USB-Blaster II JTAG via a type-B USB cable.

Table 2–1. Board Components (Part 2 of 3)

Board Reference	Type	Description
SW2	Board settings DIP switch	Controls the MAX V CPLD 5M2210 System Controller functions such as clock enable, SMA clock input control, and which image to load from flash memory at power-up.
SW3	MSEL DIP switch	Controls the configuration scheme on the board. MSEL pins 0, 1, 2, 3, and 4 connects to the DIP switch.
S13	Program select push button	Toggles the program select LEDs, which selects the program image that loads from flash memory to the FPGA.
S12	Configure push button	Load image from flash memory to the FPGA based on the settings of the program select LEDs.
D38	Configuration done LED	Illuminates when the FPGA is configured.
D40	Load LED	Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA.
D39	Error LED	Illuminates when the FPGA configuration from flash memory fails.
D37	Power LED	Illuminates when 5.0 V power is present.
D35, D36	JTAG TX/RX LEDs	Indicate the transmit or receive activity of the JTAG chain. The TX and RX LEDs would flicker if the link is in use and active. The LEDs are either off when not in use or on when in use but idle.
D41–D43	Program select LEDs	Illuminates to show which flash memory image loads to the FPGA when you press the program select push button. Refer to Table 2–5 for the LED settings.
D8, D20	FMC port present LEDs	Illuminates when a daughter card is plugged into the FMC port.
D21–D24	UART LEDs	Illuminates when UART transmitter and receiver are in use.
Clock Circuitry		
X2	Programmable oscillator	Si570 programmable oscillator with a default frequency of 100 MHz. The frequency is programmable using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X3	148.5-MHz oscillator	Si571 programmable oscillator with a default frequency of 148.5 MHz. The frequency is programmable using the clock control GUI running on the MAX V CPLD 5M2210 System Controller.
X4	50-MHz oscillator	50.000-MHz crystal oscillator for general purpose logic.
X5	125-MHz oscillator	125.000-MHz crystal oscillator for general purpose logic.
J15	Clock input SMA connector	Drive LVCMOS-compatible clock input into the dedicated clock pin.
J49	HPS SMA clock	Drive LVCMOS to HPS clock multiplexer.
U35	Multi-output oscillator	Si5338A quad-output fixed oscillator with 25M, 25M, 100M, and 100M outputs.
General User Input/Output		
D9–D16	User LEDs	Four user LEDs and four HPS LEDs. Illuminates when driven low.
SW1	User DIP switch	User DIP switch. When the switch is ON, a logic 0 is selected.
S14	CPU reset push button	Reset the FPGA logic.
S11	MAX V reset push button	Reset the MAX V CPLD 5M2210 System Controller.
S1–S8	General user push buttons	Four user push buttons and four HPS push buttons. Driven low when pressed.

Table 2–1. Board Components (Part 3 of 3)

Board Reference	Type	Description
Memory Devices		
U29, U37, U43, U49, U38, U44, U51	DDR3 SDRAM	Four 128-MB DDR3 SDRAM with a 16-bit data bus for the FPGA and three 128-MB DDR3 SDRAM with a 16-bit data plus ECC bus for the HPS.
U19	QSPI flash	1-Gb serial NOR flash with 4-bit data bus.
U28	EPCQ flash	
U13	Synchronous flash	128-Mb synchronous flash devices with a 16-bit data bus for non-volatile memory.
U34	I^2C EEPROM	32-Kb I^2C serial EEPROM.
Communication Ports		
J42	PCI Express socket	PCI Express Gen1/Gen2 ×4 socket.
J4, J26	FMC port	Two FMC ports
J43, J44	SFP+ port	Two SFP+ ports
U7, J13	Gigabit Ethernet port	RJ-45 connectors which provides a 10/100/1000 Ethernet connection via a Micrel KSZ9021RN PHY and the FPGA-based Altera Triple Speed Ethernet MegaCore function in RGMII mode (for HPS).
U55, J47, J48	Dual Ethernet port	RJ-45 connector which provides a 10/100 Ethernet connection via a Renesas uPD60620 PHY in MII mode (for FPGA).
J22, U25 J27, U36	USB-UART ports	USB connector with USB-to-UART bridge for serial UART interface.
J1, U4	USB OTG port	USB 2.0 on-the-go interface.
U11	Real-time clock	DS1339 device with built-in power sense circuit that detects power failures and automatically switches to backup battery supply, maintaining time.
J5	Micro SD card socket	Micro SD card interface with 4-bit data line.
Video and Display Ports		
J29	Character LCD	Connector that interfaces to a provided 16 character × 2 line LCD module along with two standoffs.
Power Supply		
J34	DC input jack	Accepts 16 V DC power supply.
SW5	Power switch	Switch to power on or off the board when power is supplied from the DC input jack.

Featured Device: Arria V SoC

The Arria V SoC development board features a Arria V SoC 5ASTFD5K3F40I3 device (U41) that includes a hard processor system (HPS) with integrated ARM® Cortex®-A9 MPCore processor.

For more information about Arria V device family, refer to the *Arria V Device Handbook*.

Table 2–2 describes the features of the Arria V SoC device.

Table 2–2. Arria V SoC Features

Resource		5ASTFD5K3F40I3
LE (K)		462
ALM		174,340
Register		697,360
Memory (Kb)	M10K	22,820
	MLAB	2,658
18-bit × 18-bit Multiplier		2,180
PLLs	FPGA	14
	HPS	3
Transceivers	6 Gbps	30
	10 Gbps	16

I/O Resources

The Arria V SoC 5ASTFD5K3F40I3 device has 540 general purpose FPGA I/O pins and 210 general purpose HPS I/O pins.

MAX V CPLD 5M2210 System Controller

The board utilizes the 5M2210ZF256 System Controller, an Altera MAX V CPLD, for the following purposes:

- FPGA configuration from flash
- Power measurement
- Control and status registers (CSR) for remote system update

Figure 2–2 illustrates the MAX V CPLD 5M2210 System Controller's functionality and external circuit connections as a block diagram.

Figure 2–2. MAX V CPLD 5M2210 System Controller Block Diagram

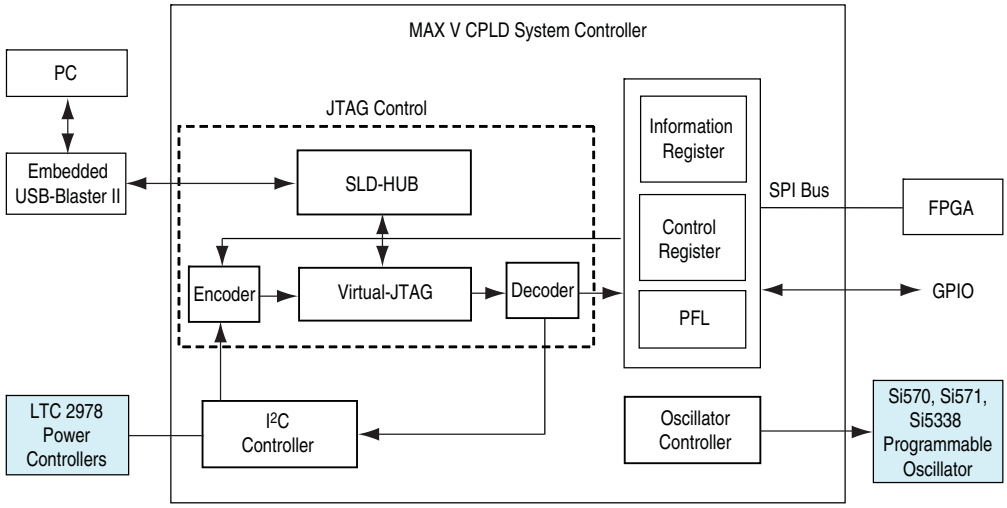


Table 2–3 lists the I/O signals present on the MAX V CPLD System Controller. The signal names and functions are relative to the MAX V device.

Table 2–3. MAX V CPLD System Controller Device Pin-Out (Part 1 of 5)

Board Reference (U27)	Schematic Signal Name	I/O Standard	Description
B9	CLK125A_EN	2.5 V	125 MHz oscillator enable
E9	CLK50_EN	2.5 V	50 MHz oscillator enable
J5	CLK_100M_MAX	2.5 V	100 MHz clock input
J12	CLK_50M_MAX	1.8 V	50 MHz clock input
D10	CPU_RESETn	2.5 V	FPGA reset push button
N11	EXTRA_SIG0	1.5 V	On-board USB-Blaster II interface. Reserved for future use
T13	EXTRA_SIG1	1.5 V	On-board USB-Blaster II interface. Reserved for future use
T15	EXTRA_SIG2	1.5 V	On-board USB-Blaster II interface. Reserved for future use
A2	FACTORY_LOAD	2.5 V	DIP switch to load factory or user design at power-up
R14	FACTORY_REQUEST	1.5 V	On-board USB-Blaster II request to send FACTORY command
N12	FACTORY_STATUS	1.5 V	On-board USB-Blaster II FACTORY command status
F11	FLASH_ADVN	1.8 V	FSM bus flash memory address valid
N14	FLASH_CEN0	1.8 V	FSM bus flash memory chip enable
D14	FLASH_CLK	1.8 V	FSM bus flash memory clock
P15	FLASH_OEN	1.8 V	FSM bus flash memory output enable
P14	FLASH_RDYBSYN	1.8 V	FSM bus flash memory ready
D13	FLASH_RESETn	1.8 V	FSM bus flash memory reset
N15	FLASH_WEN	1.8 V	FSM bus flash memory write enable
E14	FM_A0	1.8 V	FM address bus

Table 2–3. MAX V CPLD System Controller Device Pin-Out (Part 2 of 5)

Board Reference (U27)	Schematic Signal Name	I/O Standard	Description
C14	FM_A1	1.8 V	FM address bus
C15	FM_A2	1.8 V	FM address bus
E13	FM_A3	1.8 V	FM address bus
E12	FM_A4	1.8 V	FM address bus
D15	FM_A5	1.8 V	FM address bus
F14	FM_A6	1.8 V	FM address bus
D16	FM_A7	1.8 V	FM address bus
F13	FM_A8	1.8 V	FM address bus
E15	FM_A9	1.8 V	FM address bus
E16	FM_A10	1.8 V	FM address bus
F15	FM_A11	1.8 V	FM address bus
G14	FM_A12	1.8 V	FM address bus
F16	FM_A13	1.8 V	FM address bus
G13	FM_A14	1.8 V	FM address bus
G15	FM_A15	1.8 V	FM address bus
G12	FM_A16	1.8 V	FM address bus
G16	FM_A17	1.8 V	FM address bus
H14	FM_A18	1.8 V	FM address bus
H15	FM_A19	1.8 V	FM address bus
H13	FM_A20	1.8 V	FM address bus
H16	FM_A21	1.8 V	FM address bus
J13	FM_A22	1.8 V	FM address bus
J16	FM_A23	1.8 V	FM address bus
K12	FM_A24	1.8 V	FM address bus
M14	FM_A25	1.8 V	FM address bus
N13	FM_A26	1.8 V	FM address bus
J14	FM_D0	1.8 V	FM data bus
J15	FM_D1	1.8 V	FM data bus
K16	FM_D2	1.8 V	FM data bus
K13	FM_D3	1.8 V	FM data bus
K15	FM_D4	1.8 V	FM data bus
K14	FM_D5	1.8 V	FM data bus
L16	FM_D6	1.8 V	FM data bus
L11	FM_D7	1.8 V	FM data bus
L15	FM_D8	1.8 V	FM data bus
L12	FM_D9	1.8 V	FM data bus
M16	FM_D10	1.8 V	FM data bus
L13	FM_D11	1.8 V	FM data bus
M15	FM_D12	1.8 V	FM data bus

Table 2–3. MAX V CPLD System Controller Device Pin-Out (Part 3 of 5)

Board Reference (U27)	Schematic Signal Name	I/O Standard	Description
L14	FM_D13	1.8 V	FM data bus
N16	FM_D14	1.8 V	FM data bus
M13	FM_D15	1.8 V	FM data bus
M3	FMC_C2M_PG	2.5 V	FMC port A power good output
N2	FMCB_C2M_PG	2.5 V	FMC port B power good output
K1	FPGA_CONF_DONE	2.5 V	FPGA configuration done
D3	FPGA_CONFIG_D0	2.5 V	FPGA configuration data
C2	FPGA_CONFIG_D1	2.5 V	FPGA configuration data
C3	FPGA_CONFIG_D2	2.5 V	FPGA configuration data
E3	FPGA_CONFIG_D3	2.5 V	FPGA configuration data
D2	FPGA_CONFIG_D4	2.5 V	FPGA configuration data
E4	FPGA_CONFIG_D5	2.5 V	FPGA configuration data
D1	FPGA_CONFIG_D6	2.5 V	FPGA configuration data
E5	FPGA_CONFIG_D7	2.5 V	FPGA configuration data
F3	FPGA_CONFIG_D8	2.5 V	FPGA configuration data
E1	FPGA_CONFIG_D9	2.5 V	FPGA configuration data
F4	FPGA_CONFIG_D10	2.5 V	FPGA configuration data
F2	FPGA_CONFIG_D11	2.5 V	FPGA configuration data
F1	FPGA_CONFIG_D12	2.5 V	FPGA configuration data
F6	FPGA_CONFIG_D13	2.5 V	FPGA configuration data
G2	FPGA_CONFIG_D14	2.5 V	FPGA configuration data
G3	FPGA_CONFIG_D15	2.5 V	FPGA configuration data
N3	FPGA_CVP_CONFDONE	2.5 V	FPGA Configuration via Protocol (CvP) done
J3	FPGA_DCLK	2.5 V	FPGA configuration clock
N1	FPGA_NCONFIG	2.5 V	FPGA configuration active
J4	FPGA_NSTATUS	2.5 V	FPGA configuration status
H1	FPGA_PR_DONE	2.5 V	FPGA partial reconfiguration done
P2	FPGA_PR_ERROR	2.5 V	FPGA partial reconfiguration error
E2	FPGA_PR_READY	2.5 V	FPGA partial reconfiguration ready
F5	FPGA_PR_REQUEST	2.5 V	FPGA partial reconfiguration request
B11	HPS_RESETn	2.5 V	HPS reset push button
M1	I2C_SCL_MAX	2.5 V	Programmable oscillator I^2C clock
M2	I2C_SDA_MAX	2.5 V	Programmable oscillator I^2C data
L6	JTAG_MAX_TDI	2.5 V	JTAG chain data in
M5	JTAG_MAX_TDO	2.5 V	JTAG chain data out
N4	JTAG_MAX_TMS	2.5 V	JTAG chain mode
P3	JTAG_MUX_TCK	2.5 V	JTAG chain clock
P11	M570_CLOCK	1.5 V	25-MHz clock to on-board USB-Blaster II for sending FACTORY command

Table 2–3. MAX V CPLD System Controller Device Pin-Out (Part 4 of 5)

Board Reference (U27)	Schematic Signal Name	I/O Standard	Description
L5	M570_PCIE_JTAG_EN	2.5 V	PCI Express JTAG enable for the on-board USB-Blaster II
H2	MAX_AS_CONF	2.5 V	Driven low to enable AS configuration from the EPCQ flash through U13 to the FPGA
E11	MAX_CONF_DONE	2.5 V	On-board USB-Blaster II configuration done LED
A4	MAX_ERROR	2.5 V	FPGA configuration error LED
G4	MAX_FPGA_MISO	2.5 V	FPGA to MAX V SPI bus data output
G1	MAX_FPGA_MOSI	2.5 V	FPGA to MAX V SPI bus data input
H3	MAX_FPGA_SCK	2.5 V	FPGA to MAX V SPI bus clock
G5	MAX_FPGA_SSEL	2.5 V	FPGA to MAX V SPI bus slave select
A6	MAX_LOAD	2.5 V	FPGA configuration active LED
K2	MAX_QSPI_RSTN	2.5 V	QSPI reset
M9	MAX_RESETn	2.5 V	MAX V reset push button
B10	MSEL0	2.5 V	FPGA MSEL0 setting
B3	MSEL1	2.5 V	FPGA MSEL1 setting
C10	MSEL2	2.5 V	FPGA MSEL2 setting
C12	MSEL3	2.5 V	FPGA MSEL3 setting
C6	MSEL4	2.5 V	FPGA MSEL4 setting
E10	OVERTEMP	2.5 V	Temperature monitor fan enable
D12	PGM_CONFIG	2.5 V	Load the flash memory image identified by the PGM LEDs
B14	PGM_LED0	2.5 V	Flash memory PGM select indicator 0
C13	PGM_LED1	2.5 V	Flash memory PGM select indicator 1
B16	PGM_LED2	2.5 V	Flash memory PGM select indicator 2
B13	PGM_SEL	2.5 V	Toggles the PGM_LED[2:0] LED sequence
P13	RST	1.5 V	Reset input
R12	SECURITY_MODE	1.5 V	DIP switch for the On-board USB-Blaster II to send FACTORY command at power up
A10	SI570_EN	2.5 V	Si570 programmable clock enable
D4	SI571_EN	2.5 V	Si571 programmable clock enable
R16	TRST	1.5 V	Reset output
H5	USB_B2_CLK	2.5 V	On-board USB-Blaster II interface clock
R4	USB_CFG0	1.5 V	On-board USB-Blaster II interface (reserved for future use)
T4	USB_CFG1	1.5 V	On-board USB-Blaster II interface (reserved for future use)
P8	USB_CFG2	1.5 V	On-board USB-Blaster II interface (reserved for future use)
T7	USB_CFG3	1.5 V	On-board USB-Blaster II interface (reserved for future use)
N8	USB_CFG4	1.5 V	On-board USB-Blaster II interface (reserved for future use)
R8	USB_CFG5	1.5 V	On-board USB-Blaster II interface (reserved for future use)
T8	USB_CFG6	1.5 V	On-board USB-Blaster II interface (reserved for future use)
T9	USB_CFG7	1.5 V	On-board USB-Blaster II interface (reserved for future use)
R9	USB_CFG8	1.5 V	On-board USB-Blaster II interface (reserved for future use)

Table 2–3. MAX V CPLD System Controller Device Pin-Out (Part 5 of 5)

Board Reference (U27)	Schematic Signal Name	I/O Standard	Description
P9	USB_CFG9	1.5 V	On-board USB-Blaster II interface (reserved for future use)
M8	USB_CFG10	1.5 V	On-board USB-Blaster II interface (reserved for future use)
T10	USB_CFG11	1.5 V	On-board USB-Blaster II interface (reserved for future use)
A13	USB_FPGA_RESET	2.5 V	On-board USB-Blaster II interface FPGA reset
A11	USB_RESET	2.5 V	On-board USB-Blaster II interface reset

FPGA Configuration

This section describes the FPGA, flash memory, and MAX V CPLD 5M2210 System Controller device programming methods supported by the Arria V SoC development board.

The Arria V SoC development board supports the following configuration methods:

- JTAG
  - On-board USB-Blaster II is the default method for configuring the FPGA using the Quartus II Programmer in JTAG mode with the supplied USB cable.
  - External Mictor connector for configuring the HPS using the ARM DS-5 Altera Edition software and DSTREAM or Lauterbach cables.
  - External USB-Blaster for configuring the FPGA when you connect the external USB-Blaster to the JTAG header (J35).
- Flash memory download for configuring the FPGA using stored images from the flash memory on either power-up or pressing the configure push button (S12).

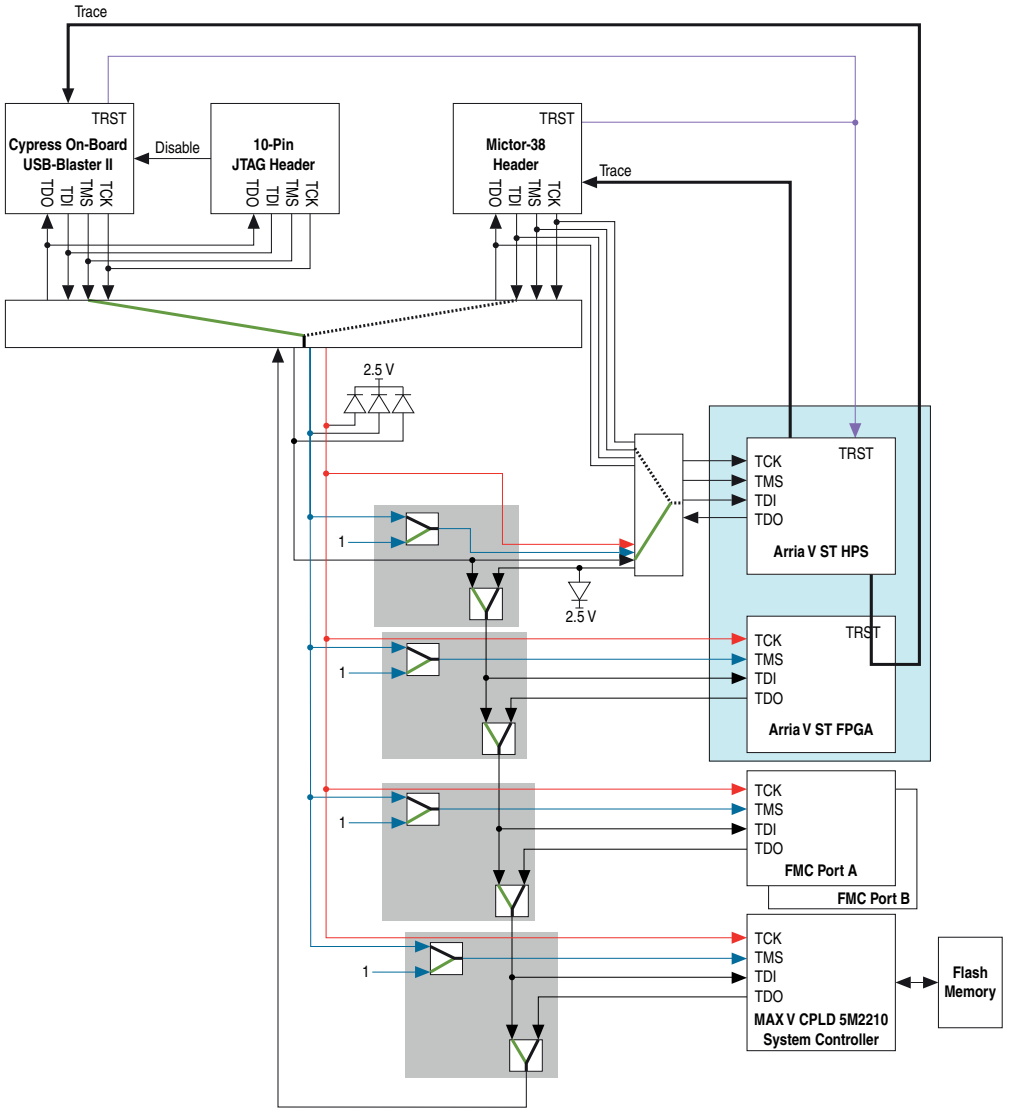
FPGA Programming over On-Board USB-Blaster II

This configuration method implements a mini-USB connector (J50), a USB 2.0 PHY device (U61), and an Altera MAX II CPLD EPM570GF100I5N (U56) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB connector on the board and a USB port on a PC running the Quartus II software.

The on-board USB-Blaster II in the MAX II CPLD EPM570GF100I5N normally masters the JTAG chain. The on-board USB-Blaster II shares the pins with the external header. and is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG header (J35). In addition to JTAG interface, the on-board USB-Blaster II has trace capabilities for HPS debug purposes. The trace interface from the HPS routes to the on-board USB-Blaster II connection pins through the FPGA.

Figure 2–3 illustrates the JTAG chain.

Figure 2–3. JTAG Chain



The JTAG chain control DIP switch (SW4) controls the jumpers shown in Figure 2–3. To connect a device or interface to the chain, their corresponding switch must be in the OFF position. Slide all the switches in the ON position to only have the FPGA in the chain.

The MAX V CPLD 5M2210 System Controller must be in the JTAG chain to use some of the GUI interfaces.

The MAX II CPLD (EPM570GF100) is dedicated to the on-board USB-Blaster II functionality only, connecting to the USB 2.0 PHY device on one side and drives JTAG signals out the other side on the GPIO pins. This device's own dedicated JTAG interface are routed to a small surface-mount header only intended for debugging of first article prototypes.

A USB 2.0 Cypress EZ-USB CY7C68013A device (U61) in a 56-pin VBGA package interfaces to a mini-USB connector.

Table 2–4 lists the USB 2.0 PHY schematic signal names and their corresponding MAX II CPLD pin numbers.

Table 2–4. USB 2.0 PHY Schematic Signal Names and Functions (Part 1 of 2)

Board Reference (U61)	Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
C1	24M_XTALIN	—	3.3 V	Crystal oscillator input
C2	24M_XTALOUT	—	3.3 V	Crystal oscillator output
E1	FX2_D_N	—	3.3 V	USB 2.0 PHY data
E2	FX2_D_P	—	3.3 V	USB 2.0 PHY data
H7	FX2_FLAGA	D1	3.3 V	Slave FIFO output status
G7	FX2_FLAGB	G1	3.3 V	Slave FIFO output status
H8	FX2_FLAGC	C1	3.3 V	Slave FIFO output status
G6	FX2_PA1	G3	3.3 V	USB 2.0 PHY port A interface
F8	FX2_PA2	B1	3.3 V	USB 2.0 PHY port A interface
F7	FX2_PA3	D2	3.3 V	USB 2.0 PHY port A interface
F6	FX2_PA4	D3	3.3 V	USB 2.0 PHY port A interface
C8	FX2_PA5	K4	3.3 V	USB 2.0 PHY port A interface
C7	FX2_PA6	F2	3.3 V	USB 2.0 PHY port A interface
C6	FX2_PA7	C2	3.3 V	USB 2.0 PHY port A interface
H3	FX2_PB0	G2	3.3 V	USB 2.0 PHY port B interface
F4	FX2_PB1	H8	3.3 V	USB 2.0 PHY port B interface
H4	FX2_PB2	F3	3.3 V	USB 2.0 PHY port B interface
G4	FX2_PB3	J3	3.3 V	USB 2.0 PHY port B interface
H5	FX2_PB4	F1	3.3 V	USB 2.0 PHY port B interface
G5	FX2_PB5	H1	3.3 V	USB 2.0 PHY port B interface
F5	FX2_PB6	H7	3.3 V	USB 2.0 PHY port B interface
H6	FX2_PB7	E1	3.3 V	USB 2.0 PHY port B interface
A8	C_USB_MAX_TCK	H3	3.3 V	USB 2.0 PHY port D interface
A7	C_USB_MAX_TDI	H2	3.3 V	USB 2.0 PHY port D interface
B6	C_USB_MAX_TDO	J2	3.3 V	USB 2.0 PHY port D interface
A6	C_USB_MAX_TMS	J1	3.3 V	USB 2.0 PHY port D interface
B3	FX2_PD4	J6	3.3 V	USB 2.0 PHY port D interface
A3	FX2_PD5	K3	3.3 V	USB 2.0 PHY port D interface
C3	FX2_PD6	J5	3.3 V	USB 2.0 PHY port D interface
A2	FX2_PD7	K2	3.3 V	USB 2.0 PHY port D interface

Table 2–4. USB 2.0 PHY Schematic Signal Names and Functions (Part 2 of 2)

Board Reference (U61)	Schematic Signal Name	MAX II CPLD Pin Number	I/O Standard	Description
B8	FX2_RESETn	K9	3.3 V	On-board USB-Blaster hard reset
F3	FX2_SCL	J4	3.3 V	USB 2.0 PHY serial clock
G3	FX2_SDA	—	3.3 V	USB 2.0 PHY serial data
A1	FX2_SLRDN	K1	3.3 V	Read strobe for slave FIFO
B1	FX2_SLWRN	J9	3.3 V	Write strobe for slave FIFO
B7	FX2_WAKEUP	—	3.3 V	USB 2.0 PHY wake signal
G2	USB_B2_CLK	E2	3.3 V	USB 2.0 PHY 48-MHz interface clock

FPGA Programming from Flash Memory

Flash memory programming is possible through a variety of methods. The default method is to use the factory design—Golden Hardware Reference Design. This design contains an on-board web server, which serves the Board Update Portal (BUP) web application. The web page allows you to link to SoC-related web pages and to control some user I/O and LCD on the development board.

On either power-up or by pressing the program configuration push button, PGM_CONFIG (S12), the MAX V CPLD 5M2210 System Controller's PFL configures the FPGA from the flash memory. The PFL megafunction reads 16-bit data from the flash memory and converts it to fast passive parallel (FPP) format. This 16-bit data is then written to the dedicated configuration pins in the FPGA during configuration.

Pressing the PGM_CONFIG push button (S12) loads the FPGA with a hardware page based on which PGM_LED[2:0] (D41, D42, D43) illuminates.

Table 2–5 lists the design that loads when you press the PGM_CONFIG push button.

Table 2–5. PGM_LED Settings *(1)*

PGM_LED0 (D43)	PGM_LED1 (D42)	PGM_LED2 (D41)	Design
ON	OFF	OFF	Factory hardware
OFF	ON	OFF	User hardware 1
OFF	OFF	ON	User hardware 2

Note to Table 2–5:

(1) ON indicates a setting of '0' while OFF indicates a setting of '1'.

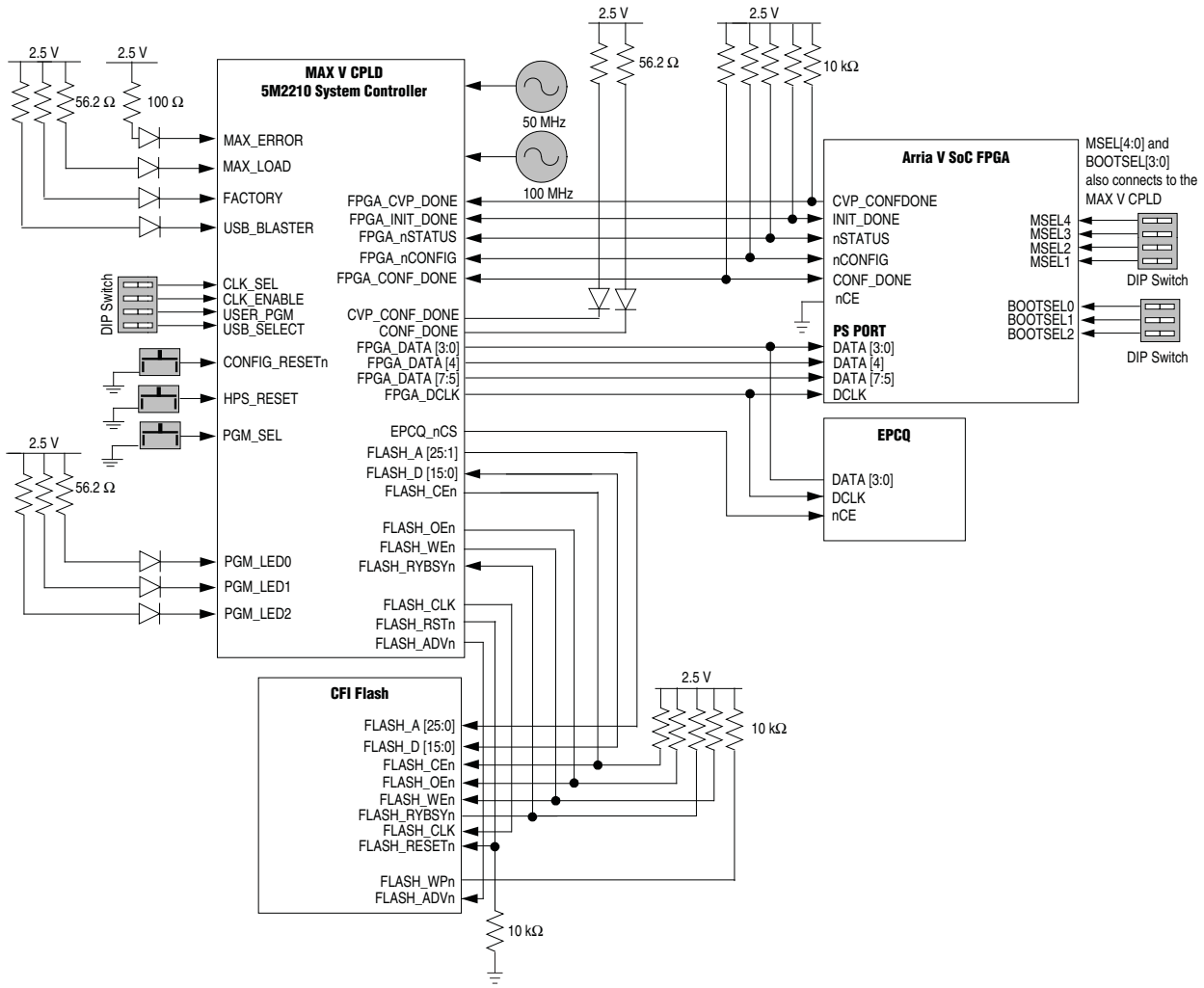
A EPCQ device is used for FPGA configuration in Active Serial (AS) mode on power-up. The EPCQ device with non-volatile memory features a simple six-pin interface and a small form factor. The EPCQ supports AS x1 and x4 modes.

By default, this board has a FPP configuration scheme setting. The MAX_AS_CONF pin needs to be driven from the MAX V CPLD to enable the bus switch to isolate the EPCQ flash (U28) from the configuration bus. This happens when the MSEL is 10010 or 10011.

In AS configuration scheme, the data is read from the EPCQ flash and directly sent to the FPGA. The MAX V CPLD 5M2210 System Controller controls the nCS line of the EPCQ to avoid line contention on the data line due to functionality sharing. In order to program non-volatile memory, CFI Flash or EPCQ special programming functionality design should be loaded into the FPGA or MAX V CPLD to allow programming using the Quartus II Programmer.

Figure 2–4 shows the PFL configuration.

Figure 2–4. PFL Configuration



For more information on the following topics, refer to the respective documents:

- Board Update Portal, PFL design, and flash memory map storage, refer to the *Arria V SoC Development Kit User Guide.*
- PFL megafunction, refer to *Parallel Flash Loader Megafunction User Guide.*

FPGA Programming over External USB-Blaster

The JTAG chain header provides another method for configuring the FPGA using an external USB-Blaster device with the Quartus II Programmer running on a PC. To prevent contention between the JTAG masters, the on-board USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain through the JTAG chain header.

Status Elements

The development board includes status LEDs. This section describes the status elements.

Table 2–6 lists the LED board references, names, and functional descriptions.

Table 2–6. Board-Specific LEDs

Board Reference	Schematic Signal Name	I/O Standard	Description
D37	Power	5.0 V	Blue LED. Illuminates when 5.0 V power is active.
D38	MAX_CONF_DONE	3.3 V	Green LED. Illuminates when the FPGA is successfully configured. Driven by the MAX V CPLD 5M2210 System Controller.
D39	MAX_ERROR	3.3 V	Red LED. Illuminates when the MAX V CPLD 5M2210 System Controller fails to configure the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D40	MAX_LOAD	3.3 V	Green LED. Illuminates when the MAX V CPLD 5M2210 System Controller is actively configuring the FPGA. Driven by the MAX V CPLD 5M2210 System Controller.
D43 D42 D41	PGM_LED[0] PGM_LED[1] PGM_LED[2]	3.3 V	Green LEDs. Illuminates to indicate which hardware page loads from flash memory when you press the PGM_SEL push button.
D20, D8	FMC_PRSNTn, FMCB_PRSNTn	2.5 V	Green LED. Illuminates when the FMC port has a board or cable plugged-in. Driven by the add-in card.
D35, D36 D34, D33	JTAG_RX, JTAG_TX SC_RX, SC_TX	1.8 V	Green LEDs. Illuminates to indicate USB-Blaster II receive and transmit activities.
D22, D21	UARTA_RX_LED, UARTA_TX_LED	3.3 V	Green LED. Illuminates to indicate UART port A receive and transmit activities.
D24, D23	UARTB_RX_LED, UARTB_TX_LED	3.3 V	Green LED. Illuminates to indicate UART port B receive and transmit activities.

Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- Board settings DIP switch
- JTAG chain control DIP switch
- FPGA configuration mode DIP switch
- HPS jumpers
- CPU reset push button
- MAX V reset push button
- Program configuration push button
- Program select push button

For more information about the default settings of the DIP switches, refer to the *Arria V SoC Development Kit User Guide.*

Board Settings DIP Switch

The board settings DIP switch (SW2) controls various features specific to the board and the MAX V CPLD 5M2210 System Controller logic design. Table 2–7 lists the switch controls and descriptions.

Table 2–7. Board Settings DIP Switch Controls

Switch	Schematic Signal Name	Description
1	CLK125A_EN	ON: Enable 125 MHz on-board oscillator OFF: Disable 125 MHz on-board oscillator
2	Si570_EN	ON: Disable programmable oscillator OFF: Enable programmable oscillator
3	FACTORY_LOAD	ON: Load the factory design from flash on power-up OFF: PFL disabled. Do not load any design from flash on power-up
4	SECURITY_MODE	ON: On-board USB-Blaster II sends FACTORY command on power-up OFF: On-board USB-Blaster II will not send FACTORY command on power-up

JTAG Chain Control DIP Switch

The JTAG chain control DIP switch (SW4) either removes or includes devices in the active JTAG chain. Table 2–8 lists the switch controls and its descriptions.

Table 2–8. JTAG Chain Control DIP Switch

Switch	Schematic Signal Name	Description
1	HPS_JTAG_EN	ON: Do not Include HPS in the JTAG chain. OFF: Include HPS in the JTAG chain.
2	FPGA_JTAG_EN	ON: Do not Include the FPGA in the JTAG chain. OFF: Include the FPGA in the JTAG chain.
3	FMC_JTAG_EN	ON: Do not include the FMCA connector in the JTAG chain. OFF: Include the FMCA connector in the JTAG chain.
4	MAX_JTAG_EN	ON: Do not include the MAX V system controller in the JTAG chain. OFF: Include the MAX V system controller in the JTAG chain.

FPGA Configuration Mode DIP Switch

The FPGA configuration mode DIP switch (SW3) defines the mode to use to configure the FPGA. Table 2–9 lists the switch controls and its descriptions. All switches at the ON position will select the default FPP x16 mode.

Table 2–9. FPGA Configuration Mode DIP Switch

Switch	Schematic Signal Name	Description
1	MSEL0	ON: Select logic 0 OFF: Select logic 1
2	MSEL1	ON: Select logic 0 OFF: Select logic 1
3	MSEL2	ON: Select logic 0 OFF: Select logic 1
4	MSEL3	ON: Select logic 0 OFF: Select logic 1
5	MSEL4	ON: Select logic 0 OFF: Select logic 1

HPS Jumpers

The HPS jumpers define the bootstrap options for the HPS—boot source, mode, HPS clocks settings, power-on-reset (POR) mode and peripherals selection. Table 2–10 lists the jumper settings and its descriptions.

Table 2–10. HPS Jumpers

Board Reference	Schematic Signal Name	Description
J39, J40, J41	HPS_BSEL[2:0] (BOOTSEL[2:0])	Selects the boot mode and source for the HPS. ■ 0x1—FPGA ■ 0x3—NAND flash (not supported on this board) ■ 0x5—Micro SD card ■ 0x7—QSPI flash All the other modes are reserved.
J37, J38	HPS_CSEL[1:0] (CLKSEL[1:0])	Selects the HPS clock settings. The actual clock settings are also dependent on the HPS_BSEL[2:0] selection.
J45, J46	OSC2_CLK_SEL[1:0]	Selects the source of OSC2 clock. ■ 00—Select on-board clock generator. ■ 01—Select external source via SMA connector. ■ 10—Select 33 MHz on-board oscillator
J19	JTAG_HPS_SEL	HPS in JTAG chain or only connect HPS to MICTOR. Selects the source to control the HPS. ■ ON: Select on-board USB-Blaster II as the JTAG master. ■ OFF: Select MICTOR-based JTAG master, such as DSTREAM or Lauterbach programming cables. Also, sets SW4.1 to ON to remove the on-board USB Blaster II from driving the HPS JTAG input port in this mode.
J21	JTAG_SEL	Selects the source of the JTAG chain. ■ ON: Select on-board USB-Blaster II as the source. ■ OFF: Select MICTOR as the source.

CPU Reset Push Button

The CPU reset push button, CPU_RESETn (S4), is an input to the Arria V HPS pin and is an open-drain I/O from the MAX V CPLD System Controller. This push button is the default reset for both the HPS and CPLD logic. The MAX V CPLD 5M2210 also drives this push button during POR mode.

MAX V Reset Push Button

The MAX V reset push button, MAX_RESETn (S11), is an input to the MAX V CPLD 5M2210 System Controller. This push button is the default reset for the CPLD logic.

Program Configuration Push Button

The program configuration push button, PGM_CONFIG (S12), is an input to the MAX V CPLD 5M2210 System Controller. This input forces a FPGA reconfiguration from the flash memory. The location in the flash memory is based on the settings of PGM_LED[2:0], which is controlled by the program select push button, PGM_SEL (S13). Valid settings include PGM_LED0, PGM_LED1, or PGM_LED2 on the three pages in flash memory reserved for FPGA designs.

Program Select Push Button

The program select push button, PGM_SEL (S13), is an input to the MAX V CPLD System Controller. This push button toggles the PGM_LED[2:0] sequence that selects which location in the flash memory is used to configure the FPGA. Refer to Table 2–5 on page 2–13 for the PGM_LED[2:0] sequence definitions.

General User Input/Output

This section describes the user I/O interface to the FPGA, including the push buttons, DIP switches, LEDs, expansion header, and character LCD.

User-Defined Push Buttons

The development board includes eight user-defined push buttons. For information about the system and safe reset push buttons, refer to "Setup Elements" on page 2–16.

Board references S1–S8 are push buttons for controlling the FPGA designs that loads into the Arria V SoC device. Push buttons S1–S4 connect to the FPGA while push buttons S5–S8 connect to the HPS. When you press and hold down the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–11 lists the user-defined push button schematic signal names and their corresponding Arria V SoC pin numbers.

Table 2–11. User-Defined Push Button Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard
S4	USER_PB_FPGA0	AT23	1.5 V
S3	USER_PB_FPGA1	AP24	1.5 V
S2	USER_PB_FPGA2	AW24	1.5 V
S1	USER_PB_FPGA3	AW23	1.5 V
S8	USER_PB_HPS0	E15	2.5 V
S7	USER_PB_HPS1	G16	2.5 V
S6	USER_PB_HPS2	E16	2.5 V
S5	USER_PB_HPS3	H16	2.5 V

User-Defined DIP Switch

Board reference SW1 is a eight-pin DIP switch. This switch is user-defined and provides additional FPGA or HPS input control. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected. There are no board-specific functions for this switch.

Table 2–12 lists the user-defined DIP switch schematic signal names and their corresponding Arria V SoC pin numbers.

Table 2–12. User-Defined DIP Switch Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard
1	USER_DIPSW_HPS0	L15	3.3 V
2	USER_DIPSW_HPS1	K15	3.3 V
3	USER_DIPSW_HPS2	K14	3.3 V
4	USER_DIPSW_HPS3	C15	3.3 V
5	USER_DIPSW_FPGA0	AL24	1.5 V
6	USER_DIPSW_FPGA1	AF24	1.5 V
7	USER_DIPSW_FPGA2	AE24	1.5 V
8	USER_DIPSW_FPGA3	AU23	1.5 V

User-Defined LEDs

Board references D1–D8 are eight user-defined LEDs. The status and debugging signals are driven to the LEDs from the FPGA or HPS designs loaded into the Arria V SoC. Driving a logic 0 on the I/O port turns the LED on while driving a logic 1 turns the LED off. There are no board-specific functions for these LEDs.

Table 2–13 lists the general LED schematic signal names and their corresponding Arria V SoC pin numbers.

Table 2–13. General LED Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard
D12	USER_LED_FPGA0	AH24	1.5 V
D11	USER_LED_FPGA1	AU24	1.5 V
D10	USER_LED_FPGA2	AT24	1.5 V
D9	USER_LED_FPGA3	AD24	1.5 V
D16	USER_LED_HPS0	R17	3.3 V
D15	USER_LED_HPS1	F16	3.3 V
D14	USER_LED_HPS2	R15	3.3 V
D13	USER_LED_HPS3	C16	3.3 V

Character LCD

The development board includes a single 10-pin 0.1" pitch single-row header that interfaces to a 2 line × 16 character Lumex character LCD using standard I²C interface connected to the HPS. The character LCD has a two headers that mount directly to the board's 10-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging, I²C expansion, or other purposes.

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.newhavendisplay.com.

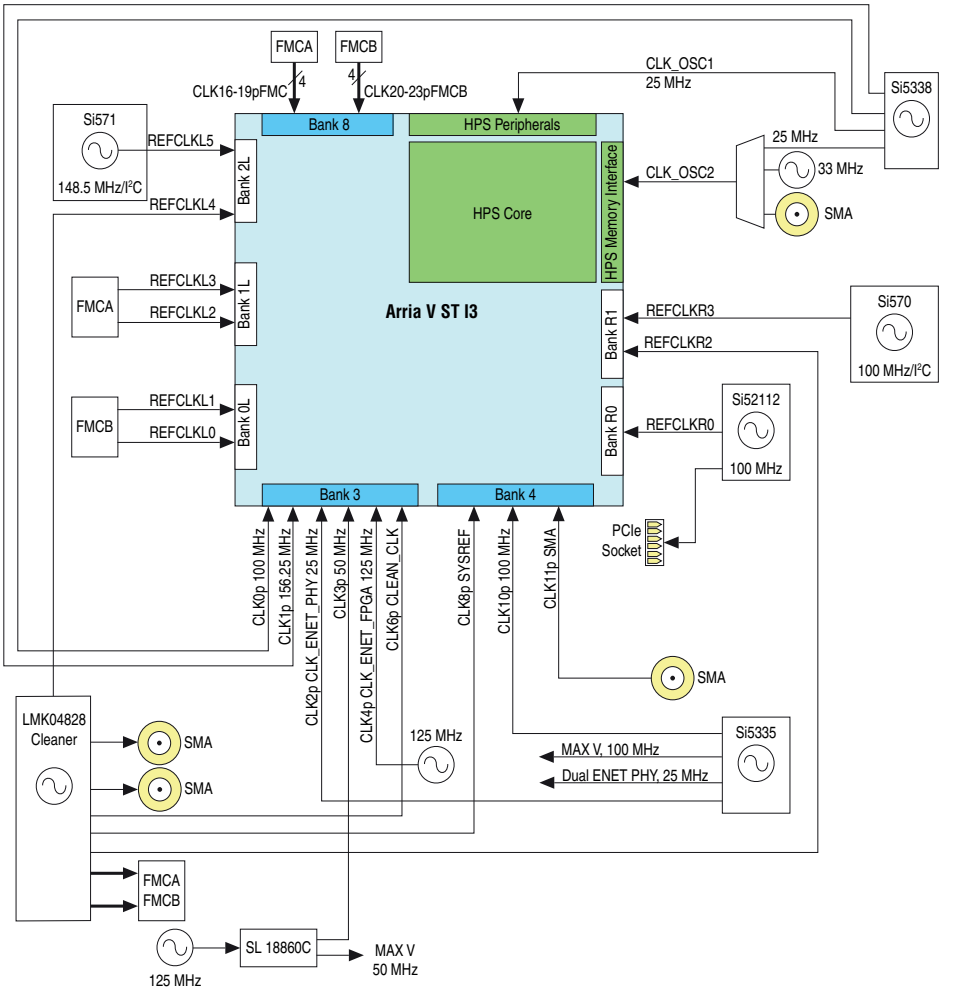
Clock Circuitry

This section describes the board's clock inputs and outputs.

On-Board Oscillators

Figure 2–5 shows the default frequencies of all external clocks going to the Arria V SoC development board.

Figure 2–5. Arria V SoC Development Board Clocks



Off-Board Input/Output Clock

The development board has input and output clocks which can be driven onto the board. The output clocks can be programmed to different levels and I/O standards according to the FPGA device's specification.

Table 2–14 lists the clock inputs for the development board.

Table 2–14. Off-Board Clock Inputs

Source	Schematic Signal Name	I/O Standard	Arria V SoC Pin Number	Description
SMA	SMA_CLKIN	2.5 V CMOS	—	Clock input to the global clock network.
SMA	OSC2_CLK_SMA	2.5 V CMOS	—	Multiplexed clock input to OSC2 of the HPS.
FMC Port A	FMC_CLK_M2C_P[1:0]	LVDS	A22, B22	LVDS input from the installed FMC card to global clock inputs.
	FMC_CLK_M2C_N[1:0]	LVDS	A21, C22	
FMC Port A	FMC_LA_RX_CLK_P	LVDS	H21	LVDS input from the installed FMC card to global clock inputs.
	FMC_LA_RX_CLK_N	LVDS	J21	
FMC Port A	FMC_LA_RX_P7	LVDS	C20	LVDS input from the installed FMC card to global clock inputs.
	FMC_LA_RX_N7	LVDS	D20	
FMC Port A	FMC_GBTCLK_M2C_P[1:0]	LVDS	AA31, AC31	LVDS input from the installed FMC card to dedicated reference clock inputs.
	FMC_GBTCLK_M2C_N[1:0]	LVDS	AA32, AC32	
FMC Port B	FMCB_CLK_M2C_P[1:0]	LVDS	C34, G34	LVDS input from the installed FMC card to global clock inputs.
	FMCB_CLK_M2C_N[1:0]	LVDS	D34, H34	
FMC Port B	FMCB_LA_RX_CLK_P	LVDS	E34	LVDS input from the installed FMC card to global clock inputs.
	FMCB_LA_RX_CLK_N	LVDS	F34	
FMC Port B	FMCB_LA_RX_P7	LVDS	N34	LVDS input from the installed FMC card to global clock inputs.
	FMCB_LA_RX_N7	LVDS	N33	
FMC Port B	FMCB_GBTCLK_M2C_P[1:0]	LVDS	AG32, AE31	LVDS input from the installed FMC card to dedicated reference clock inputs.
	FMCB_GBTCLK_M2C_N[1:0]	LVDS	AG33, AE32	

Table 2–15 lists the clock outputs for the development board.

Table 2–15. Off-Board Clock Outputs

Source	Schematic Signal Name	I/O Standard	Arria V SoC Pin Number	Description
FMC Port A	FMC_DEVCLK_P	LVDS	M23	LVDS output.
	FMC_DEVCLK_N	LVDS	N23	
FMC Port B	FMCB_DEVCLK_P	LVDS	L30	LVDS output.
	FMCB_DEVCLK_N	LVDS	M30	
PCI Express Socket	PCIE_REFCLK_SYN_P	HCSL	AF8	HCSL output to the PCI Express socket.
	PCIE_REFCLK_SYN_N	HCSL	AF7	

Components and Interfaces

This section describes the development board's communication ports and interface cards relative to the Arria V SoC device. The development board supports the following communication ports:

- PCI Express
- 10/100/1000 Ethernet (HPS)
- 10/100 Ethernet (FPGA)
- FMC
- RS-232 UART (HPS)
- Real-Time clock (HPS)
- SFP+
- I^2C interface

PCI Express

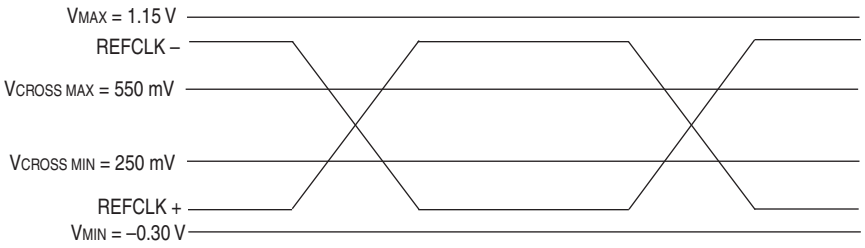
The PCI Express interface on the development board supports auto-negotiating channel width from ×1 to ×4 with the following connection speeds:

- Gen1 at 2.5 Gbps/lane for a maximum of 10 Gbps bandwidth
- Gen2 at 5 Gbps/lane for a maximum of 20 Gbps bandwidth

The `PCIE_REFCLK_P/N` signal is a 100-MHz differential input that is driven to the daughter card through the PCI Express edge connector. This signal connects directly to a Arria V SoC `REFCLK` input pin pair using DC coupling. The I/O standard is High-Speed Current Steering Logic (HCSL).

Figure 2–6 shows the PCI Express reference clock levels.

Figure 2–6. PCI Express Reference Clock Levels



The PCI Express edge connector also has a presence detect feature for the motherboard to determine if a card is installed. A jumper is provided to optionally connect `PRSNT1n` to any of the three `PRSNT2n` pins found within the x4 connector definition. This is to address issues on some PC systems that would base the link-width capability on the presence detect pins versus a query operation.

Table 2–16 summarizes the PCI Express pin assignments. The signal names and directions are relative to the Arria V SoC.

Table 2–16. PCI Express Pin Assignments, Schematic Signal Names, and Functions

Board Reference (J42)	Schematic Signal Name	I/O Standard	Arria V SoC Device Pin Number	Description
A11	PCIE_PERSTn	LVTTL	AK6	Reset
B17	PCIE_PRSNT2_X1	LVTTL	AC22	Presence detect DIP switch
B31	PCIE_PRSNT2_X4	LVTTL	AD21	Presence detect DIP switch
A14	PCIE_REFCLK_SYN_N	HCSL	AF7	Motherboard reference clock
A13	PCIE_REFCLK_SYN_P	HCSL	AF8	Motherboard reference clock
B5	PCIE_SMBCLK	LVTTL	AG20	SMB clock
B6	PCIE_SMBDAT	LVTTL	AG23	SMB data
B11	PCIE_WAKEn	LVTTL	AL6	Wake signal
A17	PCIE_RX_N0	1.5 V PCML	AU2	Receive bus
A22	PCIE_RX_N1	1.5 V PCML	AR2	Receive bus
A26	PCIE_RX_N2	1.5 V PCML	AN2	Receive bus
A30	PCIE_RX_N3	1.5 V PCML	AL2	Receive bus
A16	PCIE_RX_P0	1.5 V PCML	AU1	Receive bus
A21	PCIE_RX_P1	1.5 V PCML	AR1	Receive bus
A25	PCIE_RX_P2	1.5 V PCML	AN1	Receive bus
A29	PCIE_RX_P3	1.5 V PCML	AL1	Receive bus
B15	PCIE_TX_C_N0	1.5 V PCML	AT4	Transmit bus
B20	PCIE_TX_C_N1	1.5 V PCML	AP4	Transmit bus
B24	PCIE_TX_C_N2	1.5 V PCML	AM4	Transmit bus
B28	PCIE_TX_C_N3	1.5 V PCML	AK4	Transmit bus
B14	PCIE_TX_C_P0	1.5 V PCML	AT3	Transmit bus
B19	PCIE_TX_C_P1	1.5 V PCML	AP3	Transmit bus
B23	PCIE_TX_C_P2	1.5 V PCML	AM3	Transmit bus
B27	PCIE_TX_C_P3	1.5 V PCML	AK3	Transmit bus

10/100/1000 Ethernet (HPS)

The development board supports an RJ-45 10/100/1000 base-T Ethernet using an external Micrel KSZ9021RN PHY and the HPS EMAC function from the Altera Triple-Speed Ethernet MegaCore MAC function. The PHY-to-MAC interface employs RGMII connection using four data lines at 250 Mbps each for a connection speed of 1 Gbps.

The Micrel KSZ9021RN PHY uses 2.5 V or 3.3 V power rails. The PHY interfaces to an RJ-45 model with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–7 shows the RGMII interface between the HPS (MAC) and Micrel KSZ9021RN PHY.

Figure 2–7. RGMII Interface between HPS (MAC) and PHY

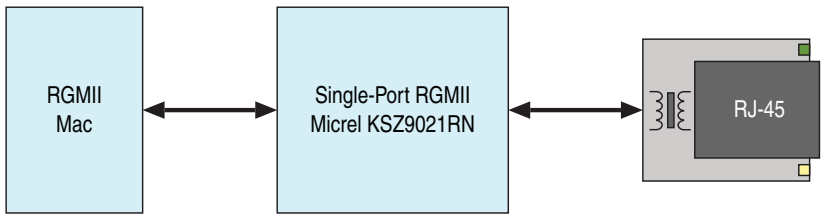


Table 2–17 lists the HPS Ethernet PHY interface pin assignments.

Table 2–17. Ethernet PHY (HPS) Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U7)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
41	CLK125_NDO_LED_MODE	—	—	Clock out 125-MHz LED mode
24	ENET_HPS_GTX_CLK	D19	3.3 V CMOS	125-MHz RGMII transmit clock
38	ENET_HPS_INTn	A18	3.3 V CMOS	Management bus interrupt
17	ENET_HPS_LED1_LINK	—	3.3 V CMOS	Receive data active LED
15	ENET_HPS_LED2_LINK	—	3.3 V CMOS	Transmit data active LED
36	ENET_HPS_MDC	L18	3.3 V CMOS	Management bus clock
37	ENET_HPS_MDIO	J18	3.3 V CMOS	Management bus data
42	ENET_HPS_RESETn	—	3.3 V CMOS	Device reset
48	ENET_HPS_RSET	—	3.3 V CMOS	PHY transmit output level set
35	ENET_HPS_RX_CLK	G21	3.3 V CMOS	RGMII receive clock
33	ENET_HPS_RX_DV	H19	3.3 V CMOS	RGMII receive data valid
32	ENET_HPS_RXD0	E19	3.3 V CMOS	RGMII receive data bus
31	ENET_HPS_RXD1	M17	3.3 V CMOS	RGMII receive data bus
28	ENET_HPS_RXD2	G20	3.3 V CMOS	RGMII receive data bus
27	ENET_HPS_RXD3	G19	3.3 V CMOS	RGMII receive data bus
25	ENET_HPS_TX_EN	N18	3.3 V CMOS	RGMII transmit enable
19	ENET_HPS_TXD0	H18	3.3 V CMOS	RGMII transmit data bus
20	ENET_HPS_TXD1	F19	3.3 V CMOS	RGMII transmit data bus

Table 2–17. Ethernet PHY (HPS) Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U7)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
21	ENET_HPS_TXD2	K18	3.3 V CMOS	RGMII transmit data bus
22	ENET_HPS_TXD3	M18	3.3 V CMOS	RGMII transmit data bus
3	MDI_HPS_N0	—	3.3 V CMOS	Media dependent interface
6	MDI_HPS_N1	—	3.3 V CMOS	Media dependent interface
8	MDI_HPS_N2	—	3.3 V CMOS	Media dependent interface
11	MDI_HPS_N3	—	3.3 V CMOS	Media dependent interface
2	MDI_HPS_P0	—	3.3 V CMOS	Media dependent interface
5	MDI_HPS_P1	—	3.3 V CMOS	Media dependent interface
7	MDI_HPS_P2	—	3.3 V CMOS	Media dependent interface
10	MDI_HPS_P3	—	3.3 V CMOS	Media dependent interface

The Micrel KSZ9021RN PHY uses a multi-level POR bootstrap encoding scheme to allow a small set of I/O pins (7) to set up a very large number of default settings within the device. The related I/O pins have integrated pull-up or pull-down resistors to configure the device. Table 2–18 lists the level encoding scheme.

Table 2–18. Ethernet PHY (HPS) Bootstrap Encoding Scheme

Board Reference (U7)	Schematic Signal Name	Description	Strapping Option
17	ENET_HPS_LED1_LINK	PHY address bit 0	Pulled low
15	ENET_HPS_LED2_LINK	PHY address bit 1	Pulled low
32	ENET_HPS_RXD0	Mode 0	Pulled high
31	ENET_HPS_RXD1	Mode 1	Pulled high
28	ENET_HPS_RXD2	Mode 2	Pulled high
27	ENET_HPS_RXD3	Mode 3	Pulled high
35	ENET_HPS_RX_CLK	PHY address bit 2	Pulled high
33	ENET_HPS_RX_DV	Clock enable	Pulled low
41	CLK125_NDO_LED_MODE	Single LED mode	Pulled high

10/100 Ethernet (FPGA)

The development board supports an RJ-45 10/100 base-T Ethernet using an external Renesas uPD60620 PHY. This PHY supports EtherCAT, Ethernet IRT and DLR features using a third party MAC IP. The PHY-to-MAC interface employs MII connection using four data lines at 25 Mbps each for a connection speed of 100 Mbps.

The PHY uses 3.3 V power rails and requires a 25 MHz reference clock to be driven from a dedicated oscillator. The PHY interfaces to a dual RJ-45 model with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–8 shows the MII interface between the FPGA (MAC) and Renesas uPD60620 PHY.

Figure 2–8. MII Interface between FPGA (MAC) and PHY

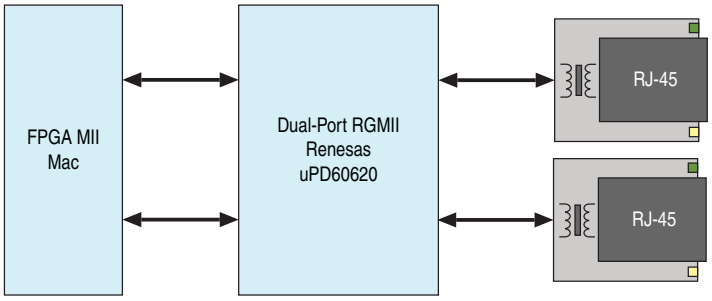


Table 2–19 lists the Ethernet PHY interface pin assignments.

Table 2–19. Ethernet PHY (FPGA) Pin Assignments, Signal Names and Functions (Part 1 of 2)

Board Reference (U55)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
68	ENET1_ACT_LED	—	2.5 V	PHY 1 active LED
69	ENET1_LINK_LED	—	2.5 V	PHY 1 link LED
18	ENET1_MDI_RX_N	—	2.5 V	Media dependent interface
17	ENET1_MDI_RX_P	—	2.5 V	Media dependent interface
16	ENET1_MDI_TX_N	—	2.5 V	Media dependent interface
15	ENET1_MDI_TX_P	—	2.5 V	Media dependent interface
59	ENET1_RX_CLK	AE22	2.5 V	MII receive clock
53	ENET1_RX_D0	AL23	2.5 V	MII receive data bus
54	ENET1_RX_D1	AW22	2.5 V	MII receive data bus
55	ENET1_RX_D2	AW21	2.5 V	MII receive data bus
56	ENET1_RX_D3	AV21	2.5 V	MII receive data bus
57	ENET1_RX_DV	AF22	2.5 V	MII receive data valid
58	ENET1_RX_ERROR	AH23	2.5 V	MII receive error
49	ENET1_TX_CLK_FB	AN23	2.5 V	25-MHz MII transmit clock
43	ENET1_TX_D0	AU22	2.5 V	MII transmit data bus
44	ENET1_TX_D1	AT22	2.5 V	MII transmit data bus
45	ENET1_TX_D2	AE23	2.5 V	MII transmit data bus
46	ENET1_TX_D3	AD22	2.5 V	MII transmit data bus
48	ENET1_TX_EN	AP23	2.5 V	MII transmit enable
65	ENET2_ACT_LED	—	2.5 V	PHY 2 active LED
67	ENET2_LINK_LED	—	2.5 V	PHY 2 link LED
4	ENET2_MDI_RX_N	—	2.5 V	Media dependent interface
5	ENET2_MDI_RX_P	—	2.5 V	Media dependent interface
6	ENET2_MDI_TX_N	—	2.5 V	Media dependent interface

Table 2–19. Ethernet PHY (FPGA) Pin Assignments, Signal Names and Functions (Part 2 of 2)

Board Reference (U55)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
7	ENET2_MDI_TX_P	—	2.5 V	Media dependent interface
41	ENET2_RX_CLK	AT20	2.5 V	MII receive clock
35	ENET2_RX_D0	AW19	2.5 V	MII receive data bus
36	ENET2_RX_D1	AL22	2.5 V	MII receive data bus
37	ENET2_RX_D2	AH22	2.5 V	MII receive data bus
38	ENET2_RX_D3	AU20	2.5 V	MII receive data bus
39	ENET2_RX_DV	AP20	2.5 V	MII receive data valid
40	ENET2_RX_ERROR	AN22	2.5 V	MII receive error
29	ENET2_TX_CLK_FB	AN21	2.5 V	25-MHz MII transmit clock
23	ENET2_TX_D0	AT21	2.5 V	MII transmit data bus
24	ENET2_TX_D1	AR21	2.5 V	MII transmit data bus
25	ENET2_TX_D2	AK21	2.5 V	MII transmit data bus
26	ENET2_TX_D3	AP22	2.5 V	MII transmit data bus
28	ENET2_TX_EN	AW20	2.5 V	MII transmit enable
1	ENET_DUAL_RESETn	AV22	2.5 V	Device reset
62	ENET_FPGA_MDC	AG22	2.5 V	Management bus clock
63	ENET_FPGA_MDIO	AK22	2.5 V	Management bus data

The PHY uses a multi-level POR bootstrap encoding scheme to allow a small set of I/O pins to set up a very large number of default settings within the device. The related I/O pins have integrated pull-up or pull-down resistors to configure the device. To change the configuration, connect an external resistor of maximum 5 kΩ to the pin. Table 2–20 lists the level encoding scheme.

Table 2–20. Ethernet PHY (FPGA) Bootstrap Encoding Scheme

Board Reference (U55)	Schematic Signal Name	Description	Strapping Option
36	ENET2_RX_D1	Auto-negotiation disabled. 100 base-T default.	Pulled low
35	ENET2_RX_D0	Full duplex operation	Pulled high
41	ENET2_RX_CLK	Disable quick auto negotiation	Pulled low
58	ENET1_RX_ERROR	MII mode operation	Pulled low
59	ENET1_RX_CLK	AUTOMDI-X enabled	Pulled high
39	ENET2_RX_DV	Transmit mode for PHY1	Pulled high
57	ENET1_RX_DV	Transmit mode for PHY0	Pulled high
53	ENET1_RX_D0	Address for Serial Management Interface (SMI)	Pulled low
54	ENET1_RX_D1	Address for SMI	Pulled low

FMC

The development board contains two high pin count (HPC) FPGA mezzanine card (FMC) ports that functions with a quadrature amplitude modulation (QAM) digital-to-analog converter (DAC) FMC module or daughter card. This pinout satisfies a QAM DAC that requires 58 LVDS data output pairs, one LVDS input clock pair, and three low-voltage differential signaling (LVDS) control pairs from the Arria V. These pins also have the option to be used as single-ended I/O pins. The VCCIO supply for FMC bank A in the low pin count (LPC) and HPC provide a variable voltage of 1.5 V, 1.8 V, 2.5 V (default), or 3.3 V. The VCCIO supply for FMC bank B in the HPC provides a variable voltage from 1.2 V to 3.3 V, which can be supplied by the FMC module. For device safety concerns, a jumper is available for you to connect this bank to the same VCCIO used for FMC bank A. This allows the VCCIO pins on the FPGA to be tied to a known power. The VCCIO pins also allows you the option to perform a manual check for the module's input voltage before connecting to the FPGA. This is to ensure that the module does not exceed the power supply maximum voltage rating.

Table 2–21 lists the FMC port A pin assignments, signal names, and functions.

Table 2–21. FMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference (J26)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
D1	FMC_C2M_PG	—	2.5 V CMOS	Power good output
H4	FMC_CLK_M2C_P0	B22	LVDS	Clock input 0
H5	FMC_CLK_M2C_N0	C22	LVDS	Clock input 0
G2	FMC_CLK_M2C_P1	A22	LVDS	Clock input 1
G3	FMC_CLK_M2C_N1	A21	LVDS	Clock input 1
C3	FMC_DP_C2M_N0	AE36	PCML	Transmit channel
A23	FMC_DP_C2M_N1	AA36	PCML	Transmit channel
A27	FMC_DP_C2M_N2	W36	PCML	Transmit channel
A31	FMC_DP_C2M_N3	R36	PCML	Transmit channel
A35	FMC_DP_C2M_N4	N36	PCML	Transmit channel
A39	FMC_DP_C2M_N5	J36	PCML	Transmit channel
B37	FMC_DP_C2M_N6	G36	PCML	Transmit channel
B33	FMC_DP_C2M_N7	C36	PCML	Transmit channel
C2	FMC_DP_C2M_P0	AE37	PCML	Transmit channel
A22	FMC_DP_C2M_P1	AA37	PCML	Transmit channel
A26	FMC_DP_C2M_P2	W37	PCML	Transmit channel
A30	FMC_DP_C2M_P3	R37	PCML	Transmit channel
A34	FMC_DP_C2M_P4	N37	PCML	Transmit channel
A38	FMC_DP_C2M_P5	J37	PCML	Transmit channel
B36	FMC_DP_C2M_P6	G37	PCML	Transmit channel
B32	FMC_DP_C2M_P7	C37	PCML	Transmit channel
C7	FMC_DP_M2C_N0	AF38	PCML	Receive channel
A3	FMC_DP_M2C_N1	AB38	PCML	Receive channel

Table 2–21. FMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference (J26)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
A7	FMC_DP_M2C_N2	Y38	PCML	Receive channel
A11	FMC_DP_M2C_N3	T38	PCML	Receive channel
A15	FMC_DP_M2C_N4	P38	PCML	Receive channel
A19	FMC_DP_M2C_N5	K38	PCML	Receive channel
B17	FMC_DP_M2C_N6	H38	PCML	Receive channel
B13	FMC_DP_M2C_N7	D38	PCML	Receive channel
C6	FMC_DP_M2C_P0	AF39	PCML	Receive channel
A2	FMC_DP_M2C_P1	AB39	PCML	Receive channel
A6	FMC_DP_M2C_P2	Y39	PCML	Receive channel
A10	FMC_DP_M2C_P3	T39	PCML	Receive channel
A14	FMC_DP_M2C_P4	P39	PCML	Receive channel
A18	FMC_DP_M2C_P5	K39	PCML	Receive channel
B16	FMC_DP_M2C_P6	H39	PCML	Receive channel
B12	FMC_DP_M2C_P7	D39	PCML	Receive channel
C34	FMC_GA0	C23	2.5 V CMOS	FMC geographical address 0
D35	FMC_GA1	P25	2.5 V CMOS	FMC geographical address 1
D4	FMC_GBTCLK_M2C_P0	AC31	LVDS	Transceiver reference clock 0
D5	FMC_GBTCLK_M2C_N0	AC32	LVDS	Transceiver reference clock 0
B20	FMC_GBTCLK_M2C_P1	AA31	LVDS	Transceiver reference clock 1
B21	FMC_GBTCLK_M2C_N1	AA32	LVDS	Transceiver reference clock 1
E18	FMC_GPIO0	B24	2.5 V CMOS	FMC general purpose IO bit 0 (part of the partially populated HPS connector signal group)
E19	FMC_GPIO1	C24	2.5 V CMOS	FMC general purpose IO bit 1 (part of the partially populated HPS connector signal group)
K19	FMC_GPIO2	F24	2.5 V CMOS	FMC general purpose IO bit 2 (part of the partially populated HPS connector signal group)
K20	FMC_GPIO3	G24	2.5 V CMOS	FMC general purpose IO bit 3 (part of the partially populated HPS connector signal group)
J21	FMC_GPIO4	H24	2.5 V CMOS	FMC general purpose IO bit 4 (part of the partially populated HPS connector signal group)
J22	FMC_GPIO5	J24	2.5 V CMOS	FMC general purpose IO bit 5 (part of the partially populated HPS connector signal group)
K22	FMC_GPIO6	B27	2.5 V CMOS	FMC general purpose IO bit 6 (part of the partially populated HPS connector signal group)
K23	FMC_GPIO7	C27	2.5 V CMOS	FMC general purpose IO bit 7 (part of the partially populated HPS connector signal group)
D30	FMC_JTAG_TDI	—	2.5 V CMOS	JTAG data in
D31	FMC_JTAG_TDO	—	2.5 V CMOS	JTAG data out
D33	FMC_JTAG_TMS	—	2.5 V CMOS	JTAG mode select
D34	FMC_JTAG_RST	—	2.5 V CMOS	JTAG mode reset

Table 2–21. FMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference (J26)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
G6	FMC_LA_RX_CLK_P	H21	LVDS	Secondary carrier-bound clock
G7	FMC_LA_RX_CLK_N	J21	LVDS	Secondary carrier-bound clock
G10	FMC_LA_RX_N0	T28	2.5 V CMOS	FMC data bus
C11	FMC_LA_RX_N1	R27	2.5 V CMOS	FMC data bus
F11	FMC_LA_RX_N2	N27	2.5 V CMOS	FMC data bus
C15	FMC_LA_RX_N3	N26	2.5 V CMOS	FMC data bus
G16	FMC_LA_RX_N4	D26	2.5 V CMOS	FMC data bus
C19	FMC_LA_RX_N5	T27	2.5 V CMOS	FMC data bus
G19	FMC_LA_RX_N6	G26	2.5 V CMOS	FMC data bus
D21	FMC_LA_RX_N7	D20	2.5 V CMOS	FMC data bus
G22	FMC_LA_RX_N8	F22	2.5 V CMOS	FMC data bus
G25	FMC_LA_RX_N9	P22	2.5 V CMOS	FMC data bus
G28	FMC_LA_RX_N10	B25	2.5 V CMOS	FMC data bus
D24	FMC_LA_RX_N11	T25	2.5 V CMOS	FMC data bus
G31	FMC_LA_RX_N12	P24	2.5 V CMOS	FMC data bus
G34	FMC_LA_RX_N13	E25	2.5 V CMOS	FMC data bus
G37	FMC_LA_RX_N14	E24	2.5 V CMOS	FMC data bus
F20	FMC_LA_RX_N15	G23	2.5 V CMOS	FMC data bus
G9	FMC_LA_RX_P0	R28	2.5 V CMOS	FMC data bus
C10	FMC_LA_RX_P1	P27	2.5 V CMOS	FMC data bus
F10	FMC_LA_RX_P2	M27	2.5 V CMOS	FMC data bus
C14	FMC_LA_RX_P3	M26	2.5 V CMOS	FMC data bus
G15	FMC_LA_RX_P4	C26	2.5 V CMOS	FMC data bus
C18	FMC_LA_RX_P5	R26	2.5 V CMOS	FMC data bus
G18	FMC_LA_RX_P6	F26	2.5 V CMOS	FMC data bus
D20	FMC_LA_RX_P7	C20	2.5 V CMOS	FMC data bus
G21	FMC_LA_RX_P8	E22	2.5 V CMOS	FMC data bus
G24	FMC_LA_RX_P9	N22	2.5 V CMOS	FMC data bus
G27	FMC_LA_RX_P10	A25	2.5 V CMOS	FMC data bus
D23	FMC_LA_RX_P11	T26	2.5 V CMOS	FMC data bus
G30	FMC_LA_RX_P12	N24	2.5 V CMOS	FMC data bus
G33	FMC_LA_RX_P13	D25	2.5 V CMOS	FMC data bus
G36	FMC_LA_RX_P14	D24	2.5 V CMOS	FMC data bus
F19	FMC_LA_RX_P15	F23	2.5 V CMOS	FMC data bus
D8	FMC_DEVCLK_P	M23	2.5 V CMOS	Mezzanine-bound clock
D9	FMC_DEVCLK_N	N23	2.5 V CMOS	Mezzanine-bound clock
H8	FMC_LA_TX_N0	J27	2.5 V CMOS	FMC data bus
H11	FMC_LA_TX_N1	K26	2.5 V CMOS	FMC data bus

Table 2–21. FMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference (J26)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
D12	FMC_LA_TX_N2	F27	2.5 V CMOS	FMC data bus
H14	FMC_LA_TX_N3	P28	2.5 V CMOS	FMC data bus
D15	FMC_LA_TX_N4	A27	2.5 V CMOS	FMC data bus
H17	FMC_LA_TX_N5	N25	2.5 V CMOS	FMC data bus
D18	FMC_LA_TX_N6	L27	2.5 V CMOS	FMC data bus
H20	FMC_LA_TX_N7	P21	2.5 V CMOS	FMC data bus
H23	FMC_LA_TX_N9	T21	2.5 V CMOS	FMC data bus
H26	FMC_LA_TX_N10	A24	2.5 V CMOS	FMC data bus
H29	FMC_LA_TX_N12	T22	2.5 V CMOS	FMC data bus
D27	FMC_LA_TX_N13	L24	2.5 V CMOS	FMC data bus
H35	FMC_LA_TX_N14	H25	2.5 V CMOS	FMC data bus
H38	FMC_LA_TX_N15	T24	2.5 V CMOS	FMC data bus
G13	FMC_LA_TX_N16	T23	2.5 V CMOS	FMC data bus
H32	FMC_LA_TX_N17	K23	2.5 V CMOS	FMC data bus
H7	FMC_LA_TX_P0	H27	2.5 V CMOS	FMC data bus
H10	FMC_LA_TX_P1	J26	2.5 V CMOS	FMC data bus
D11	FMC_LA_TX_P2	E27	2.5 V CMOS	FMC data bus
H13	FMC_LA_TX_P3	N28	2.5 V CMOS	FMC data bus
D14	FMC_LA_TX_P4	A26	2.5 V CMOS	FMC data bus
H16	FMC_LA_TX_P5	M25	2.5 V CMOS	FMC data bus
D17	FMC_LA_TX_P6	K27	2.5 V CMOS	FMC data bus
H19	FMC_LA_TX_P7	N21	2.5 V CMOS	FMC data bus
H22	FMC_LA_TX_P9	R21	2.5 V CMOS	FMC data bus
H25	FMC_LA_TX_P10	A23	2.5 V CMOS	FMC data bus
H28	FMC_LA_TX_P12	R22	2.5 V CMOS	FMC data bus
D26	FMC_LA_TX_P13	K24	2.5 V CMOS	FMC data bus
H34	FMC_LA_TX_P14	G25	2.5 V CMOS	FMC data bus
H37	FMC_LA_TX_P15	R24	2.5 V CMOS	FMC data bus
G12	FMC_LA_TX_P16	R23	2.5 V CMOS	FMC data bus
H31	FMC_LA_TX_P17	J23	2.5 V CMOS	FMC data bus
F1	FMC_M2C_PG	—	2.5 V CMOS	Power good input
H2	FMC_PRSNTn	K25	2.5 V CMOS	FMC module present
C30	FMC_SCL	J22	2.5 V CMOS	Management serial clock line
C31	FMC_SDA	D23	2.5 V CMOS	Management serial data line
D29	JTAG_MUX_TCK	AV34	2.5 V CMOS	JTAG chain clock
C23	LMK_CLK_FMC_N	—	2.5 V CMOS	Alternate mezzanine-bound clock (from LMK device)
C22	LMK_CLK_FMC_P	—	2.5 V CMOS	Alternate mezzanine-bound clock (from LMK device)

Table 2–21. FMC Port A Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference (J26)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
C27	LMK_SYSREF_FMC_N	—	2.5 V CMOS	Alternate mezzanine-bound SYSREF signal (from LMK device)
C26	LMK_SYSREF_FMC_P	—	2.5 V CMOS	Alternate mezzanine-bound SYSREF signal (from LMK device)

Table 2–22 lists the FMC port B pin assignments, signal names, and functions.

Table 2–22. FMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 4)

Board Reference (J4)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
D1	FMCB_C2M_PG	—	2.5 V CMOS	Power good output
H4	FMCB_CLK_M2C_P0	C34	LVDS	Clock input 0
H5	FMCB_CLK_M2C_N0	D34	LVDS	Clock input 0
G2	FMCB_CLK_M2C_P1	G34	LVDS	Clock input 1
G3	FMCB_CLK_M2C_N1	H34	LVDS	Clock input 1
C3	FMCB_DP_C2M_N0	AU36	PCML	Transmit channel
A23	FMCB_DP_C2M_N1	AN36	PCML	Transmit channel
A27	FMCB_DP_C2M_N2	AL36	PCML	Transmit channel
A31	FMCB_DP_C2M_N3	AG36	PCML	Transmit channel
C2	FMCB_DP_C2M_P0	AU37	PCML	Transmit channel
A22	FMCB_DP_C2M_P1	AN37	PCML	Transmit channel
A26	FMCB_DP_C2M_P2	AL37	PCML	Transmit channel
A30	FMCB_DP_C2M_P3	AG37	PCML	Transmit channel
C7	FMCB_DP_M2C_N0	AW36	PCML	Receive channel
A3	FMCB_DP_M2C_N1	AP38	PCML	Receive channel
A7	FMCB_DP_M2C_N2	AM38	PCML	Receive channel
A11	FMCB_DP_M2C_N3	AH38	PCML	Receive channel
C6	FMCB_DP_M2C_P0	AW37	PCML	Receive channel
A2	FMCB_DP_M2C_P1	AP39	PCML	Receive channel
A6	FMCB_DP_M2C_P2	AM39	PCML	Receive channel
A10	FMCB_DP_M2C_P3	AH39	PCML	Receive channel
C34	FMCB_GA0	J33	2.5 V CMOS	FMC geographical address 0
D35	FMCB_GA1	R30	2.5 V CMOS	FMC geographical address 1
D4	FMCB_GBTCLK_M2C_P0	AG32	LVDS	Transceiver reference clock 0
D5	FMCB_GBTCLK_M2C_N0	AG33	LVDS	Transceiver reference clock 0
B20	FMCB_GBTCLK_M2C_P1	AE31	LVDS	Transceiver reference clock 1
B21	FMCB_GBTCLK_M2C_N1	AE32	LVDS	Transceiver reference clock 1
E18	FMCB_GPIO0	F32	2.5 V CMOS	FMC general purpose IO bit 0 (part of the partially populated HPS connector signal group)

Table 2–22. FMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 4)

Board Reference (J4)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
E19	FMCB_GPIO1	G32	2.5 V CMOS	FMC general purpose IO bit 1 (part of the partially populated HPS connector signal group)
K19	FMCB_GPIO2	U19	2.5 V CMOS	FMC general purpose IO bit 2 (part of the partially populated HPS connector signal group)
K20	FMCB_GPIO3	U20	2.5 V CMOS	FMC general purpose IO bit 3 (part of the partially populated HPS connector signal group)
J21	FMCB_GPIO4	P20	2.5 V CMOS	FMC general purpose IO bit 4 (part of the partially populated HPS connector signal group)
J22	FMCB_GPIO5	R20	2.5 V CMOS	FMC general purpose IO bit 5 (part of the partially populated HPS connector signal group)
K22	FMCB_GPIO6	L20	2.5 V CMOS	FMC general purpose IO bit 6 (part of the partially populated HPS connector signal group)
K23	FMCB_GPIO7	M20	2.5 V CMOS	FMC general purpose IO bit 7 (part of the partially populated HPS connector signal group)
D30	FMCB_JTAG_TDI	—	2.5 V CMOS	JTAG data in
D31	FMCB_JTAG_TDO	—	2.5 V CMOS	JTAG data out
D33	FMCB_JTAG_TMS	—	2.5 V CMOS	JTAG mode select
D34	FMCB_JTAG_RST	—	2.5 V CMOS	JTAG mode reset
G6	FMCB_LA_RX_CLK_P	E34	LVDS	Secondary carrier-bound clock
G7	FMCB_LA_RX_CLK_N	F34	LVDS	Secondary carrier-bound clock
G31	FMCB_LA_RX_N0	A30	2.5 V CMOS	FMC data bus
G25	FMCB_LA_RX_N1	B33	2.5 V CMOS	FMC data bus
G22	FMCB_LA_RX_N2	D31	2.5 V CMOS	FMC data bus
F11	FMCB_LA_RX_N3	P31	2.5 V CMOS	FMC data bus
G19	FMCB_LA_RX_N4	N32	2.5 V CMOS	FMC data bus
D24	FMCB_LA_RX_N5	C30	2.5 V CMOS	FMC data bus
G16	FMCB_LA_RX_N6	M33	2.5 V CMOS	FMC data bus
C15	FMCB_LA_RX_N7	N33	2.5 V CMOS	FMC data bus
C11	FMCB_LA_RX_N8	P30	2.5 V CMOS	FMC data bus
G34	FMCB_LA_RX_N9	C29	2.5 V CMOS	FMC data bus
G37	FMCB_LA_RX_N10	A28	2.5 V CMOS	FMC data bus
D21	FMCB_LA_RX_N11	D29	2.5 V CMOS	FMC data bus
G10	FMCB_LA_RX_N12	T29	2.5 V CMOS	FMC data bus
G28	FMCB_LA_RX_N13	A35	2.5 V CMOS	FMC data bus
F20	FMCB_LA_RX_N14	D28	2.5 V CMOS	FMC data bus
C19	FMCB_LA_RX_N15	N29	2.5 V CMOS	FMC data bus
G30	FMCB_LA_RX_P0	B31	2.5 V CMOS	FMC data bus
G24	FMCB_LA_RX_P1	A33	2.5 V CMOS	FMC data bus
G21	FMCB_LA_RX_P2	C31	2.5 V CMOS	FMC data bus
F10	FMCB_LA_RX_P3	N31	2.5 V CMOS	FMC data bus

Table 2–22. FMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 4)

Board Reference (J4)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
G18	FMCB_LA_RX_P4	M32	2.5 V CMOS	FMC data bus
D23	FMCB_LA_RX_P5	B30	2.5 V CMOS	FMC data bus
G15	FMCB_LA_RX_P6	L33	2.5 V CMOS	FMC data bus
C14	FMCB_LA_RX_P7	N34	2.5 V CMOS	FMC data bus
C10	FMCB_LA_RX_P8	N30	2.5 V CMOS	FMC data bus
G33	FMCB_LA_RX_P9	B28	2.5 V CMOS	FMC data bus
G36	FMCB_LA_RX_P10	A29	2.5 V CMOS	FMC data bus
D20	FMCB_LA_RX_P11	D30	2.5 V CMOS	FMC data bus
G9	FMCB_LA_RX_P12	R29	2.5 V CMOS	FMC data bus
G27	FMCB_LA_RX_P13	B34	2.5 V CMOS	FMC data bus
F19	FMCB_LA_RX_P14	C28	2.5 V CMOS	FMC data bus
C18	FMCB_LA_RX_P15	M29	2.5 V CMOS	FMC data bus
D8	FMCB_DEVCLK_P	L30	2.5 V CMOS	Mezzanine-bound clock
D9	FMCB_DEVCLK_N	M30	2.5 V CMOS	Mezzanine-bound clock
D15	FMCB_LA_TX_N0	A32	2.5 V CMOS	FMC data bus
H23	FMCB_LA_TX_N1	J31	2.5 V CMOS	FMC data bus
H38	FMCB_LA_TX_N2	D32	2.5 V CMOS	FMC data bus
H20	FMCB_LA_TX_N3	K32	2.5 V CMOS	FMC data bus
H17	FMCB_LA_TX_N4	K34	2.5 V CMOS	FMC data bus
H32	FMCB_LA_TX_N5	F31	2.5 V CMOS	FMC data bus
G13	FMCB_LA_TX_N6	M34	2.5 V CMOS	FMC data bus
H11	FMCB_LA_TX_N7	M31	2.5 V CMOS	FMC data bus
H29	FMCB_LA_TX_N9	F33	2.5 V CMOS	FMC data bus
H14	FMCB_LA_TX_N10	K30	2.5 V CMOS	FMC data bus
H26	FMCB_LA_TX_N12	G30	2.5 V CMOS	FMC data bus
D12	FMCB_LA_TX_N13	J28	2.5 V CMOS	FMC data bus
D27	FMCB_LA_TX_N14	G28	2.5 V CMOS	FMC data bus
D18	FMCB_LA_TX_N15	G29	2.5 V CMOS	FMC data bus
H8	FMCB_LA_TX_N16	K29	2.5 V CMOS	FMC data bus
H35	FMCB_LA_TX_N17	D33	2.5 V CMOS	FMC data bus
D14	FMCB_LA_TX_P0	A31	2.5 V CMOS	FMC data bus
H22	FMCB_LA_TX_P1	H31	2.5 V CMOS	FMC data bus
H37	FMCB_LA_TX_P2	C32	2.5 V CMOS	FMC data bus
H19	FMCB_LA_TX_P3	J32	2.5 V CMOS	FMC data bus
H16	FMCB_LA_TX_P4	J34	2.5 V CMOS	FMC data bus
H31	FMCB_LA_TX_P5	E31	2.5 V CMOS	FMC data bus
G12	FMCB_LA_TX_P6	L34	2.5 V CMOS	FMC data bus
H10	FMCB_LA_TX_P7	L31	2.5 V CMOS	FMC data bus

Table 2–22. FMC Port B Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 4)

Board Reference (J4)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
H28	FMCB_LA_TX_P9	E33	2.5 V CMOS	FMC data bus
H13	FMCB_LA_TX_P10	J30	2.5 V CMOS	FMC data bus
H25	FMCB_LA_TX_P12	F30	2.5 V CMOS	FMC data bus
D11	FMCB_LA_TX_P13	H28	2.5 V CMOS	FMC data bus
D26	FMCB_LA_TX_P14	F28	2.5 V CMOS	FMC data bus
D17	FMCB_LA_TX_P15	F29	2.5 V CMOS	FMC data bus
H7	FMCB_LA_TX_P16	J29	2.5 V CMOS	FMC data bus
H34	FMCB_LA_TX_P17	C33	2.5 V CMOS	FMC data bus
F1	FMCB_M2C_PG	—	2.5 V CMOS	Power good input
H2	FMCB_PRSNTn	L19	2.5 V CMOS	FMC module present
C30	FMCB_SCL	N19	2.5 V CMOS	Management serial clock line
C31	FMCB_SDA	M19	2.5 V CMOS	Management serial data line
D29	JTAG_MUX_TCK	AV34	2.5 V CMOS	JTAG chain clock
C23	LMK_CLK_FMCB_N	—	2.5 V CMOS	Alternate mezzanine-bound clock (from LMK device)
C22	LMK_CLK_FMCB_P	—	2.5 V CMOS	Alternate mezzanine-bound clock (from LMK device)
C27	LMK_SYSREF_FMCB_N	—	2.5 V CMOS	Alternate mezzanine-bound SYSREF signal (from LMK device)
C26	LMK_SYSREF_FMCB_P	—	2.5 V CMOS	Alternate mezzanine-bound SYSREF signal (from LMK device)

RS-232 UART (HPS)

The development board supports two UART interfaces that connect to a mini-USB connector (J27) using a FT232RQ-REEL USB-to-UART bridge. The maximum supported rate for this interface is 1 Mbps. Board reference D21–D24 are the UART LEDs that illuminate to indicate TX and RX activity.

Table 2–23 lists the RS-232 UART pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–23. RS-232 UART Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
UART Port A (U25)				
2	UARTA_TX	M13	3.3 V	Transmit data
30	UARTA_RX	M12	3.3 V	Receive data
18	RESET_HPS_UARTA_N	—	3.3 V	Reset
11	POWER_ENA	—	3.3 V	Power
UART Port B (U36)				
2	UARTB_TX	N13	3.3 V	Transmit data
30	UARTB_RX	G13	3.3 V	Receive data

Table 2–23. RS-232 UART Schematic Signal Names and Functions

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
18	RESET_HPS_UARTB_N	—	3.3 V	Reset
11	POWER_ENB	—	3.3 V	Power

Real-Time Clock (HPS)

The HPS system has a battery-backed real-time clock (RTC) connected through the I^2C interface. The RTC is implemented using a DS1339 device from Maxim Semiconductor. The device has a built-in power sense circuit that detects power failures and automatically switches to backup battery supply, maintaining time. The device uses an SR44 lithium coin battery with a nominal voltage of 3 V. Using typical current capacity, the RTC is expected to have 120,000 backup hours. The battery is mounted inside a holder attached to the board to allow battery replacement or removal.

Table 2–24 lists the RTC device pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–24. RTC Device Schematic Signal Names and Functions

Board Reference (U11)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
16	I2C_SDA_HPS	C13	3.3 V	Management serial data
1	I2C_SCL_HPS	L13	3.3 V	Management serial clock

SFP+

The development board include two SFP+ ports that uses two transceiver channels from the FPGA. These ports takes in serial data from the FPGA and transform them into optical signals. Both SFP+ ports are active and include the SFP+ cage assembly.

Table 2–25 list the SFP+ ports interface pin assignments, signal names, and functions.

Table 2–25. SFP+ Ports Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
SFP+ Port A (J44)				
6	SFPA_MOD0_PRSNTn	AR9	2.5 V	Module present indicator
8	SFPA_LOS	AV7	2.5 V	Signal present indicator
2	SFPA_TXFAULT	AL9	2.5 V	Transmitter fault indicator
12	SFPA_RX_N	AE2	PCML	Receiver data
13	SFPA_RX_P	AE1	PCML	Receiver data
5	SFPA_MOD1_SCL	AT8	2.5 V	Serial 2-wire clock
4	SFPA_MOD1_SDA	AH8	2.5 V	Serial 2-wire data
3	SFPA_TXDISABLE	AP7	2.5 V	Drive low to disable transmitter
19	SFPA_TX_N	AD4	PCML	Transmitter data

Table 2–25. SFP+ Ports Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
18	SFPA_TX_P	AD3	PCML	Transmitter data
7	SFPA_RATESEL0	AU6	2.5 V	Rate select
9	SFPA_RATESEL1	AL8	2.5 V	Rate select
SFP+ Port B (J43)				
6	SFPB_MOD0_PRSNTn	AP8	2.5 V	Module present indicator
8	SFPB_LOS	AG21	2.5 V	Signal present indicator
2	SFPB_TXFAULT	AK20	2.5 V	Transmitter fault indicator
12	SFPB_RX_N	AA2	PCML	Receiver data
13	SFPB_RX_P	AA1	PCML	Receiver data
5	SFPB_MOD1_SCL	AN8	2.5 V	Serial 2-wire clock
4	SFPB_MOD1_SDA	AJ7	2.5 V	Serial 2-wire data
3	SFPB_TXDISABLE	AT6	2.5 V	Drive low to disable transmitter
19	SFPB_TX_N	Y4	PCML	Transmitter data
18	SFPB_TX_P	Y3	PCML	Transmitter data
7	SFPB_RATESEL0	AK8	2.5 V	Rate select
9	SFPB_RATESEL1	AN7	2.5 V	Rate select

I²C Interface

The HPS system has one I²C interface for communicating with the on-board and external components using a data rate of 400 Kbps.

Table 2–26 lists the I²C interface address map.

Table 2–26. I²C interface address map

Address	Device
0x68	Real-time clock
0x50	LCD
0x51	EEPROM
0x5C	HPS power monitor
0x5E	FPGA power monitor 1
0x62	FPGA power monitor 2
0x55	Si571 programmable oscillator
0x66	Si570 programmable oscillator
0x70	Si5338 quad-programmable clock

Memory

This section describes the development board's memory interface support and also their signal names, types, and connectivity relative to the Arria V SoC. The development board has the following memory interfaces:

- DDR3 SDRAM (FPGA)
- DDR3 SDRAM (HPS)
- QSPI flash (HPS)
- EPCQ flash
- Synchronous flash
- Micro SD flash memory
- I^2C EEPROM

For more information about the memory interfaces, refer to the following documents:

- *Timing Analysis* section in the External Memory Interface Handbook.
- *DDR, DDR2, and DDR3 SDRAM Design Tutorials* section in the External Memory Interface Handbook.

DDR3 SDRAM (FPGA)

The development board supports two 32Mx16x8 DDR3 SDRAM interface for very high-speed sequential memory access. The 32-bit data bus comprises of two ×16 devices with a single address or command bus. This interface connects to the dedicated HMC I/O banks on the bottom edge of the FPGA.

The DDR3 device shipped with this board are running at 533 MHz, for a total theoretical bandwidth of over 25.6 Gbps. The speed grade of this DDR3 device is 800 MHz with a CAS latency of 9.

Table 2–27 lists the DDR3 SDRAM pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
DDR3 x32 (U37)				
N3	DDR3A_A0	AU29	1.5 V SSTL Class I	Address bus
P7	DDR3A_A1	AT29	1.5 V SSTL Class I	Address bus
P3	DDR3A_A2	AV30	1.5 V SSTL Class I	Address bus
N2	DDR3A_A3	AU30	1.5 V SSTL Class I	Address bus
P8	DDR3A_A4	AT30	1.5 V SSTL Class I	Address bus
P2	DDR3A_A5	AR30	1.5 V SSTL Class I	Address bus
R8	DDR3A_A6	AL30	1.5 V SSTL Class I	Address bus
R2	DDR3A_A7	AK30	1.5 V SSTL Class I	Address bus

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
T8	DDR3A_A8	AW31	1.5 V SSTL Class I	Address bus
R3	DDR3A_A9	AW30	1.5 V SSTL Class I	Address bus
L7	DDR3A_A10	AV31	1.5 V SSTL Class I	Address bus
R7	DDR3A_A11	AU31	1.5 V SSTL Class I	Address bus
N7	DDR3A_A12	AH30	1.5 V SSTL Class I	Address bus
T3	DDR3A_A13	AG30	1.5 V SSTL Class I	Address bus
T7	DDR3A_A14	AE29	1.5 V SSTL Class I	Address bus
M2	DDR3A_BA0	AT31	1.5 V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AR31	1.5 V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AP31	1.5 V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AW32	1.5 V SSTL Class I	Column address select
K9	DDR3A_CKE	AP30	1.5 V SSTL Class I	Clock enable
J7	DDR3A_CLK_P	AP29	Differential 1.5 V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AN29	Differential 1.5 V SSTL Class I	Differential output clock
L2	DDR3A_CSN	AP32	1.5 V SSTL Class I	Chip select
E7	DDR3A_DM2	AF27	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3A_DM3	AK25	1.5 V SSTL Class I	Write mask byte lane
F7	DDR3A_DQ16	AH25	1.5 V SSTL Class I	Data bus
E3	DDR3A_DQ17	AG25	1.5 V SSTL Class I	Data bus
F8	DDR3A_DQ18	AE26	1.5 V SSTL Class I	Data bus
H8	DDR3A_DQ19	AH26	1.5 V SSTL Class I	Data bus
H7	DDR3A_DQ20	AG26	1.5 V SSTL Class I	Data bus
F2	DDR3A_DQ21	AD25	1.5 V SSTL Class I	Data bus
G2	DDR3A_DQ22	AC25	1.5 V SSTL Class I	Data bus
H3	DDR3A_DQ23	AB25	1.5 V SSTL Class I	Data bus
C2	DDR3A_DQ24	AV24	1.5 V SSTL Class I	Data bus
C3	DDR3A_DQ25	AV25	1.5 V SSTL Class I	Data bus
C8	DDR3A_DQ26	AL26	1.5 V SSTL Class I	Data bus
A3	DDR3A_DQ27	AW26	1.5 V SSTL Class I	Data bus
D7	DDR3A_DQ28	AW25	1.5 V SSTL Class I	Data bus
A2	DDR3A_DQ29	AT25	1.5 V SSTL Class I	Data bus
A7	DDR3A_DQ30	AN25	1.5 V SSTL Class I	Data bus
B8	DDR3A_DQ31	AM25	1.5 V SSTL Class I	Data bus
F3	DDR3A_DQS_P2	AF25	Differential 1.5 V SSTL Class I	Data strobe P byte lane 2
G3	DDR3A_DQS_N2	AE25	Differential 1.5 V SSTL Class I	Data strobe N byte lane 2

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
C7	DDR3A_DQS_P3	AU26	Differential 1.5 V SSTL Class I	Data strobe P byte lane 3
B7	DDR3A_DQS_N3	AT26	Differential 1.5 V SSTL Class I	Data strobe N byte lane 3
K1	DDR3A_ODT	AM31	1.5 V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AN31	1.5 V SSTL Class I	Row address select
T2	DDR3A_RESETn	AB29	1.5 V SSTL Class I	Reset
L3	DDR3A_WEN	AW33	1.5 V SSTL Class I	Write enable
L8	DDR3A_ZQ1	—	1.5 V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U29)				
N3	DDR3A_A0	AU29	1.5 V SSTL Class I	Address bus
P7	DDR3A_A1	AT29	1.5 V SSTL Class I	Address bus
P3	DDR3A_A2	AV30	1.5 V SSTL Class I	Address bus
N2	DDR3A_A3	AU30	1.5 V SSTL Class I	Address bus
P8	DDR3A_A4	AT30	1.5 V SSTL Class I	Address bus
P2	DDR3A_A5	AR30	1.5 V SSTL Class I	Address bus
R8	DDR3A_A6	AL30	1.5 V SSTL Class I	Address bus
R2	DDR3A_A7	AK30	1.5 V SSTL Class I	Address bus
T8	DDR3A_A8	AW31	1.5 V SSTL Class I	Address bus
R3	DDR3A_A9	AW30	1.5 V SSTL Class I	Address bus
L7	DDR3A_A10	AV31	1.5 V SSTL Class I	Address bus
R7	DDR3A_A11	AU31	1.5 V SSTL Class I	Address bus
N7	DDR3A_A12	AH30	1.5 V SSTL Class I	Address bus
T3	DDR3A_A13	AG30	1.5 V SSTL Class I	Address bus
T7	DDR3A_A14	AE29	1.5 V SSTL Class I	Address bus
M2	DDR3A_BA0	AT31	1.5 V SSTL Class I	Bank address bus
N8	DDR3A_BA1	AR31	1.5 V SSTL Class I	Bank address bus
M3	DDR3A_BA2	AP31	1.5 V SSTL Class I	Bank address bus
K3	DDR3A_CASN	AW32	1.5 V SSTL Class I	Column address select
K9	DDR3A_CKE	AP30	1.5 V SSTL Class I	Clock enable
J7	DDR3A_CLK_P	AP29	1.5 V SSTL Class I	Differential output clock
K7	DDR3A_CLK_N	AN29	1.5 V SSTL Class I	Differential output clock
L2	DDR3A_CSN	AP32	1.5 V SSTL Class I	Chip select
E7	DDR3A_DM0	AF27	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3A_DM1	AK25	1.5 V SSTL Class I	Write mask byte lane
H3	DDR3A_DQ0	AH25	1.5 V SSTL Class I	Data bus
F8	DDR3A_DQ1	AG25	1.5 V SSTL Class I	Data bus
G2	DDR3A_DQ2	AE26	1.5 V SSTL Class I	Data bus
H8	DDR3A_DQ3	AH26	1.5 V SSTL Class I	Data bus

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
H7	DDR3A_DQ4	AG26	1.5 V SSTL Class I	Data bus
F7	DDR3A_DQ5	AD25	1.5 V SSTL Class I	Data bus
E3	DDR3A_DQ6	AC25	1.5 V SSTL Class I	Data bus
F2	DDR3A_DQ7	AB25	1.5 V SSTL Class I	Data bus
C2	DDR3A_DQ8	AV24	1.5 V SSTL Class I	Data bus
A2	DDR3A_DQ9	AV25	1.5 V SSTL Class I	Data bus
D7	DDR3A_DQ10	AL26	1.5 V SSTL Class I	Data bus
A7	DDR3A_DQ11	AW26	1.5 V SSTL Class I	Data bus
C8	DDR3A_DQ12	AW25	1.5 V SSTL Class I	Data bus
B8	DDR3A_DQ13	AT25	1.5 V SSTL Class I	Data bus
A3	DDR3A_DQ14	AN25	1.5 V SSTL Class I	Data bus
C3	DDR3A_DQ15	AM25	1.5 V SSTL Class I	Data bus
F3	DDR3A_DQS_P0	AF25	Differential 1.5 V SSTL Class I	Data strobe P byte lane 0
G3	DDR3A_DQS_N0	AE25	Differential 1.5 V SSTL Class I	Data strobe N byte lane 0
C7	DDR3A_DQS_P1	AW28	Differential 1.5 V SSTL Class I	Data strobe P byte lane 1
B7	DDR3A_DQS_N1	AW29	Differential 1.5 V SSTL Class I	Data strobe N byte lane 1
K1	DDR3A_ODT	AM31	1.5 V SSTL Class I	On-die termination enable
J3	DDR3A_RASN	AN31	1.5 V SSTL Class I	Row address select
T2	DDR3A_RESETn	AB29	1.5 V SSTL Class I	Reset
L3	DDR3A_WEN	AW33	1.5 V SSTL Class I	Write enable
L8	DDR3A__ZQ	—	1.5 V SSTL Class I	ZQ impedance calibration
DDR3 x32 (U49)				
N3	DDR3B_A0	AP16	1.5 V SSTL Class I	Address bus
P7	DDR3B_A1	AN16	1.5 V SSTL Class I	Address bus
P3	DDR3B_A2	AK16	1.5 V SSTL Class I	Address bus
N2	DDR3B_A3	AJ16	1.5 V SSTL Class I	Address bus
P8	DDR3B_A4	AV16	1.5 V SSTL Class I	Address bus
P2	DDR3B_A5	AU16	1.5 V SSTL Class I	Address bus
R8	DDR3B_A6	AT16	1.5 V SSTL Class I	Address bus
R2	DDR3B_A7	AR16	1.5 V SSTL Class I	Address bus
T8	DDR3B_A8	AP17	1.5 V SSTL Class I	Address bus
R3	DDR3B_A9	AN17	1.5 V SSTL Class I	Address bus
L7	DDR3B_A10	AH17	1.5 V SSTL Class I	Address bus
R7	DDR3B_A11	AG17	1.5 V SSTL Class I	Address bus
N7	DDR3B_A12	AM18	1.5 V SSTL Class I	Address bus

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
T3	DDR3B_A13	AL18	1.5 V SSTL Class I	Address bus
T7	DDR3B_A14	AG18	1.5 V SSTL Class I	Address bus
M2	DDR3B_BA0	AE18	1.5 V SSTL Class I	Bank address bus
N8	DDR3B_BA1	AD18	1.5 V SSTL Class I	Bank address bus
M3	DDR3B_BA2	AC18	1.5 V SSTL Class I	Bank address bus
K3	DDR3B_CASN	AR18	1.5 V SSTL Class I	Column address select
K9	DDR3B_CKE	AM16	1.5 V SSTL Class I	Clock enable
J7	DDR3B_CLK_P	AF16	Differential 1.5 V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	AE17	Differential 1.5 V SSTL Class I	Differential output clock
L2	DDR3B_CSN	AL17	1.5 V SSTL Class I	Chip select
E7	DDR3B_DM2	AU12	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3B_DM3	AV10	1.5 V SSTL Class I	Write mask byte lane
H3	DDR3B_DQ16	AJ13	1.5 V SSTL Class I	Data bus
F2	DDR3B_DQ17	AH13	1.5 V SSTL Class I	Data bus
E3	DDR3B_DQ18	AP12	1.5 V SSTL Class I	Data bus
F8	DDR3B_DQ19	AW11	1.5 V SSTL Class I	Data bus
F7	DDR3B_DQ20	AW10	1.5 V SSTL Class I	Data bus
H8	DDR3B_DQ21	AM13	1.5 V SSTL Class I	Data bus
G2	DDR3B_DQ22	AE13	1.5 V SSTL Class I	Data bus
H7	DDR3B_DQ23	AE14	1.5 V SSTL Class I	Data bus
C8	DDR3B_DQ24	AW9	1.5 V SSTL Class I	Data bus
B8	DDR3B_DQ25	AV9	1.5 V SSTL Class I	Data bus
A7	DDR3B_DQ26	AP11	1.5 V SSTL Class I	Data bus
C2	DDR3B_DQ27	AD13	1.5 V SSTL Class I	Data bus
A2	DDR3B_DQ28	AC13	1.5 V SSTL Class I	Data bus
D7	DDR3B_DQ29	AL12	1.5 V SSTL Class I	Data bus
C3	DDR3B_DQ30	AG13	1.5 V SSTL Class I	Data bus
A3	DDR3B_DQ31	AF13	1.5 V SSTL Class I	Data bus
F3	DDR3B_DQS_P2	AW12	Differential 1.5 V SSTL Class I	Data strobe P byte lane 2
G3	DDR3B_DQS_N2	AV12	Differential 1.5 V SSTL Class I	Data strobe N byte lane 2
C7	DDR3B_DQS_P3	AU11	Differential 1.5 V SSTL Class I	Data strobe P byte lane 3
B7	DDR3B_DQS_N3	AT11	Differential 1.5 V SSTL Class I	Data strobe N byte lane 3
K1	DDR3B_ODT	AD19	1.5 V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	AD17	1.5 V SSTL Class I	Row address select

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 6 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
T2	DDR3B_RESETn	AN15	1.5 V SSTL Class I	Reset
L3	DDR3B_WEN	AP18	1.5 V SSTL Class I	Write enable
L8	DDR3B_ZQ1	—	1.5 V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U43)				
N3	DDR3B_A0	AP16	1.5 V SSTL Class I	Address bus
P7	DDR3B_A1	AN16	1.5 V SSTL Class I	Address bus
P3	DDR3B_A2	AK16	1.5 V SSTL Class I	Address bus
N2	DDR3B_A3	AJ16	1.5 V SSTL Class I	Address bus
P8	DDR3B_A4	AV16	1.5 V SSTL Class I	Address bus
P2	DDR3B_A5	AU16	1.5 V SSTL Class I	Address bus
R8	DDR3B_A6	AT16	1.5 V SSTL Class I	Address bus
R2	DDR3B_A7	AR16	1.5 V SSTL Class I	Address bus
T8	DDR3B_A8	AP17	1.5 V SSTL Class I	Address bus
R3	DDR3B_A9	AN17	1.5 V SSTL Class I	Address bus
L7	DDR3B_A10	AH17	1.5 V SSTL Class I	Address bus
R7	DDR3B_A11	AG17	1.5 V SSTL Class I	Address bus
N7	DDR3B_A12	AM18	1.5 V SSTL Class I	Address bus
T3	DDR3B_A13	AL18	1.5 V SSTL Class I	Address bus
T7	DDR3B_A14	AG18	1.5 V SSTL Class I	Address bus
M2	DDR3B_BA0	AE18	1.5 V SSTL Class I	Bank address bus
N8	DDR3B_BA1	AD18	1.5 V SSTL Class I	Bank address bus
M3	DDR3B_BA2	AC18	1.5 V SSTL Class I	Bank address bus
K3	DDR3B_CASN	AR18	1.5 V SSTL Class I	Column address select
K9	DDR3B_CKE	AM16	1.5 V SSTL Class I	Clock enable
J7	DDR3B_CLK_P	AF16	1.5 V SSTL Class I	Differential output clock
K7	DDR3B_CLK_N	AE17	1.5 V SSTL Class I	Differential output clock
L2	DDR3B_CSN	AL17	1.5 V SSTL Class I	Chip select
E7	DDR3B_DM0	AD16	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3B_DM1	AU13	1.5 V SSTL Class I	Write mask byte lane
H8	DDR3B_DQ0	AU15	1.5 V SSTL Class I	Data bus
F8	DDR3B_DQ1	AT15	1.5 V SSTL Class I	Data bus
H3	DDR3B_DQ2	AH15	1.5 V SSTL Class I	Data bus
H7	DDR3B_DQ3	AW13	1.5 V SSTL Class I	Data bus
G2	DDR3B_DQ4	AV13	1.5 V SSTL Class I	Data bus
F2	DDR3B_DQ5	AL15	1.5 V SSTL Class I	Data bus
F7	DDR3B_DQ6	AW15	1.5 V SSTL Class I	Data bus
E3	DDR3B_DQ7	AW14	1.5 V SSTL Class I	Data bus
B8	DDR3B_DQ8	AE15	1.5 V SSTL Class I	Data bus

Table 2–27. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 7 of 7)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
C8	DDR3B_DQ9	AD15	1.5 V SSTL Class I	Data bus
A7	DDR3B_DQ10	AH14	1.5 V SSTL Class I	Data bus
A3	DDR3B_DQ11	AP14	1.5 V SSTL Class I	Data bus
C3	DDR3B_DQ12	AN14	1.5 V SSTL Class I	Data bus
D7	DDR3B_DQ13	AL14	1.5 V SSTL Class I	Data bus
A2	DDR3B_DQ14	AU14	1.5 V SSTL Class I	Data bus
C2	DDR3B_DQ15	AT14	1.5 V SSTL Class I	Data bus
F3	DDR3B_DQS_P0	AH16	Differential 1.5 V SSTL Class I	Data strobe P byte lane 0
G3	DDR3B_DQS_N0	AG16	Differential 1.5 V SSTL Class I	Data strobe N byte lane 0
C7	DDR3B_DQS_P1	AF15	Differential 1.5 V SSTL Class I	Data strobe P byte lane 1
B7	DDR3B_DQS_N1	AE16	Differential 1.5 V SSTL Class I	Data strobe N byte lane 1
K1	DDR3B_ODT	AD19	1.5 V SSTL Class I	On-die termination enable
J3	DDR3B_RASN	AD17	1.5 V SSTL Class I	Row address select
T2	DDR3B_RESETn	AN15	1.5 V SSTL Class I	Reset
L3	DDR3B_WEN	AP18	1.5 V SSTL Class I	Write enable
L8	DDR3B_ZQ	—	1.5 V SSTL Class I	ZQ impedance calibration

DDR3 SDRAM (HPS)

The development board supports three 32Mx16x8 banks DDR3 SDRAM interface with ECC for very high-speed sequential memory access. The 40-bit data bus comprises of three ×16 devices with a single address or command bus. This interface connects to the dedicated HMC for HPS I/O banks on the top edge of the FPGA.

The DDR3 device shipped with this board are running at 533 MHz, for a total theoretical bandwidth of over 25.6 Gbps. The speed grade of this DDR3 device is 800 MHz with a CAS latency of 9.

Table 2–27 lists the DDR3 SDRAM pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–28. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 5)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
DDR3 x16 (U51)				
N3	DDR3_HPS_A0	N9	1.5 V SSTL Class I	Address bus
P7	DDR3_HPS_A1	M9	1.5 V SSTL Class I	Address bus
P3	DDR3_HPS_A2	N10	1.5 V SSTL Class I	Address bus
N2	DDR3_HPS_A3	M10	1.5 V SSTL Class I	Address bus

Table 2–28. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 5)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
P8	DDR3_HPS_A4	A8	1.5 V SSTL Class I	Address bus
P2	DDR3_HPS_A5	B7	1.5 V SSTL Class I	Address bus
R8	DDR3_HPS_A6	B9	1.5 V SSTL Class I	Address bus
R2	DDR3_HPS_A7	A9	1.5 V SSTL Class I	Address bus
T8	DDR3_HPS_A8	D9	1.5 V SSTL Class I	Address bus
R3	DDR3_HPS_A9	C10	1.5 V SSTL Class I	Address bus
L7	DDR3_HPS_A10	K7	1.5 V SSTL Class I	Address bus
R7	DDR3_HPS_A11	J7	1.5 V SSTL Class I	Address bus
N7	DDR3_HPS_A12	F9	1.5 V SSTL Class I	Address bus
T3	DDR3_HPS_A13	E9	1.5 V SSTL Class I	Address bus
T7	DDR3_HPS_A14	D11	1.5 V SSTL Class I	Address bus
M2	DDR3_HPS_BA0	L7	1.5 V SSTL Class I	Bank address bus
N8	DDR3_HPS_BA1	C9	1.5 V SSTL Class I	Bank address bus
M3	DDR3_HPS_BA2	D8	1.5 V SSTL Class I	Bank address bus
K3	DDR3_HPS_CASN	G9	1.5 V SSTL Class I	Column address select
K9	DDR3_HPS_CKE	R8	1.5 V SSTL Class I	Clock Enable
J7	DDR3_HPS_CLK_P	A11	Differential 1.5 V SSTL Class I	Differential output clock
K7	DDR3_HPS_CLK_N	B10	Differential 1.5 V SSTL Class I	Differential output clock
L2	DDR3_HPS_CSN	H9	1.5 V SSTL Class I	Chip select
E7	DDR3_HPS_DM4	T7	1.5 V SSTL Class I	Write mask byte lane
E3	DDR3_HPS_DQ32	G1	1.5 V SSTL Class I	Data bus
G2	DDR3_HPS_DQ33	F1	1.5 V SSTL Class I	Data bus
F2	DDR3_HPS_DQ34	P6	1.5 V SSTL Class I	Data bus
F8	DDR3_HPS_DQ35	L1	1.5 V SSTL Class I	Data bus
F7	DDR3_HPS_DQ36	M2	1.5 V SSTL Class I	Data bus
H8	DDR3_HPS_DQ37	M1	1.5 V SSTL Class I	Data bus
H7	DDR3_HPS_DQ38	N1	1.5 V SSTL Class I	Data bus
H3	DDR3_HPS_DQ39	R6	1.5 V SSTL Class I	Data bus
F3	DDR3_HPS_DQS_P4	J1	Differential 1.5 V SSTL Class I	Data strobe P byte lane 4
G3	DDR3_HPS_DQS_N4	H1	Differential 1.5 V SSTL Class I	Data strobe N byte lane 4
K1	DDR3_HPS_ODT	H7	1.5 V SSTL Class I	On-die termination enable
J3	DDR3_HPS_RASN	G8	1.5 V SSTL Class I	Row address select
T2	DDR3_HPS_RESETn	E3	1.5 V SSTL Class I	Reset
L3	DDR3_HPS_WEN	J8	1.5 V SSTL Class I	Write enable
L8	DDR3_HPS_ZQ1	—	1.5 V SSTL Class I	ZQ impedance calibration

Table 2–28. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 3 of 5)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
DDR3 x16 (U44)				
N3	DDR3_HPS_A0	N9	1.5 V SSTL Class I	Address bus
P7	DDR3_HPS_A1	M9	1.5 V SSTL Class I	Address bus
P3	DDR3_HPS_A2	N10	1.5 V SSTL Class I	Address bus
N2	DDR3_HPS_A3	M10	1.5 V SSTL Class I	Address bus
P8	DDR3_HPS_A4	A8	1.5 V SSTL Class I	Address bus
P2	DDR3_HPS_A5	B7	1.5 V SSTL Class I	Address bus
R8	DDR3_HPS_A6	B9	1.5 V SSTL Class I	Address bus
R2	DDR3_HPS_A7	A9	1.5 V SSTL Class I	Address bus
T8	DDR3_HPS_A8	D9	1.5 V SSTL Class I	Address bus
R3	DDR3_HPS_A9	C10	1.5 V SSTL Class I	Address bus
L7	DDR3_HPS_A10	K7	1.5 V SSTL Class I	Address bus
R7	DDR3_HPS_A11	J7	1.5 V SSTL Class I	Address bus
N7	DDR3_HPS_A12	F9	1.5 V SSTL Class I	Address bus
T3	DDR3_HPS_A13	E9	1.5 V SSTL Class I	Address bus
T7	DDR3_HPS_A14	D11	1.5 V SSTL Class I	Address bus
M2	DDR3_HPS_BA0	L7	1.5 V SSTL Class I	Bank address bus
N8	DDR3_HPS_BA1	C9	1.5 V SSTL Class I	Bank address bus
M3	DDR3_HPS_BA2	D8	1.5 V SSTL Class I	Bank address bus
K3	DDR3_HPS_CASN	G9	1.5 V SSTL Class I	Column address select
K9	DDR3_HPS_CKE	R8	1.5 V SSTL Class I	Clock Enable
J7	DDR3_HPS_CLK_P	A11	1.5 V SSTL Class I	Differential output clock
K7	DDR3_HPS_CLK_N	B10	1.5 V SSTL Class I	Differential output clock
L2	DDR3_HPS_CSN	H9	1.5 V SSTL Class I	Chip select
E7	DDR3_HPS_DM2	D3	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3_HPS_DM3	D1	1.5 V SSTL Class I	Write mask byte lane
F2	DDR3_HPS_DQ16	J5	1.5 V SSTL Class I	Data bus
H3	DDR3_HPS_DQ17	K5	1.5 V SSTL Class I	Data bus
G2	DDR3_HPS_DQ18	N7	1.5 V SSTL Class I	Data bus
F8	DDR3_HPS_DQ19	F3	1.5 V SSTL Class I	Data bus
H7	DDR3_HPS_DQ20	H3	1.5 V SSTL Class I	Data bus
E3	DDR3_HPS_DQ21	J4	1.5 V SSTL Class I	Data bus
H8	DDR3_HPS_DQ22	M5	1.5 V SSTL Class I	Data bus
F7	DDR3_HPS_DQ23	C3	1.5 V SSTL Class I	Data bus
A3	DDR3_HPS_DQ24	A2	1.5 V SSTL Class I	Data bus
C3	DDR3_HPS_DQ25	A3	1.5 V SSTL Class I	Data bus
C8	DDR3_HPS_DQ26	P7	1.5 V SSTL Class I	Data bus
A7	DDR3_HPS_DQ27	C1	1.5 V SSTL Class I	Data bus

Table 2–28. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 4 of 5)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
C2	DDR3_HPS_DQ28	G2	1.5 V SSTL Class I	Data bus
A2	DDR3_HPS_DQ29	F2	1.5 V SSTL Class I	Data bus
B8	DDR3_HPS_DQ30	M3	1.5 V SSTL Class I	Data bus
D7	DDR3_HPS_DQ31	E1	1.5 V SSTL Class I	Data bus
F3	DDR3_HPS_DQS_P2	G4	Differential 1.5 V SSTL Class I	Data strobe P byte lane 1
G3	DDR3_HPS_DQS_N2	H4	Differential 1.5 V SSTL Class I	Data strobe P byte lane 0
C7	DDR3_HPS_DQS_P3	C2	Differential 1.5 V SSTL Class I	Data strobe N byte lane 1
B7	DDR3_HPS_DQS_N3	D2	Differential 1.5 V SSTL Class I	Data strobe N byte lane 0
K1	DDR3_HPS_ODT	H7	1.5 V SSTL Class I	On-die termination enable
J3	DDR3_HPS_RASN	G8	1.5 V SSTL Class I	Row address select
T2	DDR3_HPS_RESETn	E3	1.5 V SSTL Class I	Reset
L3	DDR3_HPS_WEN	J8	1.5 V SSTL Class I	Write enable
L8	DDR3_HPS_ZQ2	—	1.5 V SSTL Class I	ZQ impedance calibration
DDR3 x16 (U38)				
N3	DDR3_HPS_A0	N9	1.5 V SSTL Class I	Address bus
P7	DDR3_HPS_A1	M9	1.5 V SSTL Class I	Address bus
P3	DDR3_HPS_A2	N10	1.5 V SSTL Class I	Address bus
N2	DDR3_HPS_A3	M10	1.5 V SSTL Class I	Address bus
P8	DDR3_HPS_A4	A8	1.5 V SSTL Class I	Address bus
P2	DDR3_HPS_A5	B7	1.5 V SSTL Class I	Address bus
R8	DDR3_HPS_A6	B9	1.5 V SSTL Class I	Address bus
R2	DDR3_HPS_A7	A9	1.5 V SSTL Class I	Address bus
T8	DDR3_HPS_A8	D9	1.5 V SSTL Class I	Address bus
R3	DDR3_HPS_A9	C10	1.5 V SSTL Class I	Address bus
L7	DDR3_HPS_A10	K7	1.5 V SSTL Class I	Address bus
R7	DDR3_HPS_A11	J7	1.5 V SSTL Class I	Address bus
N7	DDR3_HPS_A12	F9	1.5 V SSTL Class I	Address bus
T3	DDR3_HPS_A13	E9	1.5 V SSTL Class I	Address bus
T7	DDR3_HPS_A14	D11	1.5 V SSTL Class I	Address bus
M2	DDR3_HPS_BA0	L7	1.5 V SSTL Class I	Bank address bus
N8	DDR3_HPS_BA1	C9	1.5 V SSTL Class I	Bank address bus
M3	DDR3_HPS_BA2	D8	1.5 V SSTL Class I	Bank address bus
K3	DDR3_HPS_CASN	G9	1.5 V SSTL Class I	Column address select
K9	DDR3_HPS_CKE	R8	1.5 V SSTL Class I	Clock Enable
J7	DDR3_HPS_CLK_P	A11	1.5 V SSTL Class I	Differential output clock

Table 2–28. DDR3 SDRAM Pin Assignments, Schematic Signal Names, and Functions (Part 5 of 5)

Board Reference	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
K7	DDR3_HPS_CLK_N	B10	1.5 V SSTL Class I	Differential output clock
L2	DDR3_HPS_CSN	H9	1.5 V SSTL Class I	Chip select
E7	DDR3_HPS_DM0	C6	1.5 V SSTL Class I	Write mask byte lane
D3	DDR3_HPS_DM1	E4	1.5 V SSTL Class I	Write mask byte lane
F7	DDR3_HPS_DQ0	D7	1.5 V SSTL Class I	Data bus
F8	DDR3_HPS_DQ1	C7	1.5 V SSTL Class I	Data bus
F2	DDR3_HPS_DQ2	R10	1.5 V SSTL Class I	Data bus
E3	DDR3_HPS_DQ3	G7	1.5 V SSTL Class I	Data bus
H8	DDR3_HPS_DQ4	A6	1.5 V SSTL Class I	Data bus
H3	DDR3_HPS_DQ5	A7	1.5 V SSTL Class I	Data bus
G2	DDR3_HPS_DQ6	L6	1.5 V SSTL Class I	Data bus
H7	DDR3_HPS_DQ7	D6	1.5 V SSTL Class I	Data bus
C3	DDR3_HPS_DQ8	H6	1.5 V SSTL Class I	Data bus
A3	DDR3_HPS_DQ9	G6	1.5 V SSTL Class I	Data bus
A2	DDR3_HPS_DQ10	N8	1.5 V SSTL Class I	Data bus
D7	DDR3_HPS_DQ11	G5	1.5 V SSTL Class I	Data bus
A7	DDR3_HPS_DQ12	A4	1.5 V SSTL Class I	Data bus
B8	DDR3_HPS_DQ13	A5	1.5 V SSTL Class I	Data bus
C2	DDR3_HPS_DQ14	R9	1.5 V SSTL Class I	Data bus
C8	DDR3_HPS_DQ15	F4	1.5 V SSTL Class I	Data bus
F3	DDR3_HPS_DQS_P0	F7	Differential 1.5 V SSTL Class I	Data strobe P byte lane 1
G3	DDR3_HPS_DQS_N0	E7	Differential 1.5 V SSTL Class I	Data strobe P byte lane 0
C7	DDR3_HPS_DQS_P1	D5	Differential 1.5 V SSTL Class I	Data strobe N byte lane 1
B7	DDR3_HPS_DQS_N1	E6	Differential 1.5 V SSTL Class I	Data strobe N byte lane 0
K1	DDR3_HPS_ODT	H7	1.5 V SSTL Class I	On-die termination enable
J3	DDR3_HPS_RASN	G8	1.5 V SSTL Class I	Row address select
T2	DDR3_HPS_RESETn	E3	1.5 V SSTL Class I	Reset
L3	DDR3_HPS_WEN	J8	1.5 V SSTL Class I	Write enable
L8	DDR3_HPS_ZQ	—	1.5 V SSTL Class I	ZQ impedance calibration

QSPI Flash (HPS)

The development board supports one 1-Gb serial NOR flash device for non-volatile storage of the HPS boot code, user data, and program. The device connects to the HPS dedicated interface and may contain a secondary boot code.

This 4-bit data memory interface can sustain burst read operations at up to 108 MHz for a throughput of 54 MBps. Erase capability is at 4 KB, 64 KB, and 32 MB.

Table 2–29 lists the QSPI flash pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–29. QSPI Flash Schematic Signal Names and Functions

Board Reference (U19)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
16	QSPI_CLK	F15	3.3 V	Clock
15	QSPI_IO0	D15	3.3 V	Data bus
8	QSPI_IO1	G15	3.3 V	Data bus
9	QSPI_IO2	M15	3.3 V	Data bus
1	QSPI_IO3	H15	3.3 V	Data bus
7	QSPI_SS0	N15	3.3 V	Chip enable
3	MAX_QSPI_RSTN	—	3.3 V	Reset

EPCQ Flash

The development board supports one 256-Mb serial/quad-serial NOR flash device for non-volatile storage of the FPGA configuration image. The device connects to the FPGA dedicated interface through the IDTQS3861 device.

Table 2–30 lists the EPCQ flash pin assignments, signal names, and functions. The signal names and types are relative to the MAX V CPLD 5M2210 System Controller in terms of I/O setting and direction. Some pins are used in other interfaces as well due to functionality sharing.

Table 2–30. EPCQ Flash Schematic Signal Names and Functions

Board Reference (U28)	Schematic Signal Name	I/O Standard	Description
16	FPGA_DCLK	3.3 V	Clock
15	FPGA_AS_DATA0	3.3 V	Data bus
8	FPGA_AS_DATA1	3.3 V	Data bus
9	FPGA_AS_DATA2	3.3 V	Data bus
1	FPGA_AS_DATA3	3.3 V	Data bus
7	FPGA_NCS0	3.3 V	Chip enable

Synchronous Flash

The development board supports a 512-Mb CFI-compatible synchronous flash device for non-volatile storage of FPGA configuration data, board information, and test application data. This device connects to the MAX V CPLD 5M2210 System Controller for FPGA configuration in FPP and PS modes.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word buffer while the erase time is 800 ms for a 128 K array block.

Table 2–31 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the MAX V CPLD 5M2210 System Controller in terms of I/O setting and direction.

Table 2–31. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 1 of 2)

Board Reference (U13)	Schematic Signal Name	I/O Standard	Description
F6	FLASH_ADVN	1.8 V	Address valid
B4	FLASH_CEN0	1.8 V	Chip enable
E6	FLASH_CLK	1.8 V	Clock
F8	FLASH_OEN	1.8 V	Output enable
F7	FLASH_RDYBSYN	1.8 V	Ready
D4	FLASH_RESETn	1.8 V	Reset
G8	FLASH_WEN	1.8 V	Write enable
C6	FLASH_WPN	1.8 V	Write protect
A1	FM_A1	1.8 V	Address bus
B1	FM_A2	1.8 V	Address bus
C1	FM_A3	1.8 V	Address bus
D1	FM_A4	1.8 V	Address bus
D2	FM_A5	1.8 V	Address bus
A2	FM_A6	1.8 V	Address bus
C2	FM_A7	1.8 V	Address bus
A3	FM_A8	1.8 V	Address bus
B3	FM_A9	1.8 V	Address bus
C3	FM_A10	1.8 V	Address bus
D3	FM_A11	1.8 V	Address bus
C4	FM_A12	1.8 V	Address bus
A5	FM_A13	1.8 V	Address bus
B5	FM_A14	1.8 V	Address bus
C5	FM_A15	1.8 V	Address bus
D7	FM_A16	1.8 V	Address bus
D8	FM_A17	1.8 V	Address bus
A7	FM_A18	1.8 V	Address bus
B7	FM_A19	1.8 V	Address bus
C7	FM_A20	1.8 V	Address bus

Table 2–31. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

Board Reference (U13)	Schematic Signal Name	I/O Standard	Description
C8	FM_A21	1.8 V	Address bus
A8	FM_A22	1.8 V	Address bus
G1	FM_A23	1.8 V	Address bus
H8	FM_A24	1.8 V	Address bus
B6	FM_A25	1.8 V	Address bus
B8	FM_A26	1.8 V	Address bus
F2	FM_D0	1.8 V	Data bus
E2	FM_D1	1.8 V	Data bus
G3	FM_D2	1.8 V	Data bus
E4	FM_D3	1.8 V	Data bus
E5	FM_D4	1.8 V	Data bus
G5	FM_D5	1.8 V	Data bus
G6	FM_D6	1.8 V	Data bus
H7	FM_D7	1.8 V	Data bus
E1	FM_D8	1.8 V	Data bus
E3	FM_D9	1.8 V	Data bus
F3	FM_D10	1.8 V	Data bus
F4	FM_D11	1.8 V	Data bus
F5	FM_D12	1.8 V	Data bus
H5	FM_D13	1.8 V	Data bus
G7	FM_D14	1.8 V	Data bus
E7	FM_D15	1.8 V	Data bus

Micro SD Flash Memory

The development board supports a micro SD card interface using x4 data lines. The micro SD card interface may contain secondary boot code.

This 4-bit data interface can sustain burst read operations at up to 50 MHz for a throughput of 25 MBps.

Table 2–32 lists the micro SD flash memory interface pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–32. Micro SD Flash Memory Interface Schematic Signal Names and Functions (Part 1 of 2)

Board Reference (J5)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
5	SD_CLK	L16	3.3 V	Clock
7	SD_DAT0	C17	3.3 V	Data bus
8	SD_DAT1	N16	3.3 V	Data bus
1	SD_DAT2	J16	3.3 V	Data bus

Table 2–32. Micro SD Flash Memory Interface Schematic Signal Names and Functions (Part 2 of 2)

Board Reference (J5)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
2	SD_CD_DAT3	M16	3.3 V	Control or data bus
3	SD_CMD	D16	3.3 V	Command

I²C EEPROM

This board includes a 32 Kb EEPROM device. This device has a 2-wire I²C serial interface bus and is organized as four blocks of 4K x 8-bit memory. The main function of the device is for EtherCAT IP usage, but it can be used for other storage purposes as well.

Table 2–33 lists the I²C EEPROM pin assignments, signal names, and functions. The signal names and types are relative to the Arria V SoC in terms of I/O setting and direction.

Table 2–33. I²C EEPROM Schematic Signal Names and Functions

Board Reference (U34)	Schematic Signal Name	Arria V SoC Pin Number	I/O Standard	Description
6	I2C_SCL_HPS	L13	3.3 V	Management serial clock
5	I2C_SDA_HPS	C13	3.3 V	Management serial data

Power Supply

You can power up the development board from a laptop-style DC power input or through the DC auxiliary connector. The Arria V SoC is designed in such way that the power rails for the HPS and FPGA are independent, allowing power down for the FPGA side when the HPS side is running. This eliminates power consumption on the FPGA part when not in use.

Table 2–34 lists the maximum allowed draws of the power input.

Table 2–34. Power Input Maximum Allowed Draws

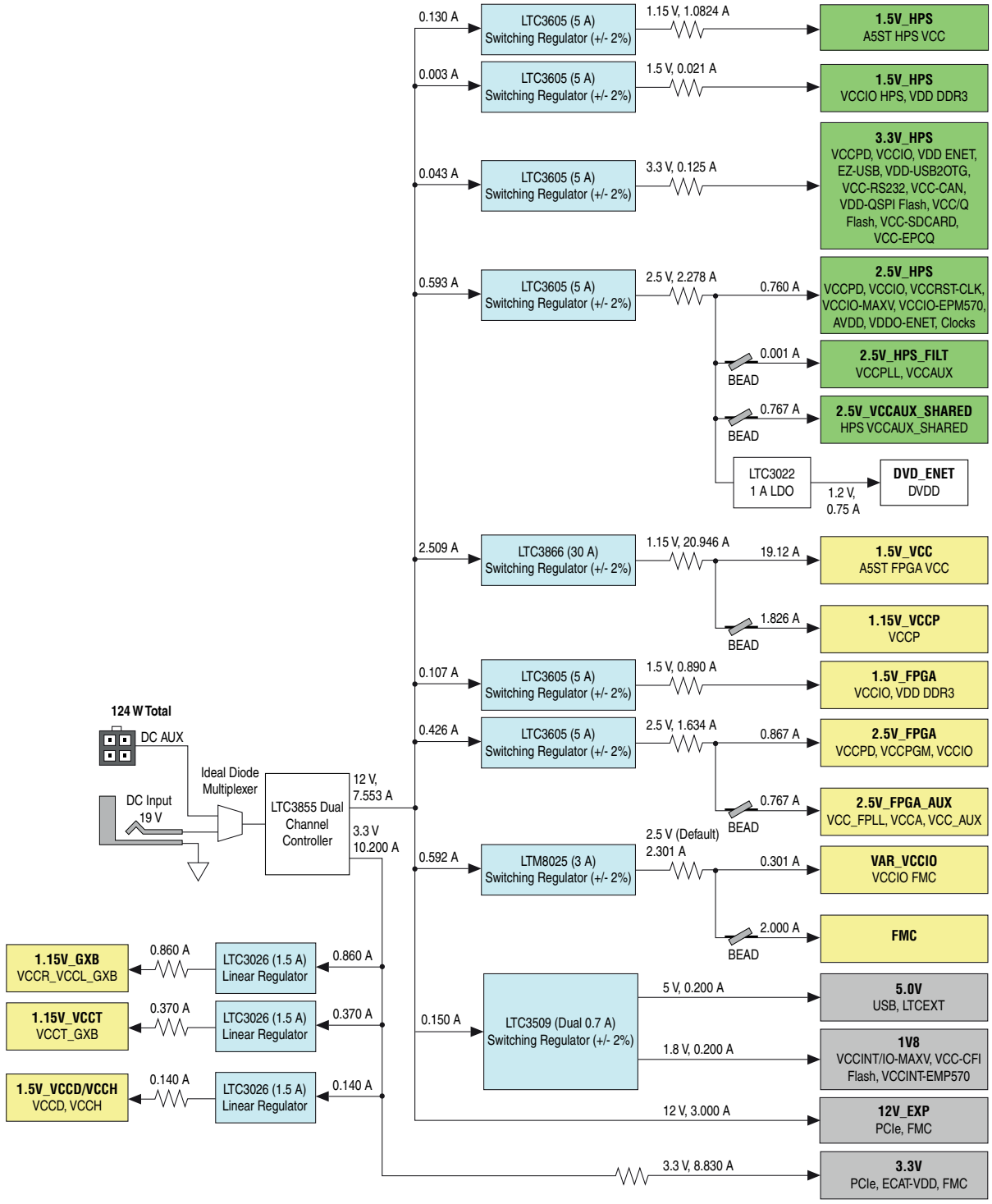
Source	Voltage (V)	Wattage (W)
Laptop Supply—DC input	16.0	300
	20.0	200
DC auxiliary connector	12.0	200

An on-board multi-channel analog-to-digital converter (ADC) measures the current for several specific board rails.

Power Distribution System

Figure 2–9 shows the power distribution system on the development board. Regulator inefficiencies and sharing are reflected in the currents shown, which are conservative absolute maximum levels.

Figure 2–9. Power Distribution System



Power Measurement

There are eleven power supply rails that have on-board current sense capabilities using 16-bit differential ADC devices. Precision sense resistors split the ADC devices and rails from the primary supply plane for the ADC to measure current.

Figure 2–10 shows the block diagram for the power measurement circuitry.

Figure 2–10. Power Measurement Circuit

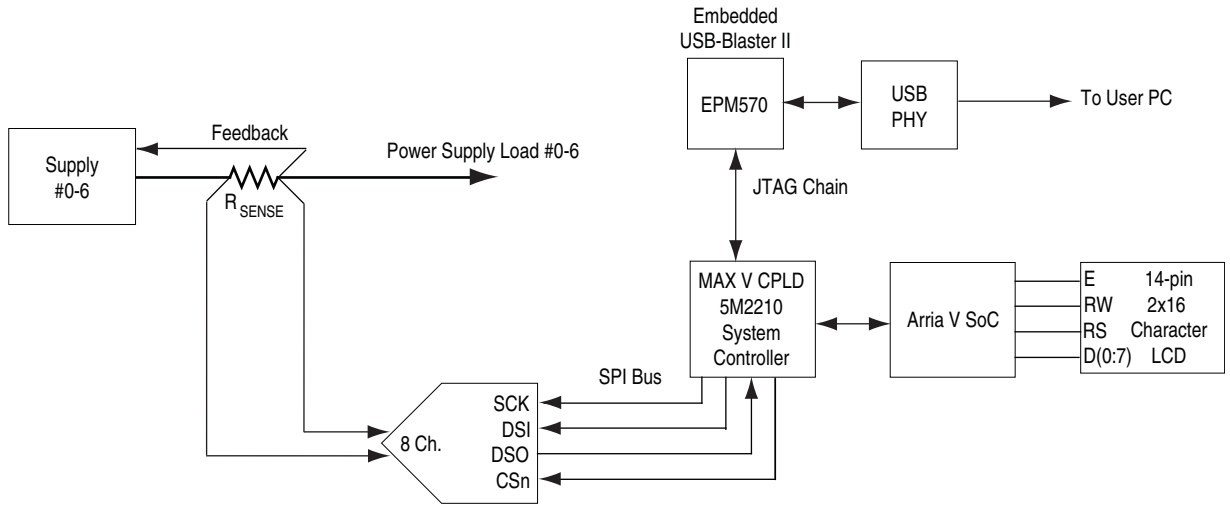


Table 2–35 lists the targeted rails. The schematic signal name column specifies the name of the rail being measured while the device pin column specifies the devices attached to the rail.

Table 2–35. Power Measurement Rails (Part 1 of 2)

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
0	2.5V_FPGA	2.5	VCCIO	I/O, FPGA internal and peripheral devices
			VCCPD	
			VCC	
1	1.5V_FPGA	1.5	VCCIO	I/O and DDR3 devices
2	1.15V_VCC	1.15	VCC	FPGA core power, transceiver, and clock
3	VAR_VCCIO	2.5, 1.8, 1.5, 1.2	VCCIO	FMC I/O
4	1.15V_GXB	1.15	VCCR_GXB	Receiver power
			VCCL_GXB	Transceiver clock network
5	1.15V_VCCT	1.15	VCCT_GXB	Transmitter power
6	1.5V_VCCD/VCCH	1.5	VCCD_FPLL	Phase-locked loop (PLL) digital power
			VCCH_GXB	Transmitter output buffer power
7	1.15V_HPS	1.15	VCC_HPS	HPS core power
8	1.5V_HPS	1.5	VCCIO_HPS	I/O and DDR3 devices

Table 2–35. Power Measurement Rails (Part 2 of 2)

Channel	Schematic Signal Name	Voltage (V)	Device Pin	Description
9	2.5V_HPS	2.5	VCCPD_HPS	I/O, HPS internal and peripheral devices
			VCCIO_HPS	
			VCC_AUX	
10	3.3V_HPS	3.3	VCCPD_HPS	I/O and HPS peripheral devices
			VCCIO_HPS	

3. Board Components Reference

This chapter lists the component reference and manufacturing information of all the components on the Arria V SoC development board.

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U41	Arria V SoC FPGA F1517, 462,000 LEs, lead free	Altera Corporation	5ASTFD5K3F40I3	www.altera.com
U27	MAX V CPLD 5M2210 System Controller	Altera Corporation	5M2210ZF256	www.altera.com
U61	High-Speed USB peripheral controller	Cypress	CY7C68013A	www.cypress.com
D9-D16, D20-D24, D33-D36, D38-D43,	Green LEDs	Lumex Inc.	SML-LXT0805GW-TR	www.lumex.com
D39	Red LED	Lumex Inc.	SML-LXT0805IW-TR	www.lumex.com
D37	Blue LED	Lumex Inc.	SML-LX0805USBC-TR	www.lumex.com
SW2, SW4	Four-position DIP switches	C&K Components/ ITT Industries	TDA04H0SB1	www.ck-components.com
SW1, SW3	Eight-Position DIP switch	C & K Components	TDA08H0SB1	www.ck-components.com
S1-S9, S12-S14	Push buttons	Panasonic	EVQPAC07K	www.panasonic.com
J17	External Mictor 38-pin connector	Tyco Electronics	2-767004-2	www.te.com
X4	50 MHz 1.8 V oscillator	ECS, Inc.	ECS-3518-500-B-xx	www.ecsxtal.com
X5	125.00 MHz LVDS crystal oscillator	Epson	EG-2121CA 125.0000M-LGPNL3	www.eea.epson.com
U35	Programmable quad clock, I^2C 0x70, defaults LVDS 156.25 MHz, 25 MHz, 25 MHz, 100 MHz default	Silicon Labs	Si5338C-A01917-GM	www.silabs.com
U42	IC - Pre-programmed (quad clock generator), 25, 25, 100, 100 MHZ LVCMOS, 1.8V, 2.5V	Silicon Labs	Si5335A-B02062-GM	www.silabs.com
U59	IC - PCIE Gen 1/2 dual output clock generator	Silicon Labs	SI52112-B3-GM2	www.silabs.com
U30	1 to 3 single-ended clock buffer	Silicon Labs	SL18860DC	www.silabs.com
X2	Programmable LVDS clock 100M defaults	Silicon Labs	570FAB000973DG	www.silabs.com
X3	Programmable LVDS clock 148.5M defaults	Silicon Labs	571FAB000973DG	www.silabs.com
J29	2×7 pin LCD socket strip	Samtec	TSM-107-07-G-D	www.samtec.com
	2×16 character LCD, 5×8 dot matrix	Lumex Inc.	LCM-S01602DSR/C	www.lumex.com

Table 3–1. Component Reference and Manufacturing Information

Board Reference	Component	Manufacturer	Manufacturing Part Number	Manufacturer Website
U7, U55	Ethernet PHY BASE-T devices	Marvell Semiconductor	88E1111-B2-CAA1C000	www.marvell.com
J13	MagJack 1000BaseT, 1×1 integrated connector module (ICM)	Bel Fuse	L829-1J1T-43	www.belfuse.com
J47, J48	RJ45 connector with integrated transformer	Wurth Elektronik	7499011121A	www.we-online.com
J42	PCIE socket ×4	Samtec	PCIE-064-02-F-D-TH	www.samtec.com
J4, J26	FMC 0.050 pitch socket array assembly, 400 I/O, 40 x 10 configuration	Samtec	ASP-134486-01	www.samtec.com
B5	SFP+ right-angle, press-fit cage	Molex	74754-0101	www.molex.com
J443, J44	SFP+ right-angle, 20-pin SMT connector	Samtec	MECT-110-01-M-D-RA1	www.samtec.com
U25, U26	USB to serial UART interface	Future Technology Devices International Ltd.	FT232RQ	www.ftdichip.com
U11	Real-time clock	Maxim	DS1339C	www.maxim-ic.com
U29, U37, U38, U43, U44, U51 U49	32M × 16 × 8, 1024-MB DDR3 SDRAM	Micron	MT41K256M16HA-125:E	www.micron.com
U19	256-Mb QSPI flash	Micron	N25Q00AA13GSF40F	www.micron.com
U13	512-Mb CFI synchronous flash	Numonyx	PC28F512P30BF	www.numonyx.com
U28	256-Mb NOR flash	Altera Corporation	EPCQ256SI16N	www.altera.com
U34	32-Kb I^2C EEPROM	Microchip	24LC32A	www.microchip.com
J5	Micro SD card socket	Wurth Elektronik	693 071 010 811	www.we-online.com
U26, U34	Octal digital power supply manager with EEPROM	Linear Technology	LTC2978	www.linear.com

Statement of China-RoHS Compliance

Table 3–2 lists hazardous substances included with the kit.

Table 3–2. Table of Hazardous Substances' Name and Concentration *Notes (1), (2)*

Part Name	Lead (Pb)	Cadmium (Cd)	Hexavalent Chromium (Cr6+)	Mercury (Hg)	Polybrominated biphenyls (PBB)	Polybrominated diphenyl Ethers (PBDE)
Arria V SoC development board	X*	0	0	0	0	0
16 V power supply	0	0	0	0	0	0
Type A-B USB cable	0	0	0	0	0	0
User guide	0	0	0	0	0	0

Notes to Table 3–2:

(1) 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

(2) X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.

CE EMI Conformity Caution

This development kit is delivered conforming to relevant standards mandated by Directive 2004/108/EC. Because of the nature of programmable logic devices, it is possible for the user to modify the kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as the result of modifications to the delivered material is the responsibility of the user.

This chapter provides additional information about the board, document and Altera.

Board Revision History

The following table lists the versions of all releases of the Arria V SoC development board.

Release Date	Version	Description
December 2013	Engineering silicon	Initial release.

Document Revision History

The following table lists the revision history for this document.

Date	Version	Changes
September 2015	1.3	■ Corrected and clarified signal names, board references, and signal descriptions. ■ Corrected battery part number. ■ Corrected signal names PCIE_SMBCLK and PCIE_SMBDAT. ■ Corrected the following I/O standards in Table 2–13 on page 2–20: ■ USER_LED_FPGA0 ■ USER_LED_FPGA1 ■ USER_LED_FPGA2 ■ USER_LED_FPGA3 ■ Corrected the following I/O standards in Table 2–12 on page 2–20: ■ USER_DIPSW_FPGA0 ■ USER_DIPSW_FPGA1 ■ USER_DIPSW_FPGA2 ■ USER_DIPSW_FPGA3 ■ Added missing signal ENET1_RX_DV in Table 2–20 on page 2–28. ■ Corrected I/O standard for discrete SFP+ control signals in Table 2–25 on page 2–37. ■ Corrected pin numbers for SFPB_RX_N and SFPB_RX_P in Table 2–25 on page 2–37. ■ Removed incorrect information about Micro SD card interface MUXing
July 2014	1.2	Added information for PCIe Gen2.
April 2014	1.1	■ Corrected reference manual to include proper F1517 info. ■ Corrected Table 2–8 ON/OFF descriptions.
December 2013	1.0	Initial release.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support

Contact (1)	Contact Method	Address
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."
`Courier type`	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	The question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	The multimedia icon directs you to a related multimedia presentation.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.

Visual Cue	Meaning
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.
	The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.