ADC08B3000 8-Bit, 3 GSPS, High Performance, Low Power A/D Converter with 4K Buffer

Check for Samples: ADC08B3000

FEATURES

- **Single +1.9V ±0.1V Operation**
- **Choice of SDR or DDR Output Clocking**
- **Internal selectable 4K Data Buffer**
- **Serial Interface for Extended Control**
- **Adjustment of Input Full-Scale Range, Offset and Clock Phase**
- **Duty Cycle Corrected Sample Clock**
- **Test Pattern Output Capability**

APPLICATIONS

- **Distance Ranging**
- **Test and Measurement**

KEY SPECIFICATIONS

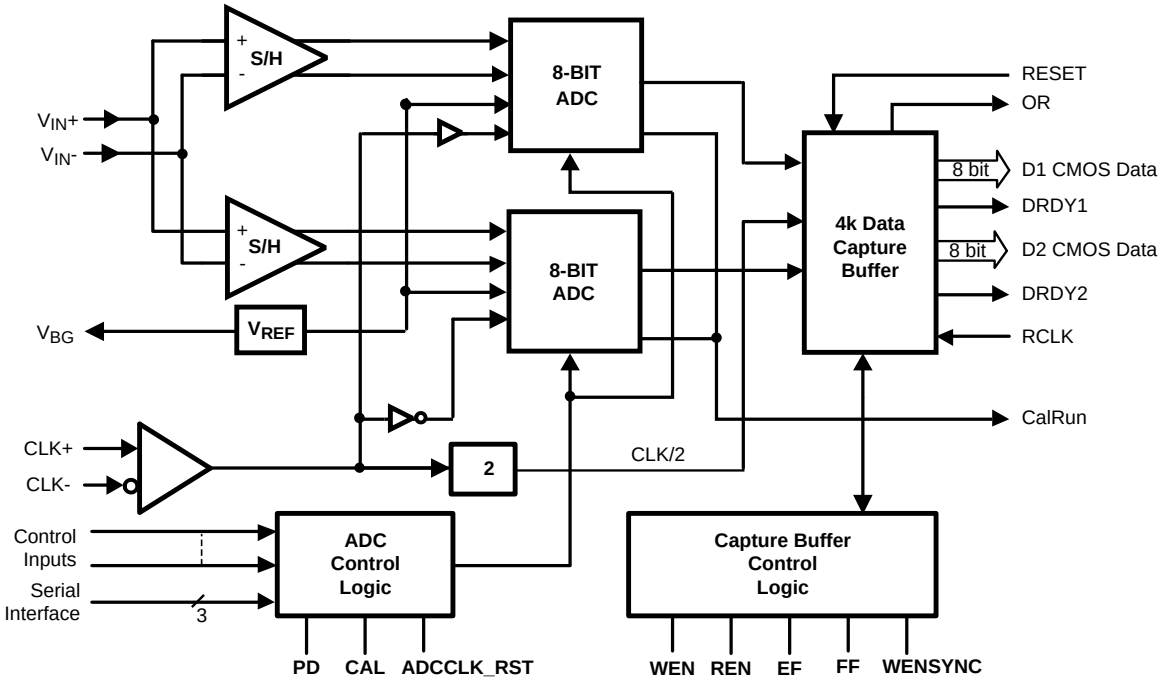
- **Resolution: 8 Bits**
- **Max Conversion Rate: 3 Gsps (min)**
- **Code Error Rate: 10^{-18} (typ)**
- **ENOB @ 748 MHz Input: 7.1 Bits (typ)**
- **SNR @ 748 MHz: 44.9 dB (typ)**
- **Full Power Bandwidth: 3 GHz (typ)**
- **Power Consumption**
  - **Full Power Capure: 1.6 W (typ)**
  - **Power Down Mode: 25 mW (typ)**

DESCRIPTION

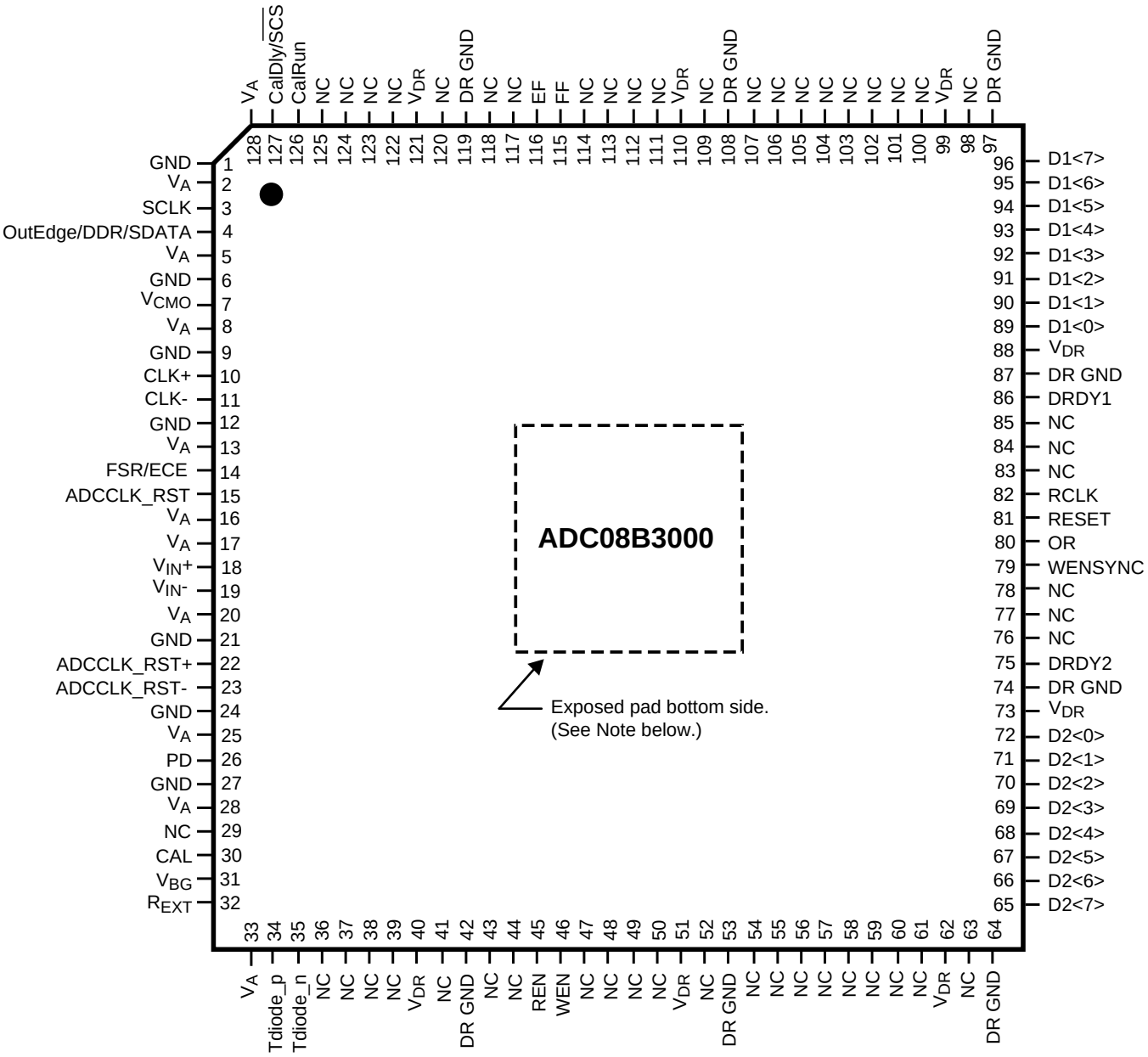
The ADC08B3000 is a single, low power, high performance CMOS analog-to-digital converter that digitizes signals to 8 bits resolution at sample rates up to 3.4 Gigasamples Per Second, (Gsps). Consuming a typical 1.6 Watts at 3 Gsps from a single 1.9 Volt supply, this device is ensured to have no missing codes over the full operating temperature range. The unique folding and interpolating architecture, the fully differential comparator design, the innovative design of the internal sample-and-hold amplifier and the calibration scheme enable an excellent response of all dynamic parameters up to Nyquist, producing a high 7.1 Effective Number Of Bits, (ENOB), with a 748 MHz input signal and a 3 GHz sample rate while providing a 10^{-18} Code Error Rate. A sample rate of 3 Gsps is achieved by interleaving two ADCs, each operating at 1.5 Gsps. Output formatting is offset binary. The device contains a 4K Capture Buffer with output on two 8-bit Low Voltage CMOS (LVCMOS) output buses at rates up to 200MHz.

The converter typically consumes less than 25 mW in the Power Down Mode and is available in a 128-lead, thermally enhanced exposed pad HLQFP and operates over the Industrial ($-40°C \le T_A \le +85°C$) temperature range.

Block Diagram



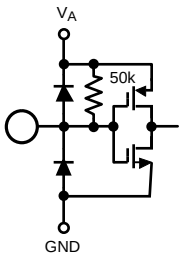
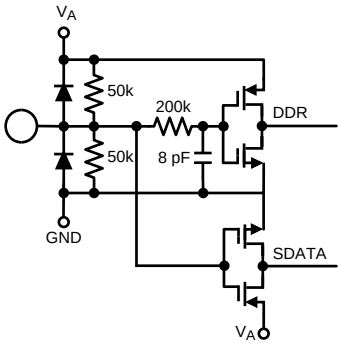
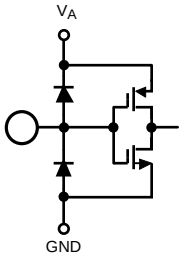
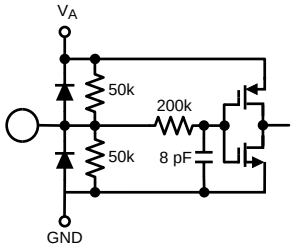
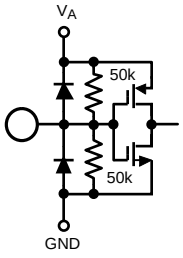
Pin Configuration



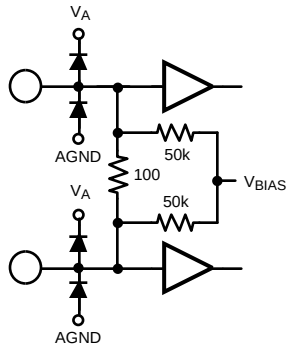
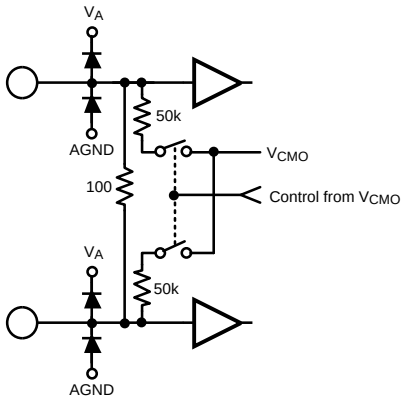
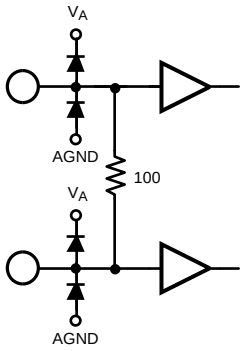
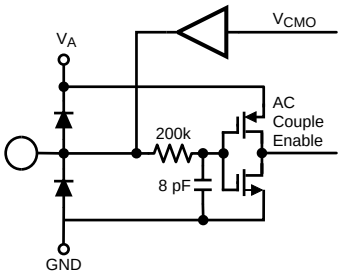
Note: The exposed pad on the bottom of the package must be soldered to a ground plane to ensure rated performance.

Figure 1. HLQFP Package
See Package Number NNB0128A

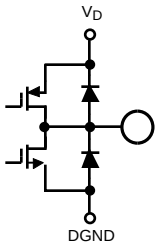
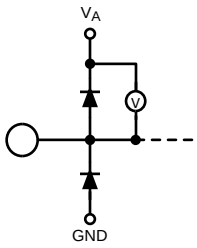
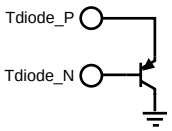
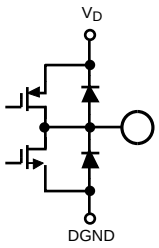
Pin Descriptions and Equivalent Circuits

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
3	SCLK		**Serial Interface Clock** **(Input): LVCMOS -** When the extended control mode is enabled, this pin functions as the SCLK input which clocks in the serial data. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface. Ground this pin when the ADC is not in extended control mode.
4	OutEdge / DDR / SDATA		**Edge Select / Double Data Rate / Serial Data** **(Input): LVCMOS -** When this input is low or high, it sets the edge of DRDY at which the output data transitions. (See OutEdge Setting). When this pin is floating or connected to 1/2 the supply voltage, DDR clocking is enabled. When the extended control mode is enabled, this pin functions as the SDATA input. See NORMAL/EXTENDED CONTROL for details on the extended control mode. See THE SERIAL INTERFACE for description of the serial interface.
15	ADCCLK_RST		**ADC Sample Clock Reset** **(Input): LVCMOS -** A positive pulse on this pin is used to reset and synchronize the ADC08B3000 with other ADC08B3000s in the system. See MULTIPLE ADC SYNCHRONIZATION. When bit 14 in the Configuration Register (address 1h) is set to 0b, this single-ended ADCCLK_RST pin is selected. See description of *pins 22, 23*.
26	PD		**Power Down** **(Input): LVCMOS -** A logic high on the PD pin puts the device, except for the Capture Buffer, into the Power Down Mode.
30	CAL		**Calibration Cycle Initiate** **(Input): LVCMOS -** A minimum 80 input clock cycles logic low followed by a minimum of 80 input clock cycles high on this pin initiates the self calibration sequence. See Calibration for an overview of calibration and On-Command Calibration for a description of on-command calibration.
14	FSR/ECE		**Full Scale Range Select / Extended Control Enable** **(Input): LVCMOS -** In the Normal (Non-Extended) Control Mode, a logic low on this pin sets the full-scale differential input range to 600 mV_{P-P}. A logic high on this pin sets the full-scale differential input range to 810 mV_{P-P}. See The Analog Inputs. To enable the extended control mode, whereby the serial interface and control registers are employed, allow this pin to float or connect it to a voltage equal to $V_A/2$. See NORMAL/EXTENDED CONTROL for information on the extended control mode.
127	CalDly / $\overline{SCS}$		**Calibration Delay / Serial Interface Chip Select** **(Input): LVCMOS -** With a logic high or low on pin 14, this pin functions as Calibration Delay and sets the number of input clock cycles after power up before calibration begins (See Calibration). With pin 14 floating, this pin acts as the chip select pin for the serial interface input and the CalDly value becomes "0" (short delay with no provision for a long power-up calibration delay).

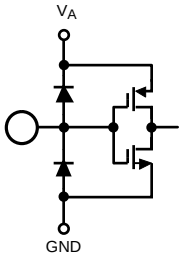
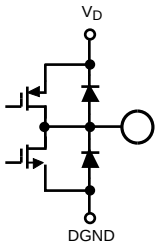
Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
10 11	CLK+ CLK-		**Sample Clock Input** **(Input): LVDS -** The differential clock signal must be a.c. coupled to these pins. The input signal is sampled on both the rising and falling edge of CLK. See Acquiring the Input for a description of acquiring the input, Clocking and THE SAMPLE CLOCK INPUT for an overview of the clock inputs.
18 19	V_{IN}+ V_{IN}−		**Signal Input** **(Input): Analog -** Analog Signal Input that must be applied differentially. The differential full-scale input is defined by pin 14 in the Normal mode and by the Full-Scale Voltage Adjust register in the Extended Control mode. See REGISTER DESCRIPTION.
22 23	ADCCLK_RST+ ADCCLK_RST-		**Sample Clock Reset** **(Input): LVDS -** A positive differential pulse on these pins is used to reset and synchronize the ADC sample clock when multiple ADCs are used. See MULTIPLE ADC SYNCHRONIZATION. When bit 14 in the Configuration Register (address 1h) is set to 1b, these differential ADCCLK_RST± pins are selected. See description for *pin 15*.
7	V_{CMO}		**Common Mode Voltage** **(Output): ANALOG -** The voltage output at this pin is required to be the common mode input voltage at V_{IN}+ and V_{IN}− when d.c. coupling is used. This pin should be grounded when a.c. coupling is used at the analog input. This pin is capable of sourcing or sinking 100µA and can drive a load up to 80 pF. See THE ANALOG INPUT.
31	V_{BG}		**Bandgap Output Voltage** **(Output): Analog -** Capable of 100 µA source/sink and can drive a load up to 80 pF.

Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
126	CalRun		**Calibration Running** **(Output): LVCMOS -** This pin is at a logic high while a calibration is running.
32	R_{EXT}		**External Bias Resistor Connection** **Analog -** Nominal value is 3.3k-Ohms (±0.1%) to ground. See Calibration.
34 35	Tdiode_P Tdiode_N		**Temperature Diode** **Analog -** Positive (Anode) and Negative (Cathode). These pins may be used for die temperature measurements, however no specified accuracy is implied or ensured. See Thermal Management.
72 71 70 69 68 67 66 65	D2<0> D2<1> D2<2> D2<3> D2<4> D2<5> D2<6> D2<7>		**Digital Data Output 2** **(Output): LVCMOS -** When the REN input is asserted and Two Port Enable, (TPE) is set to 1b in the Capture Buffer register (addr: Fh, bit: 12), half of the data is read from the capture buffer and presented at this port synchronous with each rising edge of Read CLK (RCLK). The data on this port is the earlier sample data vs. the Digital Data Output 1 data. When Two Port Enable is set to 0b in the Capture Buffer register, data output 2 is high-impedance.
75	DRDY2		**Data Ready 2** **(Output): LVCMOS -** DRDY is generated by RCLK and is synchronized to the output data. The use of this pin assists in eliminating the latency uncertainty between when Read CLK (RCLK) transitions and when data transitions at the output.
89 90 91 92 93 94 95 96	D1<0> D1<1> D1<2> D1<3> D1<4> D1<5> D1<6> D1<7>		**Digital Data Output 1** **(Output): LVCMOS -** When the REN input is asserted, data is read from the capture buffer and presented at this port synchronous with each rising edge of Read CLK (RCLK). When the Two Port Enable bit (TPE) is set to 1b in the Capture Buffer register (addr: Fh, bit: 12), half of the data is presented at this port. The data on this port is the later sample data vs. the Digital Data Output 2 data. When REN is deasserted, this output holds the data from the previous read. When Two Port Enable is set to 0b in the Capture Buffer register, this port presents all of the data from the Capture Buffer.
86	DRDY1		**Data Ready 1** **(Output): LVCMOS -** DRDY is generated by RCLK and is synchronized to the output data. The use of this pin assists in eliminating the latency uncertainty between when Read CLK (RCLK) transitions and when data transitions at the output.

Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
45	REN		**Read Enable** **(Input): LVCMOS -** A logic high on this input causes a byte of data to be read from the Capture Buffer with each RCLK cycle. This signal must not be asserted while the WEN is already asserted. See Coordinating Read Enable (REN) and Write Enable (WEN).
46	WEN		**Write Enable** **(Input): LVCMOS -** A logic high on this input causes a byte of data to be written into the Capture Buffer with each sample clock cycle. This signal may be asserted asynchronously as it is internally synchronized with the internal sample clock.
82	RCLK		**Read Clock** **(Input): LVCMOS -** Free running clock that is used to read data from the Capture Buffer. The parallel data at the output port and the EF flag are asserted synchronous with this clock.
81	RESET		**Reset** **(Input): LVCMOS -** A logic high at this input resets all Capture Buffer control logic in the chip.
79	WENSYNC		**Synchronized WEN** **(Output): LVCMOS -** The control input WEN is synchronized on-chip with the internal Sample Clock and is provided at this output.
80	OR		**Out Of Range** **(Output): LVCMOS -** A logic high on this pin indicates that the differential input is out of the linear range. This signal is asserted if the input signal has gone out of range at any time during the data capture operation. This pin is cleared after the Capture Buffer is read or after asserting the RESET pin.
115	FF		**Buffer Full Flag** **(Output): LVCMOS -** This signal is asserted synchronous with the clock when the capture buffer is full. If the WEN input remains asserted, the next CLK will cause an overflow, whereby the pointer will wrap around and begin overwriting the old data if the Auto Stop Write (ASW) bit is set to 0b in the Capture Buffer Control register. This signal is deasserted when a read cycle is initiated or a RESET is issued because the data buffer is no longer "full".
116	EF		**Buffer Empty Flag** **(Output): LVCMOS -** This signal is asserted synchronous with the RCLK signal when the Capture Buffer is empty. It is deasserted when a write cycle is initiated and the data buffer is no longer "empty".
2, 5, 8, 13, 16, 17, 20, 25, 28, 33, 128	V_A		**Analog power supply pins** **(Power)** - Bypass these pins to ground.
40, 51, 62, 73, 88, 99, 110, 121	V_{DR}		**Output Driver power supply pins** **(Power) -** Bypass these pins to DR GND.
1, 6, 9, 12, 21, 24, 27	GND		**(Gnd) -** Ground return for V_A.
42, 53, 64, 74, 87, 97, 108, 119	DR GND		**(Gnd) -** Ground return for V_{DR}.

Pin Descriptions and Equivalent Circuits (continued)

Pin Functions			
Pin No.	**Symbol**	**Equivalent Circuit**	**Description**
29, 36, 37, 38, 39, 41, 43, 44, 47, 48, 49, 50, 52, 54, 55, 56, 57, 58, 59, 60, 61, 63, 76, 77, 78, 83, 84, 85, 98, 100, 101, 102, 103, 104, 105, 106, 107, 109, 111, 112, 113, 114, 117, 118, 120, 122, 123, 124, 125	NC		**No Connection** Make no connection to these pins.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1) (2) (3)

Analog Supply Voltage (V_A)		2.2V
V_{DR}		0V to (V_A + 300mV)
Voltage on Any Input Pin (Except V_{IN}+, V_{IN}-)		−0.15V to (V_A + 0.15V)
Voltage on V_{IN}+, V_{IN}- (Maintaining Common Mode)		-0.15V to 2.5V
Ground Difference (|GND - DR GND|)		0V to 100 mV
Input Current at Any Pin (4)		±25 mA
Package Input Current (4)		±50 mA
Power Dissipation at $T_A \le 85°C$		2.3 W
ESD Susceptibility (5)	Human Body Model	2500V
	Machine Model	250V
Storage Temperature		−65°C to +150°C

(1) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.
(2) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply limits (that is, less than GND or greater than V_A), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two. This limit is not placed upon the power and ground pins.
(5) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 220 pF discharged through ZERO Ohms.

Operating Ratings (1) (2)

Ambient Temperature Range	−40°C ≤ T_A ≤ +85°C
Supply Voltage (V_A)	+1.8V to +2.0V
Driver Supply Voltage (V_{DR})	+1.8V to V_A
Analog Input Common Mode Voltage	V_{CMO} ±50mV
V_{IN}+, V_{IN}- Voltage Range (Maintaining Common Mode)	0V to 2.15V (100% duty cycle) 0V to 2.5V (10% duty cycle)
Ground Difference (|GND - DR GND|)	0V
CLK Pins Voltage Range	0V to V_A
Differential CLK Amplitude	0.4V_{P-P} to 2.0V_{P-P}

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. There is no specification of operation at the Absolute Maximum Ratings. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see Converter Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = DR GND = 0V, unless otherwise specified.

Package Thermal Resistance (1) (2)

Package	θ_{JA}	$\theta_{JC\ (Top\ of\ Package)}$	$\theta_{J\text{-}PAD\ (Thermal\ Pad)}$
128-Lead Exposed Pad HLQFP	26°C / W	10°C / W	2.8°C / W

(1) *Soldering process must comply with Reflow Temperature Profile specifications. Refer to* www.ti.com/packaging.
(2) Reflow temperature profiles are different for lead-free and non-lead-free packages.

Converter Electrical Characteristics (1) (2)

The following specifications apply after calibration for V_A = V_{DR} = 1.9V, V_{IN} FSR (a.c. coupled) = differential 810mV_{P-P}, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at 0.4V_{P-P} with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for T_A = T_{MIN} to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical (3)	Limits (3)	Units (Limits)
STATIC CONVERTER CHARACTERISTICS					
INL	Integral Non-Linearity (Best fit)	DC Coupled, 1MHz Sine Wave Over Ranged	±0.35	**±0.9**	LSB (max)
DNL	Differential Non-Linearity	DC Coupled, 1MHz Sine Wave Over Ranged	±0.20	**±0.6**	LSB (max)
	Resolution with No Missing Codes			**8**	Bits
V_{OFF}	Offset Error		-0.10		LSB
V_{OFF}_ADJ	Input Offset Adjustment Range	Extended Control Mode	±45		mV
PFSE	Positive Full-Scale Error (4)		−2.7	**±25**	mV (max)
NFSE	Negative Full-Scale Error (4)		−1.6	**±25**	mV (max)
FS_ADJ	Full-Scale Adjustment Range	Extended Control Mode	±20	**±15**	%FS
DYNAMIC CONVERTER CHARACTERISTICS					
FPBW	Full Power Bandwidth		3		GHz

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device. See Figure 2
(2) To ensure accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.
(3) Typical figures are at T_A = 25°C, and represent most likely parametric norms. Test limits are ensured to AOQL (Average Outgoing Quality Level).
(4) Calculation of Full-Scale Error for this device assumes that the actual reference voltage is exactly its nominal value. Full-Scale Error for this device, therefore, is a combination of Full-Scale Error and Reference Voltage Error. See Figure 3. For relationship between Gain Error and Full-Scale Error, see Specification Definitions for Gain Error.

Converter Electrical Characteristics[1][2] (continued)

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$, V_{IN} FSR (a.c. coupled) = differential $810mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at $0.4V_{P-P}$ with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical[3]	Limits[3]	Units (Limits)
	Code Error Rate		10^{-18}		Errors/ Sample
	Gain Flatness	0.0 to -1.0 dBFS	50 to 950		MHz
ENOB	Effective Number of Bits	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	7.2	**6.7**	Bits (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	7.1	**6.5**	Bits (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	6.4		Bits
SINAD	Signal-to-Noise Plus Distortion Ratio	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	45.1	**41.8**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	44.5	**41.0**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	40.3		dB
SNR	Signal-to-Noise Ratio	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	45.3	**42.5**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	44.9	**42**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	42.4		dB
THD	Total Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	-57	**-50**	dB (max)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	-54.8	**-48**	dB (max)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	-44.3		dB
2nd Harm	Second Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	-68		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	-65		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	-45		dB
3rd Harm	Third Harmonic Distortion	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	-63		dB
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	-57		dB
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	-51		dB
SFDR	Spurious-Free dynamic Range	f_{IN} = 373 MHz, V_{IN} = FSR − 0.5 dB	55.4	**47**	dB (min)
		f_{IN} = 748 MHz, V_{IN} = FSR − 0.5 dB	54.0	**46.5**	dB (min)
		f_{IN} = 1498 MHz, V_{IN} = FSR − 0.5 dB	45.3		dB
IMD	Intermodulation Distortion	f_{IN1} = 749.084 MHz, V_{IN} = FSR − 7 dB, f_{IN2} = 756.042 MHz, V_{IN} = FSR − 7 dB	-52		dBFS

Converter Electrical Characteristics[1][2] (continued)

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$, V_{IN} FSR (a.c. coupled) = differential 810mV_{P-P}, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at 0.4V_{P-P} with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical[3]	Limits[3]	Units (Limits)
ANALOG INPUT AND REFERENCE CHARACTERISTICS					
V_{IN}	Full Scale Analog Differential Input Range	FSR pin 14 Low	600	**550**	mV_{P-P} (min)
				650	mV_{P-P} (max)
		FSR pin 14 High	810	**740**	mV_{P-P} (min)
				880	mV_{P-P} (max)
V_{CMI}	Analog Input Common Mode Voltage		V_{CMO}	**V_{CMO} − 50** **V_{CMO} + 50**	mV (min) mV (max)
C_{IN}	Analog Input Capacitance[5]	Differential	0.8		pF
		Each input pin to ground	2.2		pF
R_{IN}	Differential Input Resistance		100	**95** **103**	Ω (min) Ω (max)
ANALOG OUTPUT CHARACTERISTICS					
V_{CMO}	Common Mode Output Voltage	I_{CMO} = ±100 µA	1.26	**0.95** **1.45**	V (min) V (max)
V_{CMO_LVL}	V_{CMO} input threshold to set DC Coupling mode	V_A = 1.8V	0.60		V
		V_A = 2.0V	0.66		V
TC V_{CMO}	Common Mode Output Voltage Temperature Coefficient	T_A = −40°C to +85°C	118		ppm/°C
C_{LOAD} V_{CMO}	Maximum V_{CMO} load Capacitance			**80**	pF
V_{BG}	Bandgap Reference Output Voltage	I_{BG} = ±100 µA	1.26	**1.20** **1.33**	V (min) V (max)
TC V_{BG}	Bandgap Reference Voltage Temperature Coefficient	T_A = −40°C to +85°C, I_{BG} = ±100 µA	28		ppm/°C
C_{LOAD} V_{BG}	Maximum Bandgap Reference load Capacitance			**80**	pF
TEMPERATURE DIODE CHARACTERISTICS					
ΔV_{BE}	Temperature Diode Voltage	192 µA vs. 12 µA, T_J = 25°C	71.23		mV
		192 µA vs. 12 µA, T_J = 85°C	85.54		mV
LVDS INPUT CHARACTERISTICS					
V_{ID}	Differential Clock Input Level	Sine Wave Clock	0.5	**0.4** **0.7**	V_{P-P} (min) V_{P-P} (max)
		Square Wave Clock	0.5	**0.4** **0.7**	V_{P-P} (min) V_{P-P} (max)
I_I	Input Current	V_{IN} = 0 or V_{IN} = V_A	±1		µA
C_{IN}	Input Capacitance[5]	Differential	0.02		pF
		Each input to ground	1.5		pF

(5) The analog and clock input capacitances include packaging capacitance values of 0.7 pF differential and 1 pF each input pin to ground, which are isolated from the die capacitance by lead and bond wire inductances.

Converter Electrical Characteristics[1][2] (continued)

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$, V_{IN} FSR (a.c. coupled) = differential $810mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at $0.4V_{P-P}$ with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical[3]	Limits[3]	Units (Limits)
LVCMOS INPUT CHARACTERISTICS					
V_{IH}	Logic High Input Voltage	ADCCLK_RST, PD, CAL		**0.69 x V_A**	V (min)
		OutEdge, FSR, CalDly		**0.79 x V_A**	V (min)
V_{IL}	Logic Low Input Voltage	All LVCMOS Inputs		**0.28 x V_A**	V (max)
I_{IH}	Logic High Input Current	ADCCLK_RST, CAL, PD, CalDly	1		µA
		FSR/ECE	30		µA
I_{IL}	Logic Low Input Current	ADCCLK_RST, CAL, PD, CalDly	1		µA
		FSR/ECE	30		µA
C_{IN}	Input Capacitance[6]	Each input to ground	1.2		pF
LVCMOS OUTPUT CHARACTERISTICS					
V_{OH}	CMOS High level output	I_{OH} = -400uA	1.65	**1.5**	V (min)
V_{OL}	CMOS Low level output	I_{OH} = 400uA	0.15	**0.3**	V (max)
POWER SUPPLY CHARACTERISTICS					
I_A	Analog Supply Current	Full Power Capture Mode WEN = High, REN =PD = Low	723	**800**	mA (max)
		Power Down Mode WEN = Low, REN = PD = High	2.4		mA
I_{DR}	Output Driver Supply Current	Full Power Capture Mode WEN = High, REN =PD = Low	135	**180**	mA (max)
		Power Down Mode WEN = Low, REN = PD = High	10.8		mA
P_D	Power Consumption	Full Power Capture Mode WEN = High, REN =PD = Low	1.6	**1.9**	W (max)
		Power Down Mode WEN = Low, REN = PD = High	25		mW
PSRR1	D.C. Power Supply Rejection Ratio	Change in Offset Error with change in V_A from 1.8V to 2.0V	70		dB
PSRR2	A.C. Power Supply Rejection Ratio	248 MHz, $100mV_{P-P}$ riding on V_A	50		dB

(6) The digital control pin capacitances are die capacitances only. Additional package capacitance of 1.6 pF each pin to ground are isolated from the die capacitances by lead and bond wire inductances.

Converter Electrical Characteristics[1][2] (continued)

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$, V_{IN} FSR (a.c. coupled) = differential $810mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at $0.4V_{P-P}$ with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical[3]	Limits[3]	Units (Limits)
AC ELECTRICAL CHARACTERISTICS - Sample Clock					
f_{CLK1}	Maximum Input Clock Frequency	Sample rate is 2x clock input		**1.5**	GHz (min)
f_{CLK2}	Minimum Input Clock Frequency	Sample rate is 2x clock input	500		MHz
t_{CYC}	Input Clock Duty Cycle	500MHz ≤ Input clock frequency ≤ 1.5 GHz[7]	50	**20** **80**	% (min) % (max)
t_{LC}	Input Clock Low Time	See[8]	333	**133**	ps (min)
t_{HC}	Input Clock High Time	See[8]	333	**133**	ps (min)
t_{AD}	Sample (Aperture) Delay	Input CLK transition to Acquisition of Data	1.4		ns
t_{AJ}	Aperture Jitter		0.55		ps rms
AC ELECTRICAL CHARACTERISTICS - Capture Buffer Signals					
f_{RCLK}	Maximum Capture Buffer Read Clock Frequency		200		MHz
t_{LHT}	Low to High Transition Time	10% to 90%	250		ps
t_{HLT}	High to Low Transition Time	10% to 90%	250		ps
t_{DWS1}	Delay WENSYNC	Delay after 3 Write Clock Cycles	7.0		ns
t_{DWS2}	Delay WENSYNC	Delay after FF assertion	-1.3		ns
t_{HWEN}	Minimum Hold Time WEN	Hold Time after WENSYNC deassertion	-5.0	**0**	ns (min)
T_{ASWEN}	Minimum Assertion Delay WEN	RCLK cycle delay after deassertion of REN	0	**1**	RCLK Cyc. (min)
t_{DFF}	Delay Full Flag	Delay after REN assertion, RCLK = 100 MHz	7.3		ns
		Delay after REN assertion, RCLK = 200 MHz	5.0		ns
t_{DEF1}	Delay Empty Flag	Delay after last DRDY pulse, RCLK = 200 MHz	0		ns
t_{DEF2}	Delay Empty Flag	Delay after RESET	2.0		ns
t_{DEF3}	Delay Empty Flag	Delay after WENSYNC assertion	9.5		ns
t_{SREN}	Minimum Setup Time REN	Setup Time before rising edge of RCLK	0.2	**0.3**	ns (min)
t_{HREN}	Minimum Hold Time REN	Hold Time after last DRDY pulse or positive edge of RESET	-5	**0**	ns (min)
t_{DDRDY}	Delay RCLK to DRDY	RCLK to DRDY Delay, RCLK = 100 MHz or 200 MHz	2.7	**1.8**	ns (min)
				4.0	ns (max)
t_{SKEW}	Skew DRDY to Data	For SDR and DDR 0º modes.	0	**±200**	ps (max)
t_{SO}	Setup Time Data Output	Data Output to DRDY For DDR 90º mode	5		ns
t_{HO}	Hold Time Data Output	DRDY to Data Output For DDR 90º mode	5		ns

(7) This parameter is ensured by design and/or characterization and is not tested in production.
(8) This parameter is ensured by design and is not tested in production.

Converter Electrical Characteristics[1][2] (continued)

The following specifications apply after calibration for $V_A = V_{DR} = 1.9V$, V_{IN} FSR (a.c. coupled) = differential $810mV_{P-P}$, C_L = 10 pF, Differential a.c. coupled sine wave Input Clock, f_{CLK} = 1.5 GHz at $0.4V_{P-P}$ with 50% duty cycle, Duty Cycle Stabilizer enabled, RCLK = 100 MHz, V_{BG} = Floating, Non-Extended Control Mode, SDR Mode, R_{EXT} = 3300Ω ±0.1%, Analog Signal Source Impedance = 100Ω Differential, after calibration. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX}.** All other limits T_A = 25°C, unless otherwise noted.

Parameter		Test Conditions	Typical[3]	Limits[3]	Units (Limits)
AC ELECTRICAL CHARACTERISTICS - Serial Interface					
f_{SCLK}	Serial Clock Frequency		67		MHz
t_{SSU}	Data to Serial Clock Rising Setup Time		2.5		ns (min)
t_{SH}	Data to Serial Clock Rising Hold Time		1		ns (min)
t_{SCS}	CS to Serial Clock Rising Setup Time		2.5		ns
t_{HCS}	$\overline{CS}$ to Serial Clock Falling Hold Time		1.5		ns
	Serial Clock Low Time			**6**	ns (min)
	Serial Clock High Time			**6**	ns (min)
AC ELECTRICAL CHARACTERISTICS - General Signals					
t_{SR}	Setup Time ADCCLK_RST±	Differential ADCCLK_RST	90		ps
t_{HR}	Hold Time ADCCLK_RST±	Differential ADCCLK_RST	30		ps
t_{PWR}	Pulse Width ADCCLK_RST±	See[9]		**4**	CLK± Cyc. (min)
t_{WU}	PD low to Rated Accuracy Conversion (Wake-Up Time)		1		µs
t_{CAL}	Calibration Cycle Time		1.4×10^5		CLK± Cyc.
t_{CAL_L}	CAL Pin Low Time	See[9] and Figure 6		**80**	CLK± Cyc. (min)
t_{CAL_H}	CAL Pin High Time	See[9] and Figure 6		**80**	CLK± Cyc. (min)
t_{CalDly}	Calibration delay CalDly = Low	See[9], Calibration and Figure 6		$\mathbf{2^{25}}$	CLK± Cyc. (max)
	Calibration delay CalDly = High	See[9], Calibration and Figure 6		$\mathbf{2^{31}}$	CLK± Cyc. (max)

(9) This parameter is ensured by design and is not tested in production.

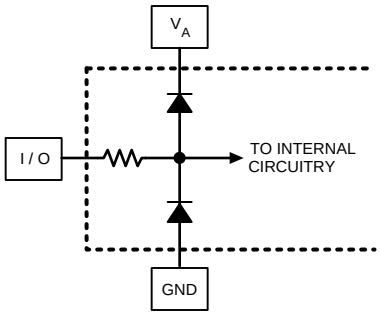


Figure 2.

SPECIFICATION DEFINITIONS

APERTURE (SAMPLING) DELAY is the amount of delay, measured from the sample edge of the Clock input, after which the signal present at the input pin is sampled inside the device.

APERTURE JITTER (t_{AJ}) is the variation in aperture delay from sample to sample. Aperture jitter shows up as input noise.

CLOCK DUTY CYCLE is the ratio of the clock wave form logic high to the total time of one clock period.

CODE ERROR RATE (C.E.R.) is the probability of error and is defined as the probable number of errors per unit of time divided by the number of words seen in that amount of time. A Code Error Rate of 10^{-18} corresponds to a statistical error in one conversion about every four (4) years.

COMMON MODE VOLTAGE is the d.c. potential that is common to both pins of a differential pair. For a voltage to be a common mode one, the signal departure from this d.c. common mode voltage at any given instant must be the same for each of the pins, but in opposite directions from each other.

DIFFERENTIAL NON-LINEARITY (DNL) is the maximum deviation from the ideal step size of 1 LSB. Measured at 3 Gsps with a sine wave input.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as (SINAD − 1.76) / 6.02 and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH (FPBW) is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It can be calculated from Offset and Full-Scale Errors:

Pos. Gain Error = Offset Error − Pos. Full-Scale Error (1)

Neg. Gain Error = − (Offset Error − Neg. Full-Scale Error) (2)

Gain Error = Neg. Full-Scale Error − Pos. Full-Scale Error = Pos. Gain Error + Neg. Gain Error (3)

INTEGRAL NON-LINEARITY (INL) is the maximum departure of the transfer curve from a straight line through the input to output transfer function. The deviation of any given code from this straight line is measured from the center of that code value. The best fit method is used.

INTERMODULATION DISTORTION (IMD) is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the power in one of the original frequencies. IMD is usually expressed in dBFS.

LSB (LEAST SIGNIFICANT BIT) is the bit that has the smallest value or weight of all bits. This value is

$$V_{FS} / 2^n \quad (4)$$

where V_{FS} is the differential full-scale amplitude of V_{IN} as set by the FSR input (pin-14) and "n" is the ADC resolution in bits, which is 8 for the ADC08B3000.

MISSING CODES are those output codes that are skipped and will never appear at the ADC outputs. These codes cannot be reached with any input value.

MSB (MOST SIGNIFICANT BIT) is the bit that has the largest value or weight. Its value is one half of full scale.

NEGATIVE FULL-SCALE ERROR (NFSE) is a measure of how far the first code transition is from the ideal 1/2 LSB above a differential $-V_{IN} / 2$. For the ADC08B3000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

OFFSET ERROR (V_{OFF}) is a measure of how far the mid-scale point is from the ideal zero voltage differential input.

Offset Error = Actual Input causing average of 8k samples to result in an average code of 128.

OVER-RANGE RECOVERY TIME is the time required after the differential input voltages goes from ±1.2V to 0V for the converter to recover and make a conversion with its rated accuracy.

POSITIVE FULL-SCALE ERROR (PFSE) is a measure of how far the last code transition is from the ideal 1-1/2 LSB below a differential $+V_{IN}$ / 2. For the ADC08B3000 the reference voltage is assumed to be ideal, so this error is a combination of full-scale error and reference voltage error.

POWER SUPPLY REJECTION RATIO (PSRR) can be one of two specifications. PSRR1 (DC PSRR) is the ratio of the change in full-scale error that results from a power supply voltage change from 1.8V to 2.0V. PSRR2 (AC PSRR) is a measure of how well an a.c. signal riding upon the power supply is rejected from the output and is measured with a 248 MHz, 100 mV_{P-P} signal riding upon the power supply. It is the ratio of the output amplitude of that signal at the output to its amplitude on the power supply pin. PSRR is expressed in dB.

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of the sum of all other spectral components below one-half the sample frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD) is the ratio, expressed in dB, of the rms value of the input signal at the output to the rms value of all of the other spectral components below half the input clock frequency, including harmonics but excluding d.c.

SPURIOUS-FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the rms values of the input signal at the output and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input, excluding d.c.

TOTAL HARMONIC DISTORTION (THD) is the ratio expressed in dB, of the rms total of the first nine harmonic levels at the output to the level of the fundamental at the output. THD is calculated as

$$\text{THD} = 20 \times \log \sqrt{\frac{A_{f2}^2 + \ldots + A_{f10}^2}{A_{f1}^2}} \tag{5}$$

where A_{f1} is the RMS power of the fundamental (output) frequency and A_{f2} through A_{f10} are the RMS power of the first 9 harmonic frequencies in the output spectrum.

– Second Harmonic Distortion (2nd Harm) is the difference, expressed in dB, between the RMS power in the input frequency seen at the output and the power in its 2nd harmonic level at the output.

– Third Harmonic Distortion (3rd Harm) is the difference expressed in dB between the RMS power in the input frequency seen at the output and the power in its 3rd harmonic level at the output.

Transfer Characteristic

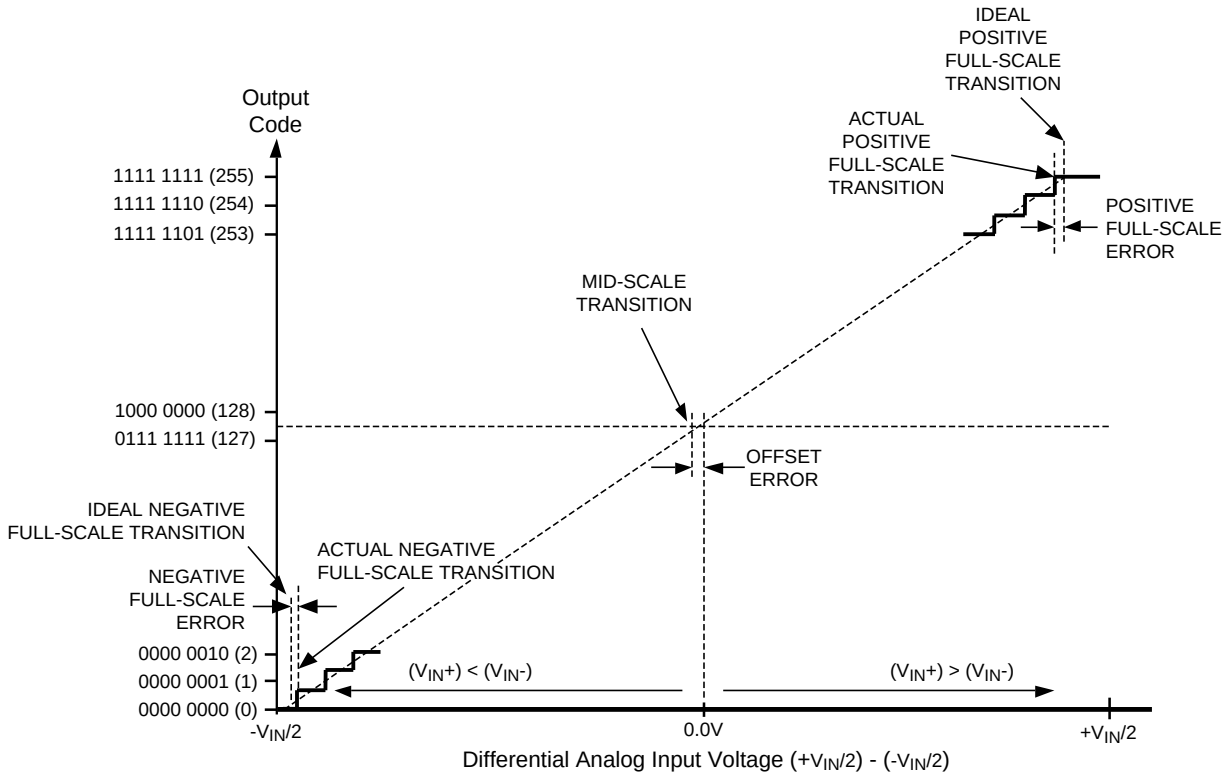


Figure 3. Input / Output Transfer Characteristic

TEST CIRCUIT DIAGRAMS

Timing Diagrams

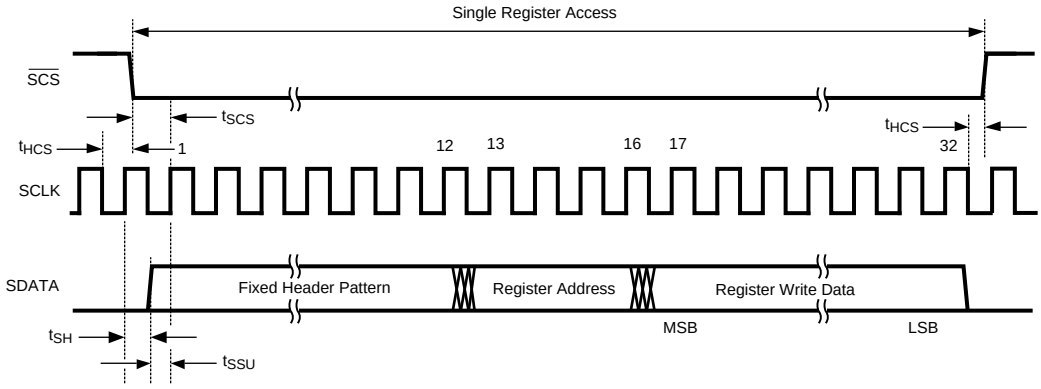


Figure 4. Serial Interface Timing

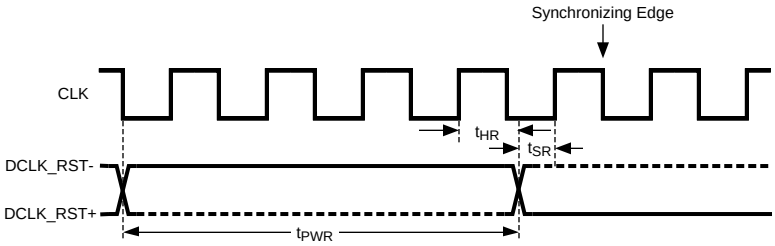


Figure 5. Clock Reset Timing

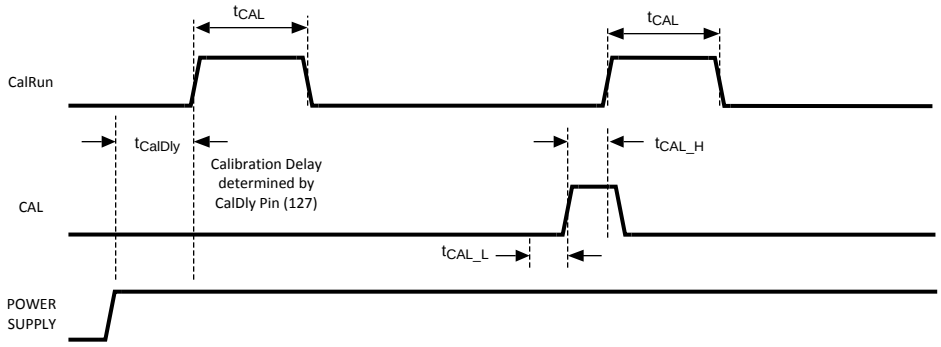


Figure 6. Self Calibration and On-Command Calibration Timing

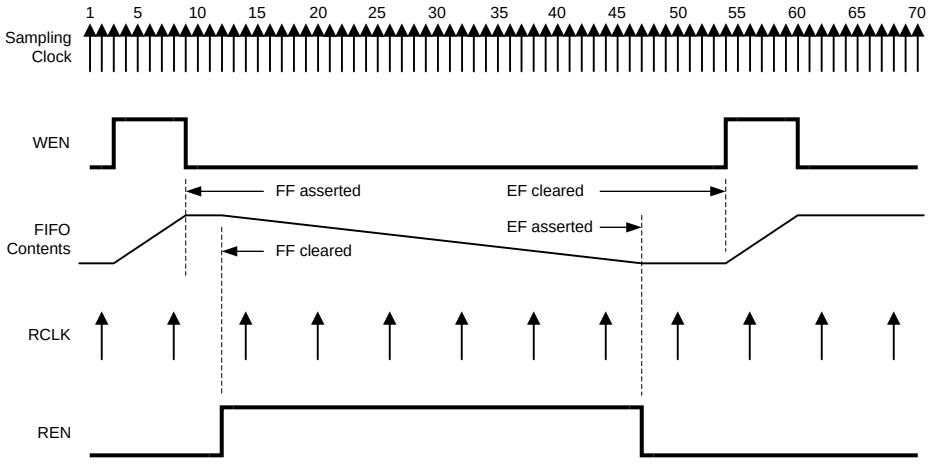


Figure 7. Capture Buffer Read Operation

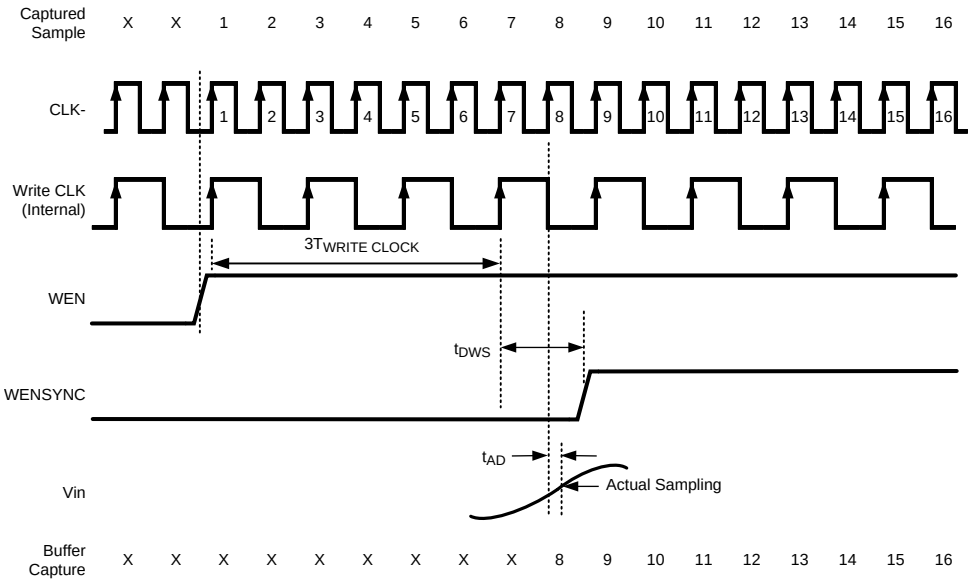


Figure 8. Capture Buffer Write Enable Timing - 7 Input Clock Cycles

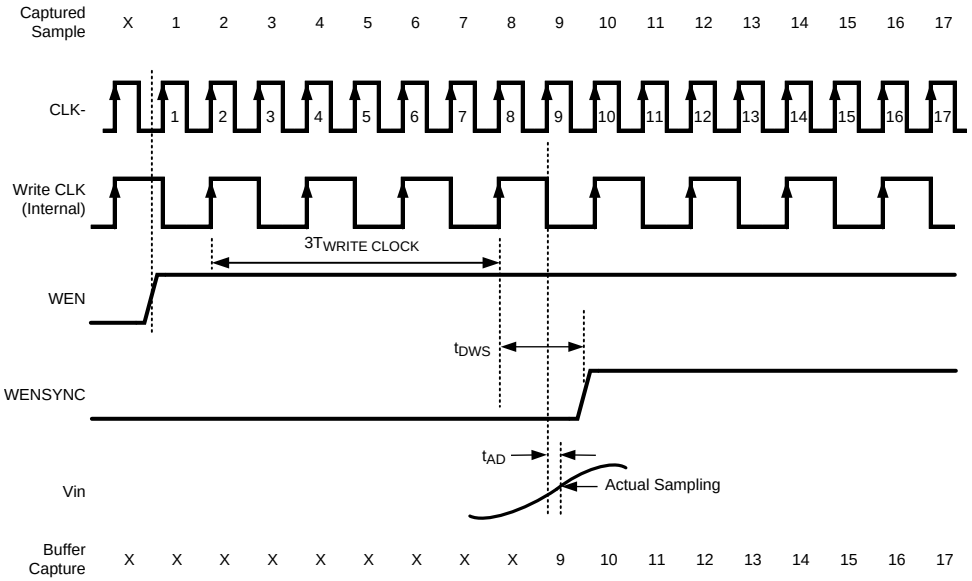


Figure 9. Capture Buffer Write Enable Timing - 8 Input Clock Cycles

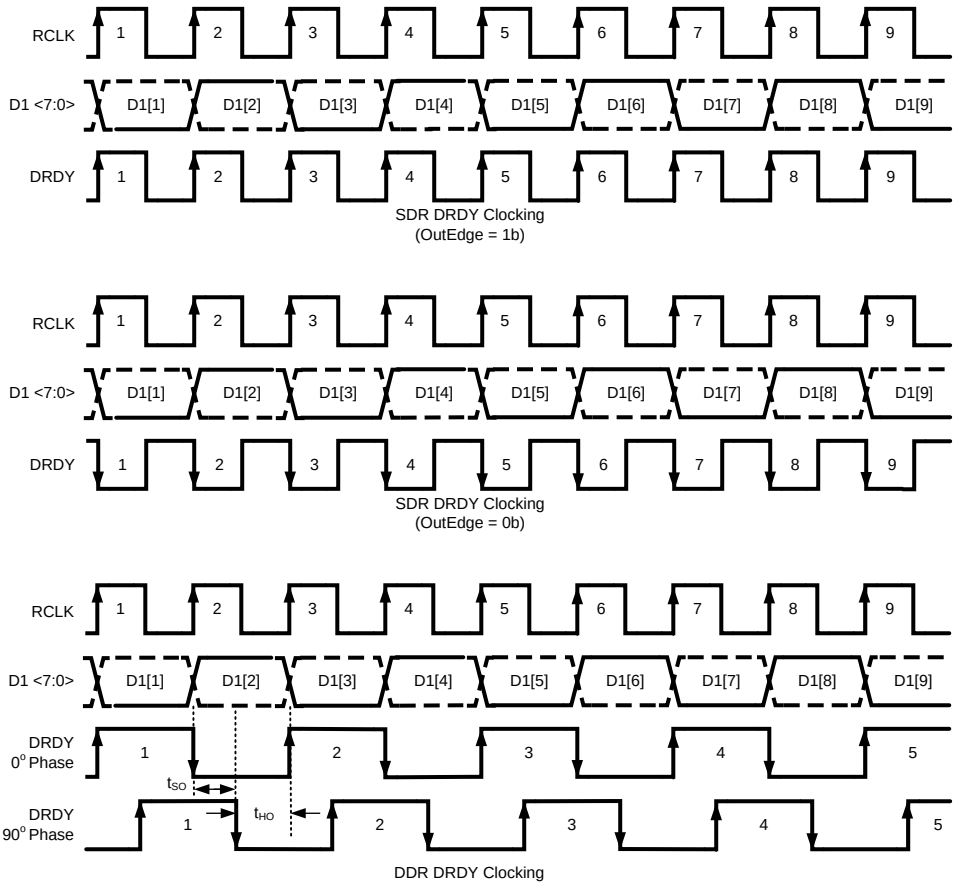
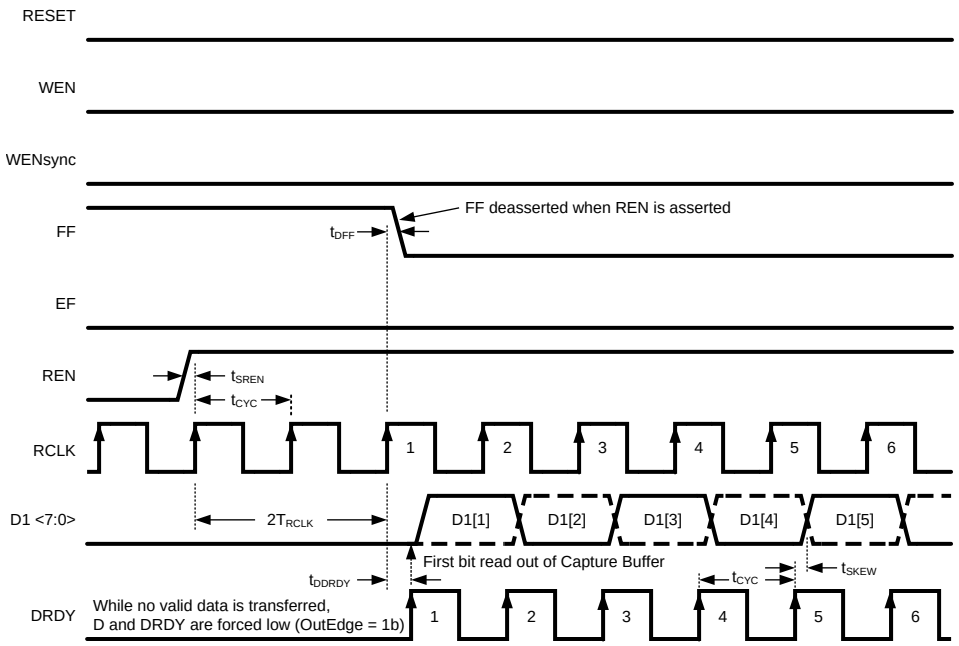
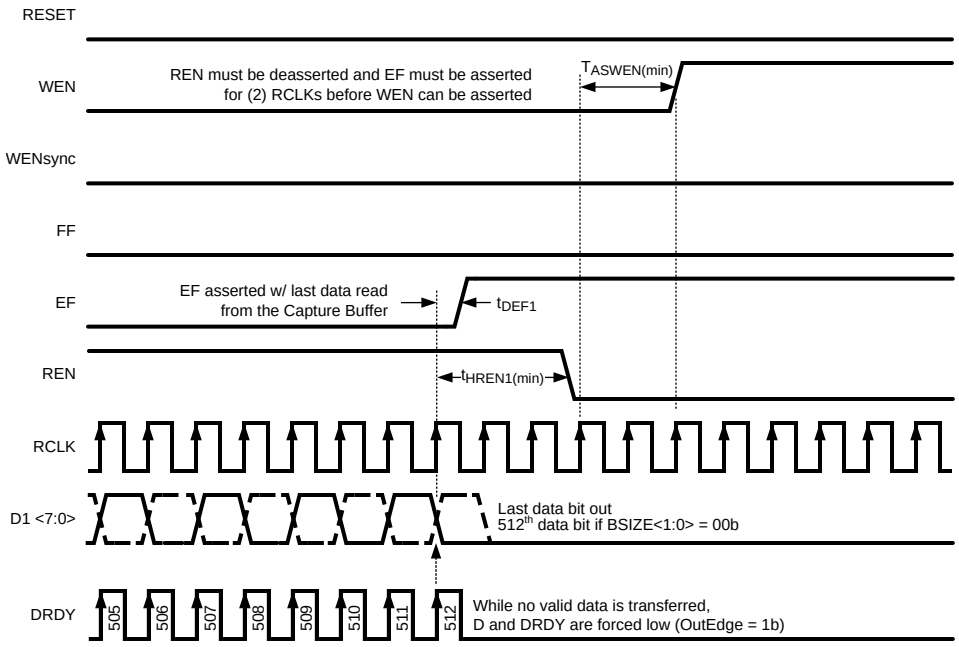


Figure 10. Capture Buffer DRDY Timing - SDR/DDR



A. For (OutEdge = 0b), all activity occurs on falling edge of DRDY.

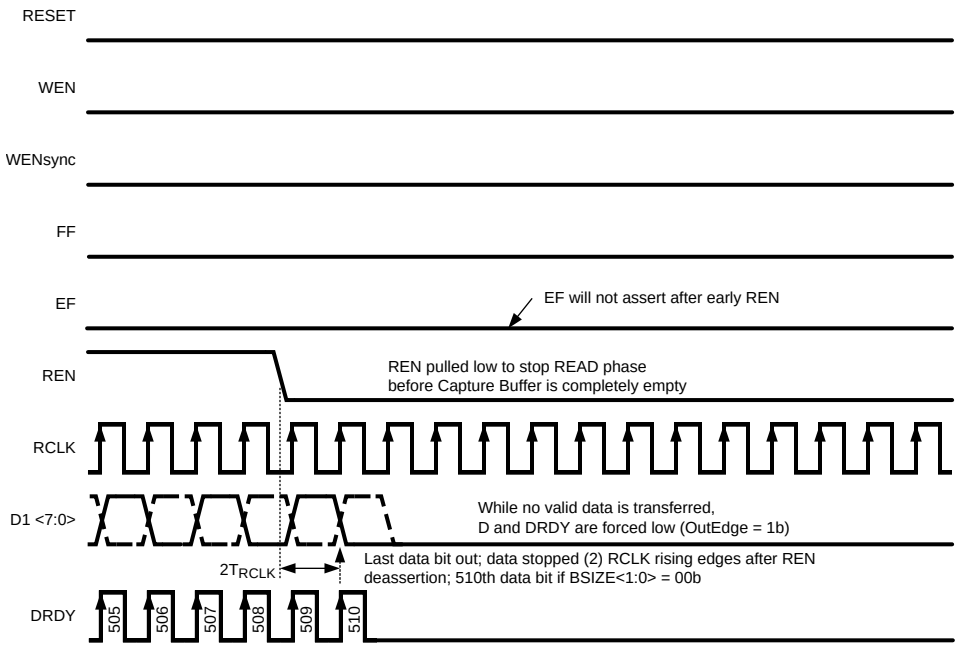
Figure 11. Capture Buffer Beginning of READ Phase (OutEdge = 1b)



A. For (OutEdge = 0b), all activity occurs on falling edge of DRDY.

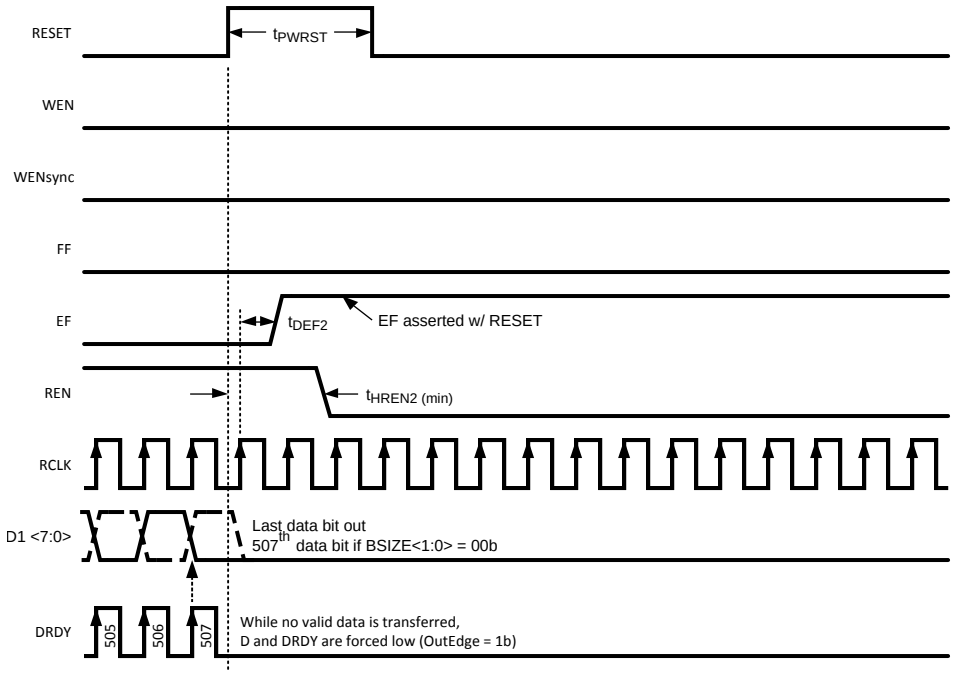
B. t_{HREN}: REN is internally latched on the 3rd rising edge of RCLK (see Figure 12)

Figure 12. Capture Buffer End of READ Phase (OutEdge = 1b)



A. For (OutEdge = 0b), all activity occurs on falling edge of DRDY.

Figure 13. Capture Buffer Early REN Deassertion on READ Phase (OutEdge = 1b)



A. For (OutEdge = 0b), all activity occurs on falling edge of DRDY.

Figure 14. Capture Buffer RESET on READ Phase (OutEdge = 1b)

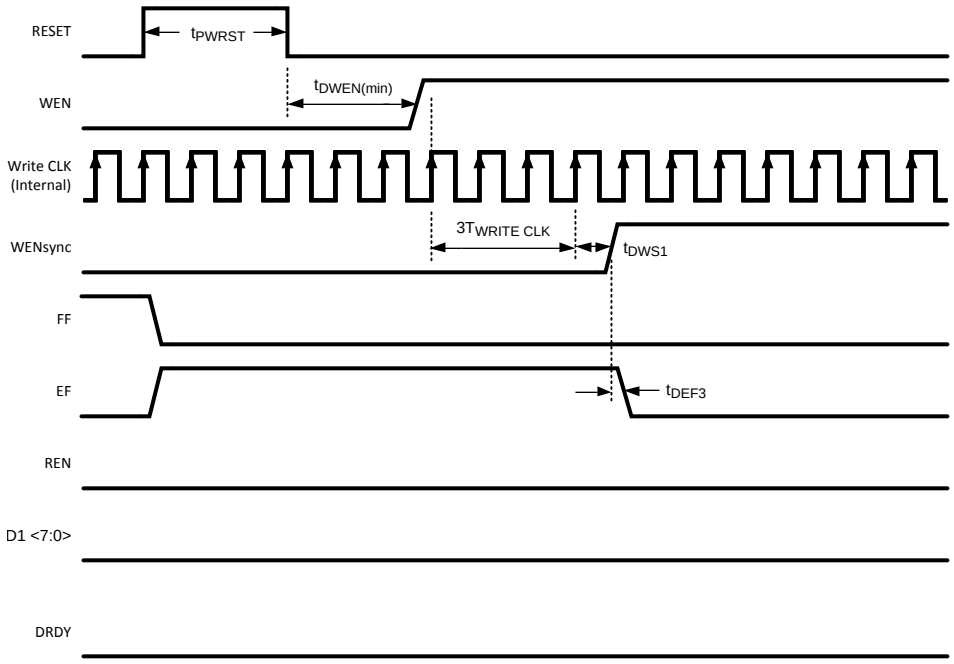
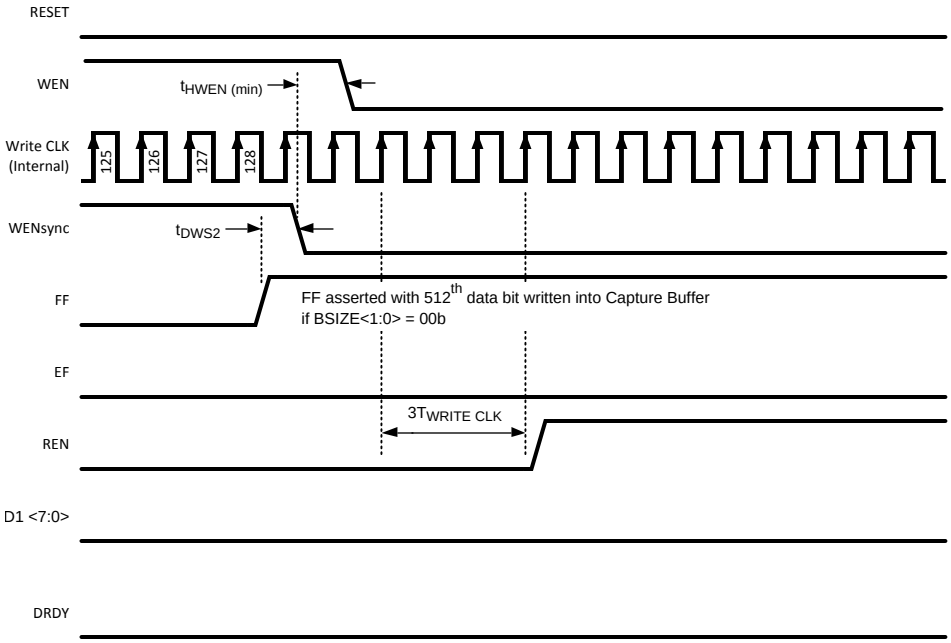


Figure 15. Capture Buffer Beginning of WRITE Phase



A. t_{HWEN}: WEN is internally latched on the 4th rising edge of the internal write clock (see Figure 16)

Figure 16. Capture Buffer End of WRITE Phase (ASW = 1b)

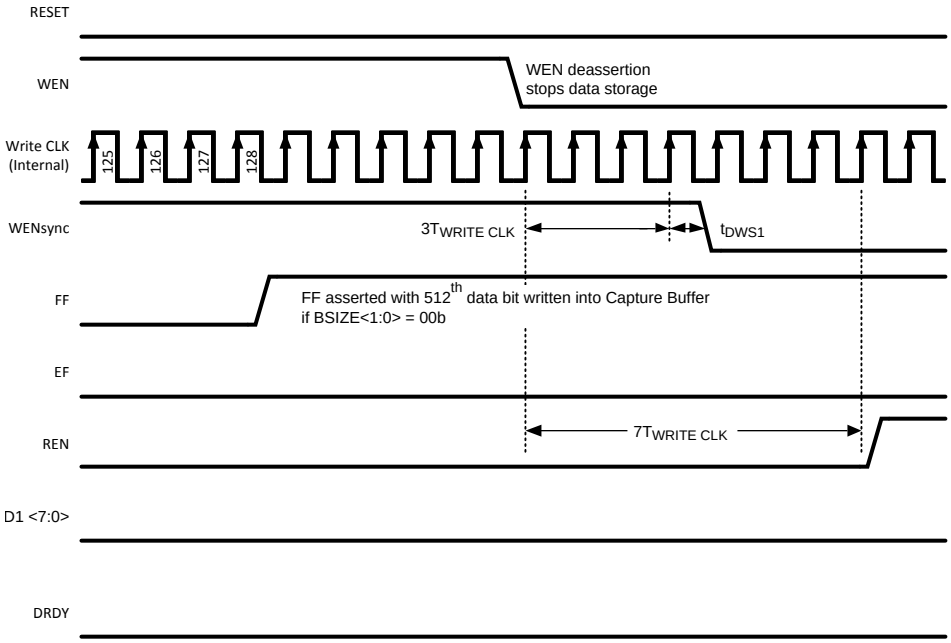


Figure 17. Capture Buffer End of WRITE Phase (ASW = 0b)

Typical Performance Characteristics

V_A=V_{DR}=1.9V, f_{CLK}=1500 MHz (i.e., Sample Rate = 3 Gsps), f_{IN}=373 MHz, T_A=25°C unless otherwise stated.

DNL vs. TEMPERATURE

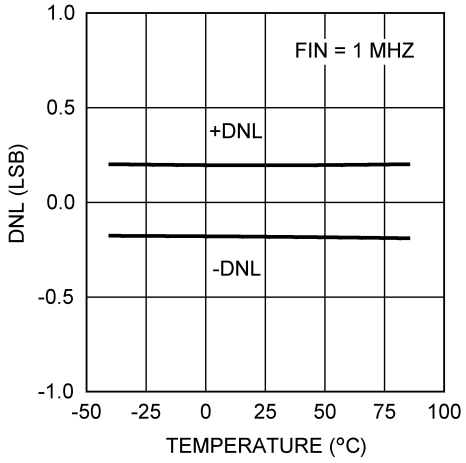


Figure 18.

INL vs. TEMPERATURE

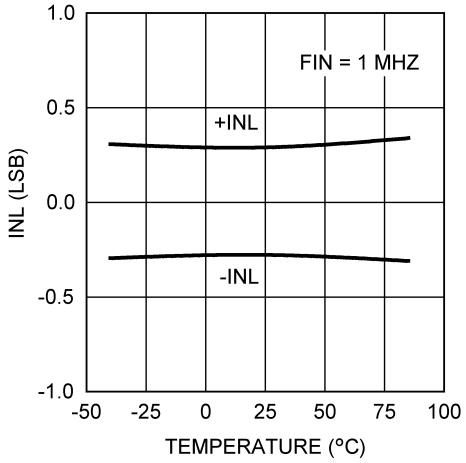


Figure 19.

DNL vs. CODE

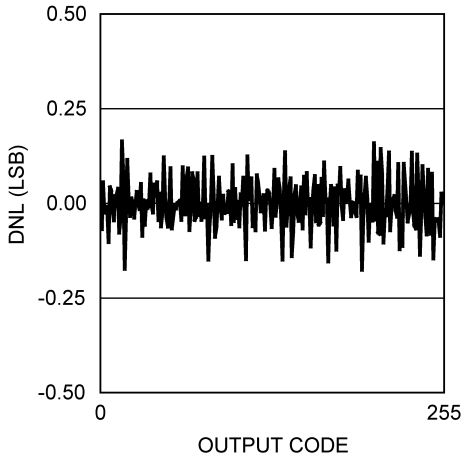


Figure 20.

INL vs. CODE

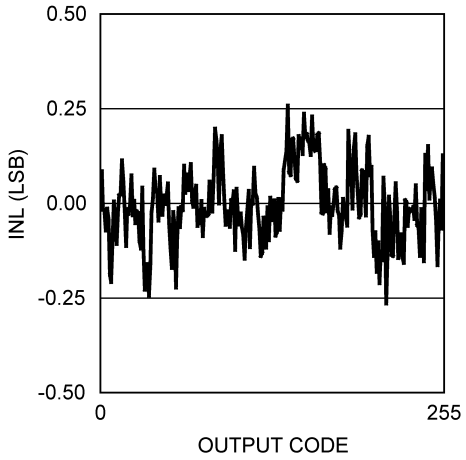


Figure 21.

POWER CONSUMPTION vs. SAMPLE RATE

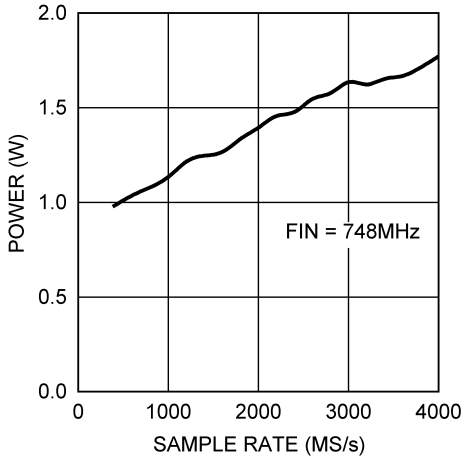


Figure 22.

ENOB vs. TEMPERATURE

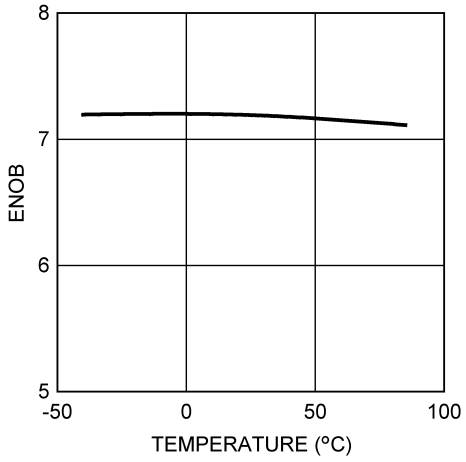


Figure 23.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, f_{CLK}=1500 MHz (i.e., Sample Rate = 3 Gsps), f_{IN}=373 MHz, T_A=25°C unless otherwise stated.

ENOB vs. SUPPLY VOLTAGE

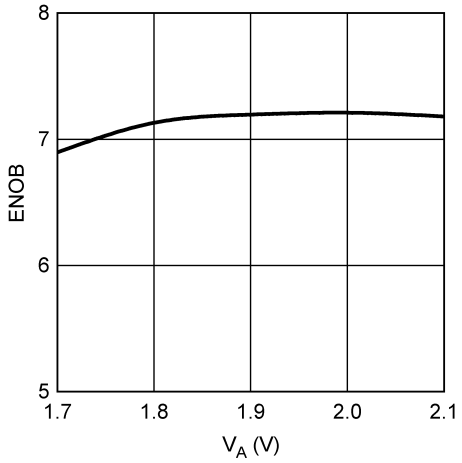


Figure 24.

ENOB vs. SAMPLE RATE

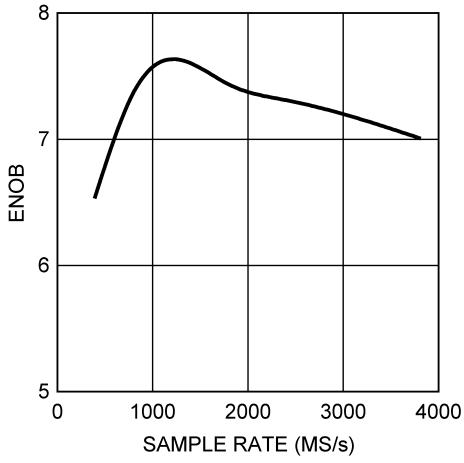


Figure 25.

ENOB vs. INPUT FREQUENCY

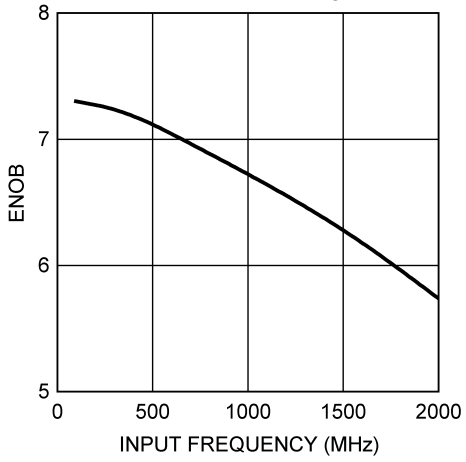


Figure 26.

SNR vs. TEMPERATURE

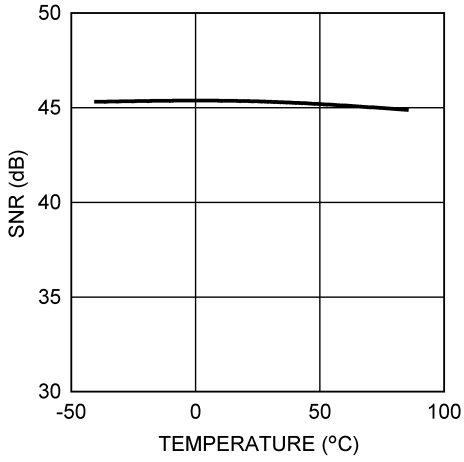


Figure 27.

SNR vs. SUPPLY VOLTAGE

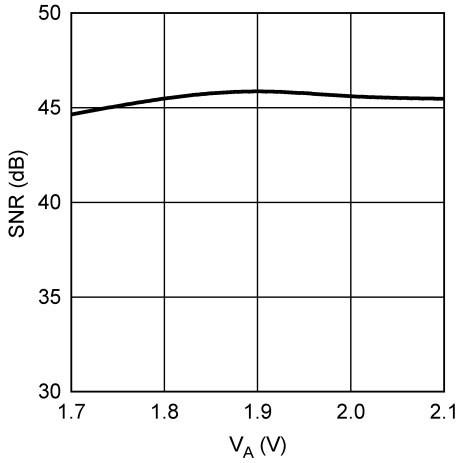


Figure 28.

SNR vs. SAMPLE RATE

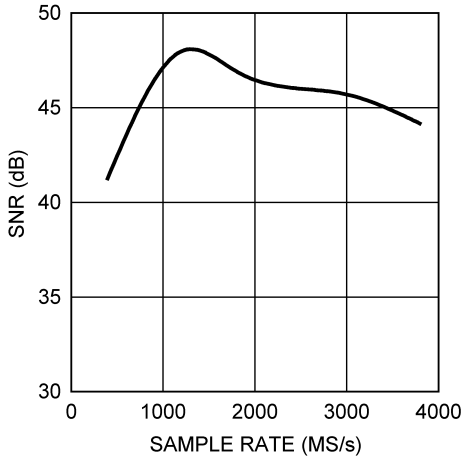


Figure 29.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, f_{CLK}=1500 MHz (i.e., Sample Rate = 3 Gsps), f_{IN}=373 MHz, T_A=25°C unless otherwise stated.

SNR vs. INPUT FREQUENCY

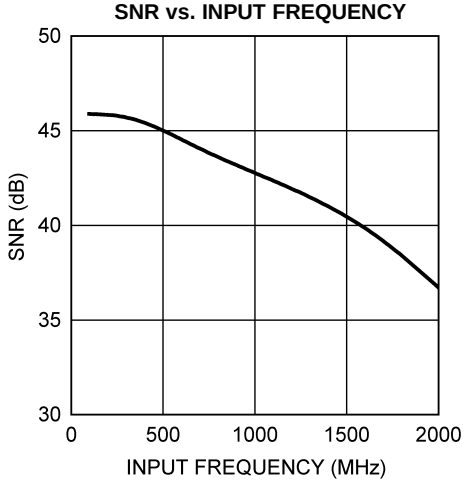


Figure 30.

THD vs. TEMPERATURE

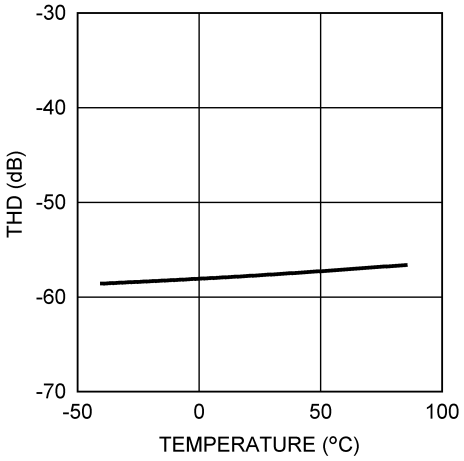


Figure 31.

THD vs. SUPPLY VOLTAGE

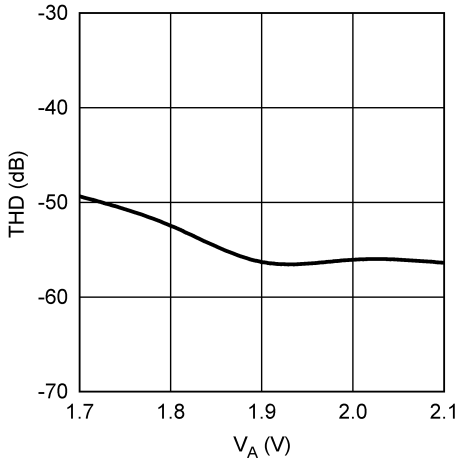


Figure 32.

THD vs. SAMPLE RATE

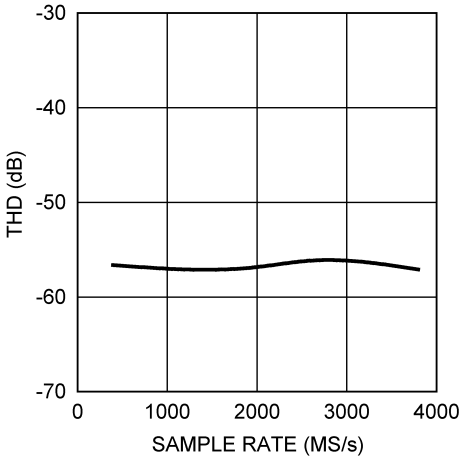


Figure 33.

THD vs. INPUT FREQUENCY

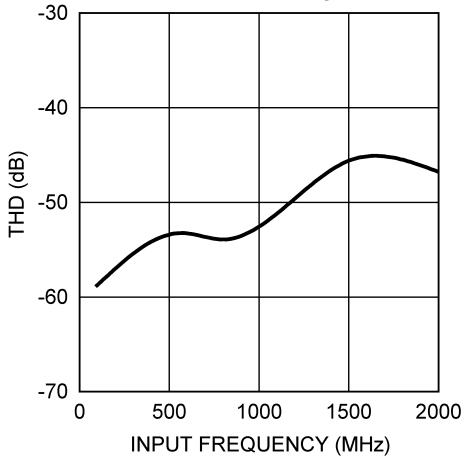


Figure 34.

SFDR vs. TEMPERATURE

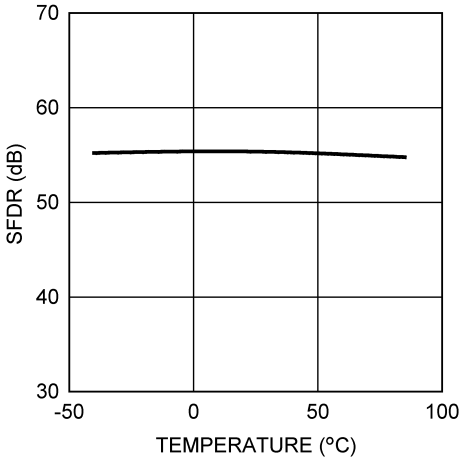


Figure 35.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, f_{CLK}=1500 MHz (i.e., Sample Rate = 3 Gsps), f_{IN}=373 MHz, T_A=25°C unless otherwise stated.

SFDR vs. SUPPLY VOLTAGE

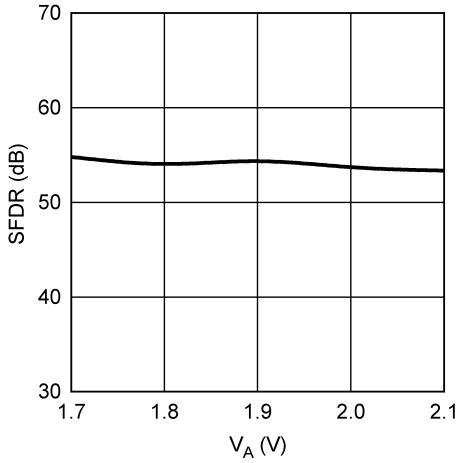


Figure 36.

SFDR vs. SAMPLE RATE

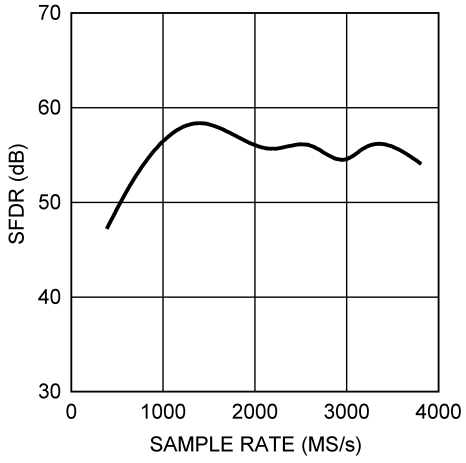


Figure 37.

SFDR vs. INPUT FREQUENCY

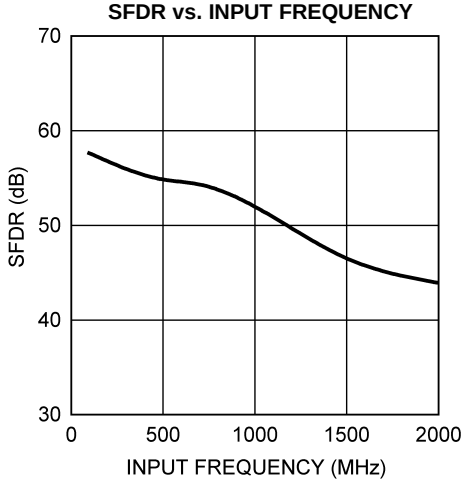


Figure 38.

Spectral Response at FIN = 373 MHz

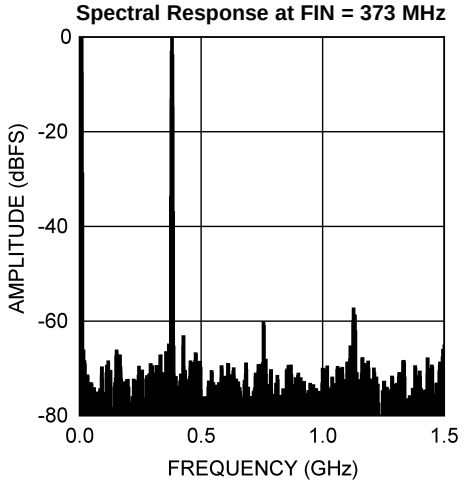


Figure 39.

Spectral Response at FIN = 748 MHz

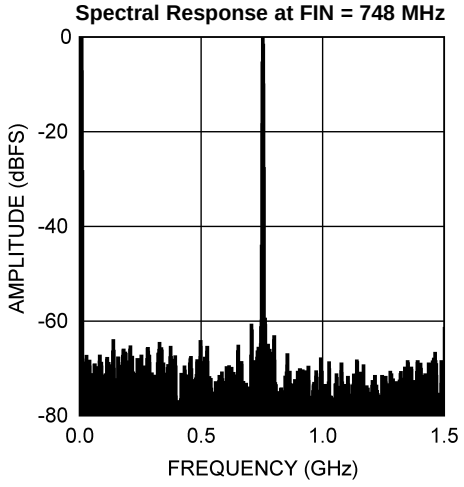


Figure 40.

Spectral Response at FIN = 1497 MHz

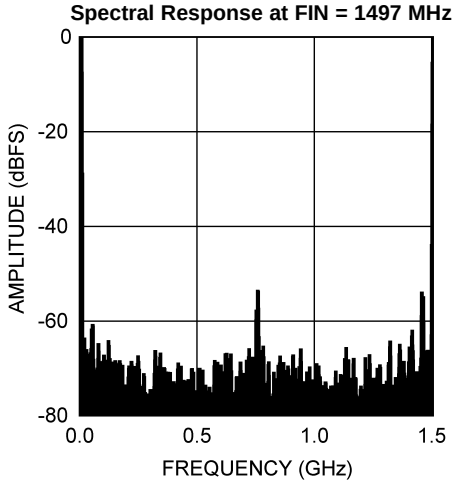


Figure 41.

Typical Performance Characteristics (continued)

V_A=V_{DR}=1.9V, f_{CLK}=1500 MHz (i.e., Sample Rate = 3 Gsps), f_{IN}=373 MHz, T_A=25°C unless otherwise stated.

FULL POWER BANDWIDTH

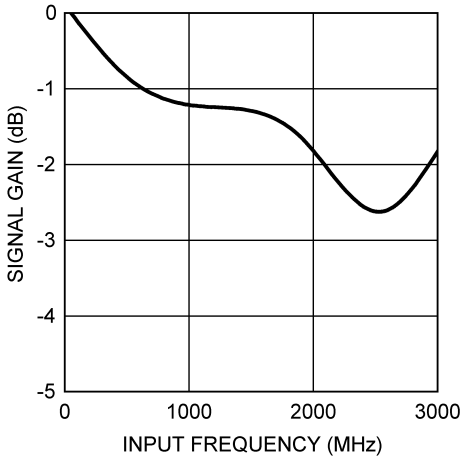


Figure 42.

FUNCTIONAL DESCRIPTION

The ADC08B3000 is a versatile A/D Converter with an innovative architecture permitting very high speed operation. The controls available ease the application of the device to circuit solutions. Optimum performance requires adherence to the provisions discussed here and in Applications Information.

While it is generally poor practice to allow an active pin to float, pins 4 and 14 of the ADC08B3000 are designed to be left floating without jeopardy. In all discussions throughout this data sheet, whenever a function is called by allowing a control pin to float, connecting that pin to a potential of one half the V_A supply voltage will have the same effect as allowing it to float.

OVERVIEW

The ADC08B3000 uses a calibrated folding and interpolating architecture that achieves very high performance. The use of folding amplifiers greatly reduces the number of comparators and power consumption. Interpolation reduces the number of front-end amplifiers required, minimizing the load on the input signal and further reducing power requirements. In addition to other things, on-chip calibration reduces the INL bow often seen with folding architectures. The result is an extremely fast, high performance, low power converter.

The analog input signal that is within the converter's input voltage range is digitized to eight bits at speeds of 1.0 Gsps to 3.4 Gsps, typical. Differential input voltages below negative full-scale will cause the output word to consist of all zeroes. Differential input voltages above positive full-scale will cause the output word to consist of all ones. Either of these conditions at the analog input will cause the OR (Out of Range) output to be activated. This single OR output indicates when the output code from the converter is below negative full scale or above positive full scale.

Calibration

A calibration is performed upon power-up and can also be invoked by the user upon command. Calibration trims the 100Ω analog input differential termination resistor and minimizes full-scale error, offset error, DNL and INL, resulting in maximizing SNR, THD, SINAD (SNDR) and ENOB. Internal bias currents are also set with the calibration process. All of this is true whether the calibration is performed upon power up or is performed upon command. Running the calibration is an important part of this chip's functionality and is required in order to obtain adequate performance. In addition to the requirement to be run at power-up, calibration must be re-run by the user whenever the state of the FSR pin is changed. For best performance, we recommend an on command calibration be run after initial power up and the device has reached a stable temperature. Also, we recommend that an on-command calibration be run 20 seconds or more after application of power and whenever the operating temperature changes significantly relative to the specific system performance requirements. See On-Command Calibration for more information. Calibration can not be initiated or run while the device is in the power-down mode. See Power Down for information on the interaction between Power Down and Calibration.

In normal operation, calibration is performed just after application of power and whenever a valid calibration command is given, which is holding the CAL pin low for at least 80 input clock cycles, then hold it high for at least another 80 input clock cycles. The time taken by the calibration procedure is specified in the AC ELECTRICAL CHARACTERISTICS section of Converter Electrical Characteristics. Holding the CAL pin high during power up will prevent the calibration process from running until the CAL pin experiences the above-mentioned 80 input clock cycles low followed by 80 cycles high.

CalDly (pin 127) is used to select one of two delay times from the application of power before the start of calibration. This calibration delay is 2^{25} input clock cycles (about 22 ms with a 1.5 GHz clock) with CalDly low, or 2^{31} input clock cycles (about 1.4 seconds with a 1.5 GHz clock) with CalDly high. These delay values allow the power supply to come up and stabilize before calibration takes place. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

NOTE: These things should be noted regarding device calibration:

- If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied and PD is already high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.
- During the calibration cycle, the OR output may be active as a result of the calibration algorithm. All data on the output pins and the OR output are invalid during the calibration cycle.
- If a calibration is initiated at any time after clock phase adjustment has been enabled (bit 15 of Coarse Clock Phase Adjust Register, address Eh, set to 1b), the internal clock will stop running at the very beginning of the calibration sequence. It is important to ensure that the clock phase enable bit is off (set to 0b), or that the Resistor Trim Disable bit is on (set to 1b) before running an on-command calibration.
- At least one calibration cycle must be run with the RTD bit in the Configuration Register cleared (at 0b) after power-up to adjust the Analog Input Termination Resistor.
- All input must be within operating norms during the entire calibration process.
- The on-board registers must not be accessed during the calibration process, although the SCLK may be active.
- The CalRun output is high whenever the calibration procedure is running. This is true whether the calibration is done at power-up or on-command.

Acquiring the Input

Data is acquired at both the rising and falling edges of CLK (pin 10). When a Write Enable (WEN) is initiated, the converted data from the ADCs will be loaded into the Capture Buffer. Because of the asynchronous nature of WEN to the sample clock, the Capture Buffer write will occur after the two ADCs have completed a full conversion cycle. This allows the Capture Buffer to store the converted data in a predictable, ordered fashion.

The Capture Buffer will output its digital data at two, 8 bit wide LVCMOS outputs when initiated with the Read Enable (REN) command. For more information on Capture Buffer operation, please refer to CAPTURE BUFFER FUNCTIONAL DESCRIPTION and its subsections. Refer to the timing diagrams related to the Capture Buffer for timing related information.

The ADC08B3000 will convert as long as the sample input clock signal is present. The ADC08B3000 output data signaling is LVCMOS and the output format is offset binary.

Control Modes

Much of the user control can be accomplished with several control pins that are provided. Examples include initiation of the calibration cycle, power down mode and full scale range setting. However, the ADC08B3000 also provides an Extended Control mode whereby a serial interface is used to access register-based control of several advanced features. The Extended Control mode is not intended to be enabled and disabled dynamically. Rather, the user is expected to employ either the normal control mode or the Extended Control mode at all times. When the device is in the Extended Control mode, pin-based control of several features is replaced with register-based control and those pin-based controls are disabled. These pins are OutEdge/DDR (pin 4), FSR (pin 14) and CalDly (pin 127). See THE SERIAL INTERFACE for details on the Extended Control mode.

The Analog Inputs

The ADC08B3000 must be driven with a differential input signal. Operation with a single-ended signal is not recommended as performance will suffer. It is important that the input signals are either a.c. coupled to the inputs with the V_{CMO} pin grounded or d.c. coupled with the V_{CMO} pin left floating or lightly loaded. An input common mode voltage that is equal to and tracks the V_{CMO} output must be provided when d.c. coupling is used.

In the Normal mode, the full-scale range is set to one of two levels, as indicated in Converter Electrical Characteristics, with pin 14 (FSR). In the Extended Control Mode, the full-scale range may be set to one of 512 values, as described in REGISTER DESCRIPTION.

In the Extended Control mode, the full-scale input range can be set to values between 560 mV_{P-P} and 840 mV_{P-P} through a serial interface. See NORMAL/EXTENDED CONTROL, THE SERIAL INTERFACE, and THE ANALOG INPUT.

Clocking

The ADC08B3000 must be driven with an a.c. coupled, differential clock signal. THE SAMPLE CLOCK INPUT describes the use of the clock input pins. This sample clock, CLK, has an optional duty cycle correction feature which is enabled by default and provides improved ADC clocking. This circuitry allows the ADC to be clocked with a signal source having a duty cycle of 20% to 80% (worst case).

To assist the user in reading captured data from the Capture Buffer, the ADC08B3000 has an RCLK input. RCLK is a free-running clock which can be applied asynchronously with respect to the analog input sample clock and can operate up to 200MHz. The data output, DRDY signals and EF flag are asserted synchronous with RCLK. See CAPTURE BUFFER FUNCTIONAL DESCRIPTION and its subsections for information on reading the Capture Buffer.

Dual-Edge Sampling

To achieve 3 Gsps with a 1.5 GHz sample clock, the device uses two ADCs, one sampling the input on the positive edge of the sample clock and the other ADC sampling the same input on the negative edge of the sample clock. The input is thus sampled twice per sample clock cycle, resulting in an overall sample rate of twice the sample clock frequency.

The ADC08B3000 includes an automatic clock phase background adjustment which automatically and continuously adjusts the phase of the rising and falling clock edges relative to each other. This feature removes the need to manually adjust the clock phase and provides optimal ENOB performance.

Double Data Rate

Choice of single data rate (SDR) or double data rate (DDR) output is offered. To select the DDR mode, address 1h, bit 10 of the Configuration Register must be set to 0b. With single data rate the Data Ready (DRDY) frequency is the same as the data rate of the two output buses. With double data rate the DRDY frequency is half the data rate and data is sent to the outputs on both edges of DRDY. DDR clocking is enabled in non-Extended Control mode by allowing pin 4 to float.

OutEdge Setting

To help ease data capture in the SDR mode, the output data may be caused to transition on either the positive or the negative edge of the Data Ready (DRDY) Pins. This is chosen in the Normal mode with the OutEdge input (pin 4). A high on the OutEdge input pin causes the output data to transition on the rising edge of DRDY, while grounding this input causes the output to transition on the falling edge of DRDY. See Output Edge Synchronization. In the Extended Control mode, the OutEdge setting is made with bit 8 of the Configuration Register. See REGISTER DESCRIPTION.

Power Down

The ADC08B3000 is in the active state when the Power Down pin (PD) is low. When the PD pin is high, the device is in the power down mode. In this power down mode the data output pins, DRDY, FF, EF, OR, REN, RCLK and RESET are left active to allow the user to unload the Capture Buffer while the ADC core and the Capture Buffer write circuitry power down to reduce the device power consumption to a minimal level.

See Calibration for information on the interaction of the power down and calibration functions.

NORMAL/EXTENDED CONTROL

The ADC08B3000 may be operated in one of two modes. In the Normal Control Mode, the user accomplishes available configuration and control of the device through several control pins. The "extended control mode" provides additional configuration and control options through the serial interface and a set of 6 internal registers. The control mode is selected with pin 14 (FSR/ECE). The choice of control modes is required to be a fixed selection and is not intended to be switched dynamically while the device is operational.

Table 1 shows how several of the device features are affected by the control mode chosen.0

Table 1. Features and Modes

Feature	Normal Control Mode	Extended Control Mode
SDR or DDR Clocking	Selected with pin 4	Selected with nDE in the Configuration Register (address 1h; bit 10). When the device is in DDR mode, address 1h, bit 8 must be set to 0b.
DDR Clock Phase	Not Selectable (0° Phase Only)	Selected with DCP in the Configuration Register (address 1h; bit 11).
SDR Data transitions with rising or falling DRDY edge	Selected with pin 4	Selected with OE in the Configuration Register (address 1h; bit 8).
Power-On Calibration Delay	Delay Selected with pin 127	Short delay only.
Full-Scale Range	Two ranges selected with pin 14 as described in Converter Electrical Characteristics (1)(2).	512 step adjustments possible over a nominal range of 560 mV to 840 mV by using the Full-Scale Voltage Register (address 3h; bits 7 thru 15).
Input Offset Adjust	Not possible	Up to ±45 mV adjustment in 512 steps in the Offset Adjust Register (address 2h; bits 7 thru 15).
Sample Clock Phase Adjustment	Not possible	The clock phase can be adjusted manually through the Fine & Coarse registers (address Dh and Eh).
Test Pattern Output	Not possible	A test pattern can be made present at the data outputs by selecting TPO in the Test Pattern Register (address Fh; bit 11).

(1) The analog inputs are protected as shown below. Input voltage magnitudes beyond the Absolute Maximum Ratings may damage this device. See Figure 2
(2) To ensure accuracy, it is required that V_A and V_{DR} be well bypassed. Each supply pin must be decoupled with separate bypass capacitors. Additionally, achieving rated performance requires that the backside exposed pad be well grounded.

The default state of the Extended Control Mode is set upon power-on reset (internally performed by the device) and is shown in Table 2.

Table 2. Extended Control Mode Operation (Pin 14 Floating)

Feature	Extended Control Mode Default State
Calibration Delay	Short Delay
Full-Scale Range	700 mV nominal
Input Offset Adjust	0 mV
Clock Phase Adjust - Fine	0 ps Phase Adjust
Clock Phase Adj - Course	0 ps Phase Adjust
Duty Cycle Stabilizer	Enabled
DDR Clock Phase	90° phase aligned
DDR Enable	Single Data Rate, SDR
Capture Buffer Size	4K bytes
Auto-Stop Write	Writes to Capture Buffer will stop automatically
Two Port Enable	Data on data D1 only
Output Edge	Falling edge of DRDY
Test Pattern Output	No test pattern
Differential ADCCLK_RST Enable	Single-ended ADCCLK_RST

THE SERIAL INTERFACE

NOTE

IMPORTANT: During the initial write using the serial interface, all six registers must be written with desired or default values. Subsequent writes to single registers are allowed.

The 3-pin serial interface is enabled only when the device is in the Extended Control mode. The pins of this interface are Serial Clock (SCLK), Serial Data (SDATA) and Serial Interface Chip Select ($\overline{SCS}$). Eight write only registers are accessible through this serial interface. Registers are write only and can not be read back.

$\overline{SCS}$: This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

SCLK: Serial data input is accepted at the rising edge of this signal. There is no minimum frequency requirement of this signal.

SDATA: Each register access requires a specific 32-bit pattern at this input. This pattern consists of a header, register address and register value. The data is shifted in MSB first. Setup and hold times with respect to the SCLK must be observed. See the Timing Diagram of Figure 4.

Each Register access consists of 32 bits, as shown in Figure 4 of the Timing Diagrams. The fixed header pattern is 0000 0000 0001 (eleven zeros followed by a 1). The loading sequence is such that a "0" is loaded first. The next 4 bits are the address of the register that is to be written to and the last 16 bits are the data written to the addressed register. The addresses of the various registers are indicated in Table 3. Refer to REGISTER DESCRIPTION for information on the data to be written to the registers. Subsequent register accesses may be performed immediately, starting with the 33rd SCLK. This means that the $\overline{SCS}$ input does not have to be de-asserted and asserted again between register addresses. It is possible, although not recommended, to keep the $\overline{SCS}$ input permanently enabled (at a logic low) when using extended control.

NOTE

IMPORTANT: The Serial Interface should not be accessed while the ADC is undergoing a calibration cycle. Doing so will impair the performance of the device until it is re-calibrated correctly. Programming the serial registers will also reduce dynamic performance of the ADC for the duration of the register access time.

Table 3. Register Addresses

4-Bit Address					
Loading Sequence: A3 loaded after Fixed Header Pattern, A0 loaded last					
A3	A2	A1	A0	Hex	Register Addressed
0	0	0	0	0h	Reserved
0	0	0	1	1h	Configuration
0	0	1	0	2h	Offset
0	0	1	1	3h	Full-Scale Voltage Adjust
0	1	0	0	4h	Reserved
0	1	0	1	5h	Reserved
0	1	1	0	6h	Reserved
0	1	1	1	7h	Reserved
1	0	0	0	8h	Reserved
1	0	0	1	9h	Reserved
1	0	1	0	Ah	Reserved
1	0	1	1	Bh	Reserved
1	1	0	0	Ch	Reserved
1	1	0	1	Dh	Extended Clock Phase Adjust Fine
1	1	1	0	Eh	Extended Clock Phase Adjust Coarse
1	1	1	1	Fh	Capture Buffer

REGISTER DESCRIPTION

Six write-only registers provide several control and configuration options in the Extended Control Mode. These registers have no effect when the device is in the Normal Control Mode. Each register description below also shows the Power-On Reset (POR) state of each control bit.

The contents of the all registers are retained when the device is in the Power Down mode.

Table 4. Configuration Register

Addr: 1h (0001b)	

D15	D14	D13	D12	D11	D10	D9	D8
1	DRE	RTD	DCS	DCP	nDE	1	OE

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	Must be set to 1b
Bit 14	DRE: Differential Reset Enable. When this bit is set to 0b, it enables the single-ended ADCCLK_RST input. When this bit is set to 1b, it enables the differential ADCCLK_RST input.
	POR State: 0b
Bit 13	RTD: Resistor Trim Disable. The state of this bit determines whether the input signal termination resistor is trimmed or not during the calibration cycle. If the Clock Phase Adjust feature is enabled (ENA bit is set to 1b in register Eh), then this bit must be set to 1b also.
	NOTE: The input termination resistor MUST be trimmed at least once, which will only happen if this bit is 0b. The Power-Up self-calibration cycle will trim the termination resistor as the power-up default value of this bit is 0b.
	POR State: 0b
Bit 12	DCS: Duty Cycle Stabilizer. When this bit is set to 1b, a duty cycle stabilization circuit is applied to the clock input. When this bit is set to 0b the stabilization circuit is disabled.
	POR State: 1b
Bit 11	DCP: DDR Clock Phase. This bit only has an effect in the DDR mode. When this bit is set to 0b, the DRDY edges are time-aligned with the data bus edges (“0° Phase”). When this bit is set to 1b, the DRDY edges are placed in the middle of the data bit cells (“90° Phase”).
	POR State: 1b
Bit 10	nDE: DDR Enable. When this bit is set to 0b, data bus clocking follows the DDR (Dual Data Rate) mode whereby a data word is output with each rising and falling edge of DRDY. When this bit is set to a 1b, data bus clocking follows the SDR (Single Data Rate) mode whereby each data word is output with either the rising or falling edge of DRDY, as determined by the OutEdge bit.
	POR State: 1b
Bit 9	Must be set to 1b
Bit 8	OE: Output Edge. This bit selects the edge of the DRDY pins with which the data words transition in the SDR mode and has the same effect as the OutEdge pin in the normal control mode. When this bit is set to 1b, the data outputs change with the rising edge of the DRDY pins. When this bit is set to 0b, the data outputs change with the falling edge of the DRDY pins.
	POR State: 0b
Bits 7:0	Must be set to 1b.

Table 5. Offset Adjust

Addr: 2h (0010b)	

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Offset Value					(LSB)

D7	D6	D5	D4	D3	D2	D1	D0
Sign	1	1	1	1	1	1	1

Bits 15:8	Offset Value. The input offset of the ADC is adjusted linearly and monotonically by the value in this field. 00h provides a nominal zero offset, while FFh provides a nominal 45 mV of offset. Thus, each code step provides 0.176 mV of offset.
	POR State: 0000 0000 b (no adjustment)
Bit 7	Sign bit. 0b gives positive offset, 1b gives negative offset.
	POR State: 0b
Bit 6:0	Must be set to 1b

Table 6. Full-Scale Voltage Adjust

Addr: 3h (0011b)	

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Adjust Value					

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7	Full Scale Voltage Adjust Value. The input full-scale voltage or gain of the ADC is adjusted linearly and monotonically with a 9 bit data value. The adjustment range is ±20% of the nominal 700 mV_{P-P} differential value.	
	0000 0000 0	560mV_{P-P}
	1000 0000 0 Default Value	700mV_{P-P}
	1111 1111 1	840mV_{P-P}
	For best performance, it is recommended that the value in this field be limited to the range of 0110 0000 0b to 1110 0000 0b. i.e., limit the amount of adjustment to ±15%. The remaining ±5% headroom allows for the ADC's own full scale variation. A gain adjustment does not require ADC re-calibration.	
	POR State: 1000 0000 0b	
Bits 6:0	Must be set to 1b	

Table 7. Sample Clock Phase Adjust Fine

Addr: Dh (1101b)	

D15	D14	D13	D12	D11	D10	D9	D8
(MSB)		Fine Phase Adjust					

D7	D6	D5	D4	D3	D2	D1	D0
(LSB)	1	1	1	1	1	1	1

Bit 15:7	Fine Adjust Magnitude. The phase of the ADC sample clock is adjusted monotonically by the value in this register. A value of 00h provides a nominal zero phase adjustment, while 1FFh provides a nominal 110ps delay.
	POR State: 0000 0000 0b
Bit 6:0	Must be set to 1b

Table 8. Sample Clock Phase Adjust Coarse

Addr: Eh (1110b)	

D15	D14	D13	D12	D11	D10	D9	D8
ENA	CAM				LFS	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	Enable Sample Clock Phase Adjust. Default is 0b. When this feature is enabled, the RTD bit in register 1h **MUST** also be enabled to ensure proper calibration.
Bit 14:11	Coarse Adjust Magnitude. Each LSB results in approximately 70ps of clock adjust.
	POR State: 0000b
Bit 10	Low Frequency Sample clock. When this bit is set 1b, the dynamic performance of the device is improved when the sample clock is less than 900MHz.
	POR State: 0b
Bits 9:0	Must be set to 1b
	NOTE: When this feature is enabled, the RTD bit in register 1h must also be enabled.

Table 9. Capture Buffer Register

Addr: Fh (1111b)	

D15	D14	D13	D12	D11	D10	D9	D8
BSIZE		ASW	TPE	TPO	1	1	1

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	1	1	1

Bit 15	BSIZE<1>: This bit in combination with BSIZE<0> (BIT 14) is used to select the buffer size of the Capture Buffer. The Capture Buffer is size adjustable and it cannot be split between the two LVCMOS data output ports. See CAPTURE BUFFER FUNCTIONAL DESCRIPTION for a table which relates the Capture Buffer size to BSIZE<1:0> programming.
	POR State: 1b
Bit 14	BSIZE<0>: This bit in combination with BSIZE<1> (BIT 15) is used to select the buffer size of the Capture Buffer. The Capture Buffer is size adjustable and it cannot be split between the two LVCMOS data output ports. See CAPTURE BUFFER FUNCTIONAL DESCRIPTION for a table which relates the Capture Buffer size to BSIZE<1:0> programming.
	POR State: 1b
Bit 13	ASW: Auto-Stop Write. When ASW is set to 1b, Capture Buffer writing will stop automatically when the Capture Buffer is full of captured data and the FF flag is asserted. If this bit is set to 0b, the device will continuously write data to the Capture Buffer while overwriting previously captured data.
	POR State: 1b
Bit 12	TPE: Two Port Output Enable. When this bit is set to 1b, data stored in the Capture Buffer will appear on two 8 bit output ports. When this bit is set to 0b, data will only appear on the D1 8 bit output port.
	POR State: 0b
Bit 11	TPO: Test Pattern Output enable. When this bit is set 1b, the ADC is disengaged and a test pattern generator is connected to the outputs including the OR output. This test pattern will work with the device in either the SDR and DDR modes. See ADC TEST PATTERN OUTPUT.
	POR State: 0b
Bits10:0	Must be set to 1b

Clock Phase Adjustment

This is a feature intended to help the system designer remove small imbalances in clock distribution traces at the board level when multiple ADCs are used. Please note, however, that enabling this feature will reduce the dynamic performance (SNR, ENOB, SFDR) some finite amount. The amount of degradation increases with the amount of adjustment applied. The user is strongly advised to use the minimal amount of adjustment and to verify the net benefit of this feature in his system before relying upon it.

Extended Mode Offset Correction

For offset values of +0000 0000 and -0000 0000, the actual offset is not the same. By changing only the sign bit in this case, an offset step in the digital output code of about 1/10th of an LSB is experienced. This is shown more clearly in the Figure 43.

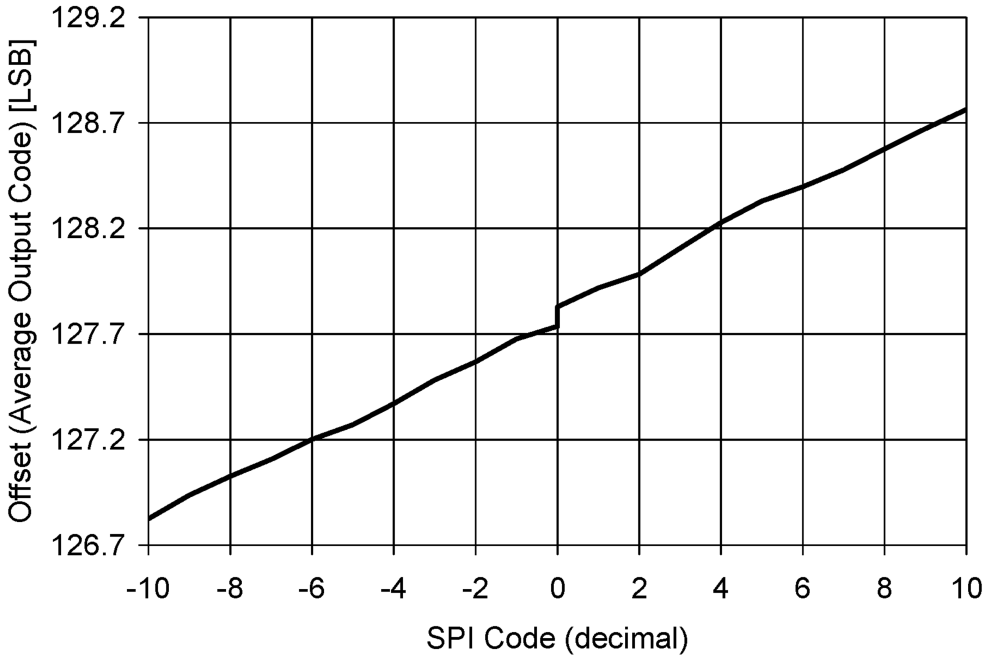


Figure 43. Extended Mode Offset Behavior

MULTIPLE ADC SYNCHRONIZATION

The ADC08B3000 has the capability to precisely reset its sample clock input to support the synchronization of multiple ADCs in a system. The ADCCLK_RST allows multiple ADCs in a system to be synchronized so that there is a known relationship between the sampling times of all ADCs.

The ADC08B3000 has been designed to accommodate systems which require a single-ended (LVCMOS) ADCCLK_RST and those using a differential (LVDS) ADCCLK_RST. In either case, the ADCCLK_RST signal must observe the timing requirements shown in Figure 5 of the Timing Diagrams. The ADCCLK_RST pulse must be of a minimum width and its deassertion edge must observe setup and hold times with respect to the CLK input rising edge. These timing specifications are listed as t_{HR}, t_{SR}, and t_{PWR}. The duration of the ADCCLK_RST pulse affects the length of time before valid data can be captured, so minimizing this pulse width is recommended.

Single-Ended (LVCMOS) ADCCLK_RST: The Power on Reset state of ADCCLK_RST is to have single-ended ADCCLK_RST activated. That is, bit 14, (DRE) in the Configuration Register is low, 0b. When not using singled-ended ADCCLK_RST, this input pin should be grounded. When using the single-ended ADCCLK_RST, consider the ADCCLK_RST+ signal of Figure 5 and ignore ADCCLK_RST-.

Differential (LVDS) ADCCLK_RST: Activated by setting bit 14 (DRE) of the configuration register high, 1b. When the differential ADCCLK_RST is not activated (that is, when bit 14 of the Configuration Register is 0b), these inputs should be grounded. Differential ADCCLK_RST has an internal 100 ohm termination resistor and should be DC coupled, not be AC coupled.

The ADCCLK_RST signal can be asserted asynchronous to the input clock. When the ADCCLK_RST signal is de-asserted in synchronization with the CLK rising edge, the next CLK falling edge synchronizes the ADC08B3000 with the other ADC08B3000s in the system. The user has the option of using a single-ended ADCCLK_RST signal, but a differential ADCCLK_RST is strongly recommended due to its superior timing performance.

ADC TEST PATTERN OUTPUT

To aid in system debug, the ADC08B3000 has the capability of providing a test pattern at the 2 outputs completely independent of the input signal. By default, the test pattern will only appear at the D1 port. To have the test pattern appear at both D1 and D2 ports, bit 12 (TPE) must be programmed to 1b in the Capture Buffer Register (address Fh). Refer to REGISTER DESCRIPTION. To engage the test pattern, bit 11 (TPO) must be programmed to 1b in the Capture Buffer Register (address Fh). When the test pattern is enabled, the ADC is disengaged and a test pattern generator is connected to the output ports, including OR. The OR output is asserted high at the start of the test pattern output and will remain high until the data is read out of the Capture Buffer and the Empty Flag (EF) is asserted high. Each port can output a unique pattern sequence as described in Table 10 and Table 11. The test pattern appears on the output port with the transition of DRDY.

Table 10. Test Pattern Output By Port in One Port Output SDR Mode

Time	Port D1	Port D2	OR	Comments
T0	01h	Hi-Z	1	Pattern Sequence n
T1	02h		1	
T2	03h		1	
T3	04h		1	
T4	FEh		1	
T5	FDh		1	
T6	FCh		1	
T7	FBh		1	
T8	01h		1	
T9	02h		1	
T10	03h		1	
T11	04h		1	
T12	FEh		1	
T13	FDh		1	
T14	FCh		1	
T15	FBh		1	
T16	01h		1	
T17	02h		1	
T18	03h		1	
T19	04h		1	

Table 10. Test Pattern Output By Port in One Port Output SDR Mode (continued)

Time	Port D1	Port D2	OR	Comments
T20	01h	Hi-Z	1	Pattern Sequence n+1
T21	02h		1	
T22	03h		1	
T23	04h		1	
T24	FEh		1	
T25	FDh		1	
T26	FCh		1	
T27	FBh		1	
T28	01h		1	
T29	02h		1	
T30	...		...	

Table 11. Test Pattern Output By Port in Two Port Output SDR Mode

Time	Port D1	Port D2	OR	Comments
T0	02h	01h	1	Pattern Sequence n
T1	04h	03h	1	
T2	FDh	FEh	1	
T3	FBh	FCh	1	
T4	02h	01h	1	
T5	04h	03h	1	
T6	FDh	FEh	1	
T7	FBh	FCh	1	
T8	02h	01h	1	
T9	04h	03h	1	
T10	02h	01h	1	Pattern Sequence n+1
T11	04h	03h	1	
T12	FDh	FEh	1	
T13	FBh	FCh	1	
T14	02h	01h	1	
T15	...	...	...	

CAPTURE BUFFER FUNCTIONAL DESCRIPTION

With the integration of the Capture Buffer, the ADC08B3000 allows sampling and processing tasks to be separated. The intent is that the input signal can be sampled at a high rate and collected samples can be off-loaded for digital processing at a slower rate. There are 5 main signals which are used to coordinate the handshaking between the Capture Buffer data capture operation and the Capture Buffer read operation. These five signals are Write Enable (WEN), Read Enable (REN), Empty Flag (EF), Full Flag (FF) and RESET.

It is important to note that the Capture Buffer implemented in this product is not a general purpose FIFO. The Capture Buffer size is programmable in the Extended Control Mode using bit 15 (BSIZE<1>) and bit 14 (BSIZE<0>) in the Capture Buffer Register. See Table 12. In order for a Capture Buffer read to commence, the entire buffer has to be filled. It is not possible to write to and read from the Capture Buffer simultaneously.

Table 12. Programmable Capture Buffer Size

BSIZE<1>	BSIZE<0>	Buffer Size (Bytes)
0	0	512
0	1	1024
1	0	2048
1	1	4096

Error Flags

The ADC08B3000 provides two output control signals, the Full Flag (FF) and the Empty Flag (EF), to monitor the status of the Capture Buffer. Following the assertion of REN and the subsequent reading of the Capture Buffer, the Empty Flag (EF) will be asserted by the device to indicate that the last data was read and the Capture Buffer is now empty. Once the (EF) Empty Flag is asserted by the device, the user cannot re-read the Capture Buffer. Only when Empty Flag (EF) is asserted high can a Capture Buffer data capture or WEN operation begin. The assertion of WEN clears the Empty Flag (EF).

The data can only be read from the Capture Buffer when the buffer is full. That is, when FF (Full Flag) is high. Once the FF is high, the data is ready to be read from the Capture Buffer on the rising edges of RCLK. The assertion of REN clears the Full Flag (FF).

The assertion of a RESET signal clears the Full Flag (FF), sets the Empty Flag (EF) and clears both the data capture to buffer and the buffer read operations.

Writing to the Capture Buffer

An internally generated write clock is used to write the converted data into the Capture Buffer. The write clock is the same speed as the ADC Sample Clock. Unless the chip is in a power-down state, the ADC is always converting the input signal. The data is stored in the Capture Buffer only when the Write Enable (WEN) signal is asserted.

After the Capture Buffer is full and the Full Flag (FF) is asserted, new data will start writing over the oldest data because the Write Pointer will wrap-around. The user has the option to stop the writing of the Capture Buffer automatically upon a full condition with the use of the ASW (Auto-Stop Write) input. This is done in the Extended Control Mode by setting bit 13 in the Capture Buffer register to 1b. Refer to REGISTER DESCRIPTION.

When the data is completely read from the Capture Buffer, the Empty Flag (EF) will be asserted by the device. Only at this point can another data capture sequence begin (by the assertion of WEN). The assertion and internal synchronization of WEN clears the Empty Flag (EF).

Reading from the Capture Buffer

Once the Full Flag (FF) is asserted high, the data is ready to be read from the Capture Buffer on the rising edges of RCLK, which is an externally applied free-running clock that can be asynchronous with respect to the ADC sample clock. To read the data out of the Capture Buffer, the Read Enable (REN) signal must be asserted. The Full Flag (FF) is cleared with the assertion and internal synchronizing of REN. An Empty Flag (EF) will be asserted by the device to indicate that the last data was read and the Capture Buffer is now empty.

When the Two Port Output Enable is set to 0b in the Capture Buffer Register (addr: Fh, bit: 12 (TPE)), only port D1 will be enabled for data extraction from the Capture Buffer. When the Two Port Output Enable is set to 1b in the Capture Buffer Register, ports D1 and D2 will be enabled for data extraction. For interleaving purposes, the format of data is in 8-bit words with D2 outputting the first 8-bits from the Capture Buffer followed by D1 and back to D2. Data output order is the same as the Test Pattern Output mode data output order. See Table 11 for data order in Test Pattern Output mode.

Coordinating Read Enable (REN) and Write Enable (WEN)

It is not possible to write to and read from the Capture Buffer simultaneously. This means that the Write Enable (WEN) and the Read Enable (REN) signals should not be asserted simultaneously. If the Read Enable (REN) and Write Enable (WEN) signals are asserted at the same time, the Write Enable (WEN) signal supersedes and the Read Enable (REN) signal is ignored. This is true even if the Read Enable (REN) signal is asserted first and the buffer read operation is progressing normally. If the Write Enable (WEN) signal is asserted while Read Enable (REN) is asserted, the Capture Buffer will freeze its operation until a RESET is applied. Recall that RESET allows the Capture Buffer pointers to be reset so a new data capture operation can begin.

Capture Buffer Reset

The RESET signal clears FF and sets EF and halts both the data capture and data read operations. The RESET signal can be useful during a partial read scenario where the data read operation stops early and the EF is not asserted by the device. In this case the RESET signal allows the Capture Buffer pointers to be reset so a new data capture operation can begin. The RESET signal has no effect upon the operation of the ADC, which has its own internal Power-On Reset circuit.

Data Ready and Write Enable Sync

The ADC08B3000 has three other signals available to coordinate the Capture Buffer data capture and Capture Buffer read operations. These signals are Data Ready Port 1 (DRDY1), Date Ready Port 2 (DRDY2), and Write Enable Sync (WENSYNC). Data Ready Port 1 (DRDY1) and Data Ready Port 2 (DRDY2) can be used as latch clocks for external systems as there are applications where using RCLK alone to capture the data on the data output ports D1 and D2 is not practical. The Data Ready (DRDY) pins offer improved data capture capability by eliminating the impact of the RCLK path delay and the internal RCLK-to-DataOut delay. Data Ready (DRDY) is presented on the output ports at the same time as the data output. RCLK is used by the device to clock the data out of the Capture Buffer and the DRDY signals are used to clock that data into the receiving circuit. The output data and DRDY signals appear at the output ports three rising edges of RCLK after the assertion of REN.

Write Enable Sync (WENSYNC) is a synchronized version of Write Enable (WEN) and is synchronized with the ADC sample clock. Write Enable Sync (WENSYNC) is provided as an output because Write Enable (WEN) can be asserted completely asynchronous with the ADC sample clock, therefore it would be difficult for the user to know exactly when the data capture operation actually began. Write Enable Sync (WENSYNC) allows the user to determine this.

Out of Range

Out of Range (OR) is a signal used to determine if the input signal has over gone out of range at any time during a data capture operation. It is asserted if an Out of Range condition occurred during the data capture operation and is cleared only after the Capture Buffer read operation is complete and the Empty Flag (EF) is asserted. The OR output is invalid during a calibration cycle.

Applications Information

THE REFERENCE VOLTAGE

The voltage reference for the ADC08B3000 is derived from a 1.254V bandgap reference, a buffered version of which is made available at pin 31, V_{BG}, for user convenience. This output has an output current capability of ±100 µA. This reference voltage should be buffered if more current is required.

The internal bandgap-derived reference voltage has a choice of two nominal values in the Normal mode as determined by the FSR pin and described in The Analog Inputs.

There is no provision for the use of an external reference voltage, but the full-scale input voltage can be set to one of two values in the Normal mode, as shown in the Electrical Tables, or it can be set through the Full-Scale Voltage Adjust Register in the Extended Control mode to one of 512 values, as explained in NORMAL/EXTENDED CONTROL. Never drive this pin.

Differential input signals up to the chosen full-scale level will be digitized to 8 bits. Signal excursions beyond the full-scale range will be clipped at the output.

THE ANALOG INPUT

The analog input is a differential one to which the signal source may be a.c. coupled or d.c. coupled. The full-scale input range is selected with the FSR pin, or can be adjusted to one of 512 values in the Extended Control mode through the Serial Interface. For best performance it is recommended that the full-scale range be kept between 595 mV_{P-P} and 805 mV_{P-P} in the Extended Control mode because the internal DAC which sets the full-scale range is not as linear at the ends of its range.

Table 13 gives the input to output relationship with the FSR pin high when the Normal (non-extended) mode is used. With the FSR pin grounded, the millivolt values in Table 13 are reduced to about 75% (600/810) of the values indicated. In the Enhanced Control Mode, these values will be determined by the full scale range and offset settings in the Control Registers.

Table 13. DIFFERENTIAL INPUT TO OUTPUT RELATIONSHIP (Non-Extended Control Mode, FSR High)

V_{IN}+	V_{IN}−	Output Code
V_{CM} − 405 mV	V_{CM} + 405 mV	0000 0000
V_{CM} − 202.5 mV	V_{CM} + 202.5 mV	0100 0000
V_{CM}	V_{CM}	0111 1111 / 1000 0000
V_{CM} + 202.5 mV	V_{CM} − 202.5 mV	1100 0000
V_{CM} + 405 mV	V_{CM} − 405 mV	1111 1111

The internally buffered analog inputs simplify the task of driving these inputs and the RC pole that is generally used at sampling ADC inputs is not required. If it is desired to use an amplifier circuit before the ADC, use care in choosing an amplifier with adequate noise and distortion performance and adequate gain at the frequencies used for the application.

The Input impedance of the analog input in the d.c. coupled mode (V_{CMO} pin not grounded) consists of a precision 100Ω resistor across the inputs and a capacitance from each of these inputs to ground. In the a.c. coupled mode, the input appears the same except there is also a resistor of 50KΩ between each analog input pin and the on-chip V_{CMO} potential.

When the inputs are a.c. coupled, the V_{CMO} output *must* be grounded, as shown in Figure 44. This causes the on-chip V_{CMO} voltage to be connected to the inputs through on-chip 50KΩ resistors.

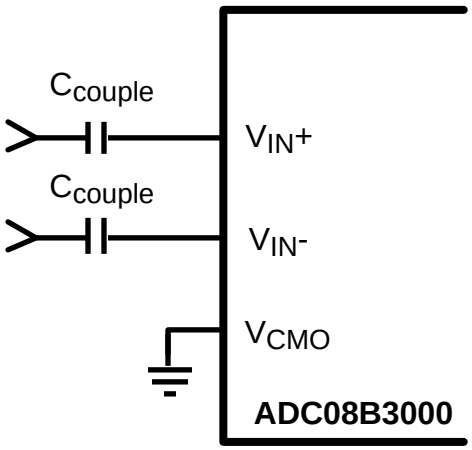


Figure 44. Differential Data Input Connection

When the d.c. coupled mode is used, a precise common mode voltage must be provided at the differential inputs. This common mode voltage should track the V_{CMO} output pin. Note that the V_{CMO} output potential will change with temperature. The common mode output of the driving device should track this change.

Full-scale distortion performance falls off rapidly as the input common mode voltage deviates from V_{CMO}. This is a direct result of using a very low supply voltage to minimize power. Keep the input common voltage within 50 mV of V_{CMO}.

Performance is as good in the d.c. coupled mode as it is in the a.c. coupled mode, provided the input common mode voltage at both analog inputs remain within 50 mV of V_{CMO}.

Handling Single-Ended Input Signals

There is no provision for the ADC08B3000 to adequately process single-ended input signals. The best way to handle single-ended signals is to convert them to differential signals before presenting them to the ADC.

A.C. Coupled Input

The easiest way to accomplish single-ended to differential conversion for a.c. signals is with an appropriate balun, as shown in Figure 45. This figure is a generic depiction of a single-ended to differential signal conversion using a balun. The balun-specific circuitry will depend upon the type of balun selected and the overall board layout. It is recommended that the manufacturer of the selected balun be contacted for aid in designing the best performing single-ended to differential conversion circuit using that particular balun.

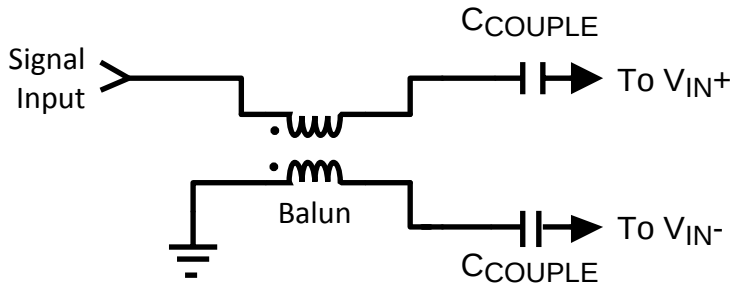


Figure 45. Single-Ended to Differential Signal Conversion with a Balun

When selecting a balun, it is important to understand the input architecture of the ADC. There are specific balun parameters about which the system designer should be mindful. Match the impedance of the analog source to transmission path and that path to the ADC08B3000's on-chip 100Ω differential input termination resistor. The range of this input termination resistor is described in Converter Electrical Characteristics as the specification R_{IN}.

The phase and amplitude balance are important. The lowest possible phase and amplitude imbalance is desired when selecting a balun. The phase imbalance should be no more than ±2.5° and the amplitude imbalance should be limited to less than 1dB at the desired input frequency range.

Finally, when selecting a balun, the VSWR (Voltage Standing Wave Ratio), bandwidth and insertion loss of the balun should also be considered. The VSWR aids in determining the overall transmission line termination capability of the balun when interfacing to the ADC input. The insertion loss should be considered so that the signal at the balun output is within the desired input range at the ADC input.

D.C. Coupled Input

When d.c. coupling to the ADC08B3000 analog input is required, single-ended to differential conversion may be easily accomplished with the LMH6555 fully differential amplifier. An example of this type of circuit is shown in Figure 46. In such applications, the LMH6555 performs the task of single-ended to differential conversion while delivering low distortion and noise, as well as output balance, that supports the operation of the ADC08B3000. Connecting the ADC08B3000 V_{CMO} pin to the V_{CM_REF} pin of the LMH6555 will ensure that the common mode input voltage is as needed for optimum performance of the ADC08B3000. The LMV321 was chosen to buffer V_{CMO} for its low voltage operation and reasonable offset voltage.

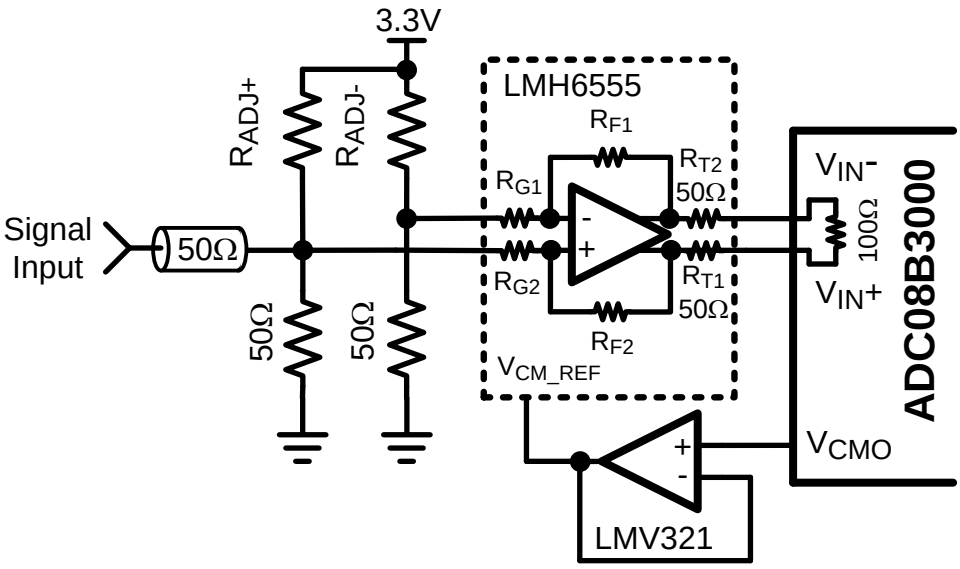


Figure 46. Example of Servoing the Analog Input with V_{CMO}

Be sure that the current drawn from the V_{CMO} output does not exceed 100 µA.

In Figure 46, R_{ADJ-} and R_{ADJ+} are used to adjust the differential offset that can be measured between the ADC inputs V_{IN+} and V_{IN-}. An unadjusted positive offset greater than 15mV should be reduced with a resistor in the R_{ADJ-} position. Likewise, an unadjusted negative offset more negative than −15mV should be reduced with a resistor in the R_{ADJ+} position. Table 14 gives suggested R_{ADJ-} and R_{ADJ+} values for various unadjusted differential offsets to bring the offset between V_{IN+} and V_{IN-} back to within |15mV|. The circuit of Figure 46 assumes a 50Ω d.c. coupled driving source.

Table 14. D.C. Coupled Offset Adjustment

Unadjusted Offset Reading	Resistor Value
0mV to 10mV	no resistor needed
11mV to 30mV	20.0kΩ
31mV to 50mV	10.0kΩ
51mV to 70mV	6.81kΩ
71mV to 90mV	4.75kΩ
91mV to 110mV	3.92kΩ

Out Of Range (OR) Indication

When the conversion result is clipped the Out of Range output is activated such that OR+ goes high and OR- goes low. This output is active as long as accurate data on either or both of the buses would be outside the range of 00h to FFh. The OR output is invalid During a calibration cycle.

Full-Scale Input Range

As with all A/D Converters, the input range is determined by the value of the ADC's reference voltage. The reference voltage of the ADC08B3000 is derived from an internal band-gap reference. In the Normal Mode, the FSR pin controls the effective reference voltage of the ADC08B3000 such that the differential full-scale input range at the analog inputs is one value with the FSR pin high and another value with the FSR pin low. These full scale values are in Converter Electrical Characteristics. In the Extended Control Mode, the Full Scale Range can be set to any of 512 values, as indicated in the Full-Scale Adjust Register description of REGISTER DESCRIPTION. Best SNR is obtained with higher Full Scale Ranges, but better distortion and SFDR are obtained with lower Full Scale Ranges. The LMH6555 of Figure 46 is suitable for any Full Scale Range capability of the ADC08B3000.

THE SAMPLE CLOCK INPUT

The ADC08B3000 has a differential LVDS clock input which must be driven with an a.c. coupled, differential clock signal. Although the ADC08B3000 is tested and its performance is ensured with a differential 1.5 GHz clock, it typically will function well with input clock frequencies indicated in Converter Electrical Characteristics. The clock inputs are internally terminated and biased. The input clock signal must be capacitively coupled to the clock pins as indicated in Figure 47.

Operation up to the sample rates indicated in Converter Electrical Characteristics is typically possible if the maximum ambient temperatures indicated are not exceeded. Operating at higher sample rates than indicated for the given ambient temperature may result in reduced device reliability and product lifetime. This is because of the higher power consumption and die temperatures at high sample rates. Also important for reliability is proper thermal management, as discussed in Thermal Management.

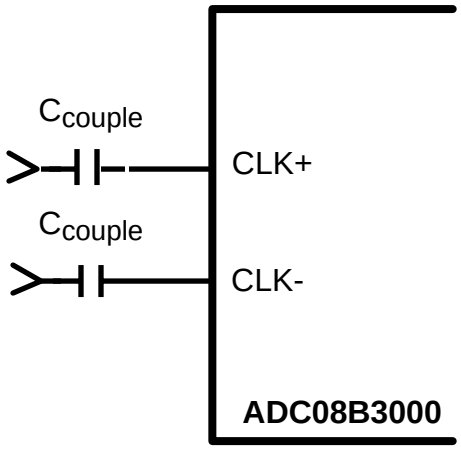


Figure 47. Differential Sample Clock Connection

The differential sample clock line should have a differential characteristic impedance of 100Ω and be terminated at the clock source in that (100Ω) characteristic impedance. The input clock line should be as short and as direct as possible. The ADC08B3000 clock input is internally terminated with an untrimmed 100Ω resistance.

The clock level is important if the specified dynamic performance is to be met. Insufficient input clock levels will result in poor noise performance. Excessively high input clock levels could result in poor SFDR performance our cause a change in the analog input offset voltage. To avoid these problems, keep the input clock level within the range specified in Converter Electrical Characteristics.

The low and high times of the input clock signal can affect the performance of any A/D Converter. The ADC08B3000 features a clock duty cycle correction circuit which can maintain performance over a wide range of input clock duty cycles and over temperature. The ADC will meet its performance specification if the input clock high and low times are maintained as specified in Converter Electrical Characteristics.

High speed, high performance ADCs such as the ADC08B3000 require a very stable input clock signal with minimum phase noise or jitter. ADC jitter requirements are defined by the ADC resolution (number of bits), maximum ADC input frequency and the input signal amplitude relative to the ADC input full scale range. The maximum jitter (the sum of the jitter from all sources) allowed to prevent a jitter-induced reduction in SNR is found to be

$$t_{J(MAX)} = (V_{INFSR}/V_{IN(P-P)}) \times (1/(2^{(N+1)} \times \pi \times f_{IN})) \quad (6)$$

where $t_{J(MAX)}$ is the rms total of all jitter sources in seconds, $V_{IN(P-P)}$ is the peak-to-peak analog input signal, V_{INFSR} is the full-scale range of the ADC, "N" is the ADC resolution in bits and f_{IN} is the maximum input frequency, in Hertz, at the ADC analog input.

Note that the maximum jitter described above is the Root Sum Square, (RSS), of the jitter from all sources, including the internal ADC clock jitter, that added by the system to the ADC input clock and input signals and that added by the ADC itself. Since the effective jitter added by the ADC is beyond user control, the best the user can do is to keep the sum of the externally added input clock jitter and the jitter added by the analog circuitry to the analog signal to a minimum.

Synchronizing Multiple ADCs (Manual Sample Clock Phase Adjust)

To facilitate the synchronization of multiple ADC08B3000 chips to achieve net sample rates higher than that possible with a single device, the ADC08B3000 has a manual clock phase capability. This adjustment is only possible in the Extended Control Mode and is intended to allow the user to accommodate subtle layout differences when between multiple ADCs. Register addresses Dh and Eh provide extended mode access to fine and coarse adjustments. Use of Low Frequency Sample Clock control, (register Eh; bit 10) is not supported while using manual sample clock phase adjustments.

It should be noted that by just enabling the phase adjust capability (register Eh; bit 15), degradation of dynamic performance is expected, specifically SFDR. It is intended that very small adjustments are used. That is just a few counts of the fine adjustment and no adjustment of the coarse adjustment. Larger increases in phase adjustments will begin to affect SNR and ultimately ENOB. Therefore, the use of coarse phase adjustment should be minimized in favor of better system design.

It is best, then, to ensure that the proper phase relationships exist between the analog input and clock signals presented to each of the ADC08B3000s that are synchronized. That is, use as much care in PCB design and layout that would be used if there were no clock phase adjustment circuitry.

Figure 48 and Figure 49 indicate the typical phase adjustment for the fine and coarse phase adjustments, respectively.

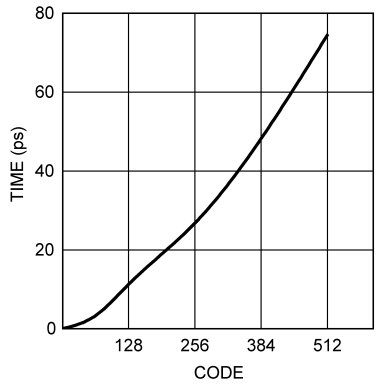


Figure 48. Typical Fine Clock Phase Adjust Range

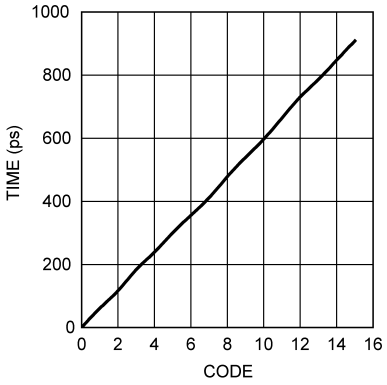


Figure 49. Typical Coarse Clock Phase Adjust Range

CONTROL PINS

Without the use of the serial interface, six control pins provide a range of possibilities in the operation of the ADC08B3000 to facilitate its use. These control pins provide Full-Scale Input Range setting, Self Calibration, Calibration Delay, Output Edge Synchronization choice, and Power Down.

Full-Scale Input Range Setting

The input full-scale range can be selected to be either of two settings with the FSR control input (pin 14) in the Normal Mode of operation. In the Extended Control Mode, the input full-scale range may be set to any of 512 settings. See REGISTER DESCRIPTION for more information.

Calibration

The ADC08B3000 calibration must be run to achieve specified performance. The calibration procedure is run upon power-up and can be run any time on command. The calibration procedure is exactly the same whether there is an input clock present upon power up or if the clock begins some time after application of power. The calibration procedure is also exactly the same whether it is a power-on calibration or an on-command calibration. The CalRun output is high while a calibration is in progress.

Power-On Calibration

Power-on calibration begins after a time delay following the application of power. This time delay is determined by the setting of CalDly. See Calibration Delay.

The calibration process will be not be performed if the CAL pin is high at power up. In this case, the calibration cycle will not begin until the on-command calibration conditions are met. The ADC08B3000 will function with the CAL pin held high at power up, but no calibration will be done and performance will be impaired. A manual calibration, however, may be performed after powering up with the CAL pin high. See On-Command Calibration.

The internal power-on calibration circuitry comes up in an unknown logic state. If the input clock is not running at power up and the power on calibration circuitry is active, it will hold the analog circuitry in power down and the power consumption will typically be less than 25 mW. The power consumption will be normal after the clock starts.

On-Command Calibration

To initiate an on-command calibration, bring the CAL pin high for a minimum of 80 input clock cycles after it has been low for a minimum of 80 input clock cycles. Holding the CAL pin high upon power up will prevent execution of power-on calibration until the CAL pin is low for a minimum of 80 input clock cycles, then brought high for a minimum of another 80 input clock cycles. The calibration cycle will begin 80 input clock cycles after the CAL pin is thus brought high. The CalRun signal should be monitored to determine when the calibration cycle has completed.

The minimum t_{CAL_L} and t_{CAL_H} input clock cycle sequence is required to ensure that random noise does not cause a calibration to begin when it is not desired. As mentioned in Calibration, for best performance a calibration should be performed 20 seconds or more after power up because and repeated when the operating temperature changes significantly relative to the specific system design performance requirements. The suggestion for performing an on-command calibration 20 seconds or more after application of power is because dynamic performance changes with a large change in die temperature and that temperature is nearly stable about 20 seconds after application of power. Dynamic performance changes slightly with increasing junction temperature and can be easily corrected by performing an on-command calibration.

Both the ADC and the input termination resistor are calibrated during a power-on calibration cycle. By default, on-command calibration includes calibration of the input termination resistor and the ADC. However, since the input termination resistor changes only slightly with temperature, the user has the option to disable the input termination resistor trim, once trimmed at power up. The Resistor Trim Disable can be programmed in the Configuration Register when in the Extended Control mode.

Calibration Delay

The CalDly input (pin 127) is used to select one of two delay times after the application of power to the start of calibration, as described in Calibration. The calibration delay values allow the power supply to come up and stabilize before calibration takes place. With no delay or insufficient delay, calibration might begin before the power supply is stabilized at its operating value and result in non-optimal calibration coefficients. If the PD pin is high upon power-up, the calibration delay counter will be disabled until the PD pin is brought low. Therefore, holding the PD pin high during power up will further delay the start of the power-up calibration cycle. The best setting of the CalDly pin depends upon the power-on settling time of the power supply.

Note that the calibration delay selection is not possible in the Extended Control mode and the short delay time is used.

Input Termination Resistor Trim

The calibration algorithm also trims the input signal termination resistor. This is essential for proper operation of the device. Once trimmed upon power-up, however, it is not essential for proper operation of the device. Once trimmed, however, it is not necessary to trim the resistor at each subsequent calibration. The RTD bit in the Configuration Register allows the user to disable input resistor trim. It is required that this RTD bit be set to 1b if the Clock Phase Adjust feature is used.

Output Edge Synchronization

OutEdge is an input available to help latch the converter output data into external circuitry. This pin may make data capture easier, especially when output clock and data trace lengths are not matched. This pin allows the user to shift the phase of the Data Ready pins (DRDY1 and DRDY2) with respect to the data outputs. See Double Data Rate.

Power Down Feature

The Power Down pin (PD) allows the ADC08B3000 to be powered down while the capture buffer is still active so that it may be read. See Power Down for details on the power down feature.

The Capture Buffer, its control pins and digital data outputs remain active in the power down mode, allowing the user to read the Capture Buffer when the PD is high. Upon return to normal operation, the pipeline will contain meaningless information and must be flushed.

If the PD input is brought high while a calibration is running, the device will not go into power down until the calibration sequence is complete. However, if power is applied when the PD input is high, the device will not begin the calibration sequence until the PD input goes low. If a manual calibration is requested while the device is powered down, the calibration will not begin at all. That is, the manual calibration input is completely ignored in the power down state.

THE DIGITAL OUTPUTS

The output format is Offset Binary and the logic is LVCMOS. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}− will produce an output code of all ones, a full-scale input level with V_{IN}− positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}− are equal, the output code will be 127 or 128.

Since the minimum recommended input clock rate for this ADC is 500 MHz and the ADC08B3000 sample rate is twice the clock rate, the minimum sample rate is generally 1 Gsps. However, the output can easily be decimated by two, which effectively reduces the minimum effective sample rate to 500 Msps. This is done by setting the TPE bit in the Capture Buffer register (address Fh, bit D12) to 1b, setting the clock rate to 500 MHz and using the output data from only one of the two ports.

The output format is Offset Binary. Accordingly, a full-scale input level with V_{IN}+ positive with respect to V_{IN}- will produce an output code of all ones, a full-scale input level with V_{IN}- positive with respect to V_{IN}+ will produce an output code of all zeros and when V_{IN}+ and V_{IN}- are equal, the output code will vary between code 127 and 128.

POWER CONSIDERATIONS

A/D converters draw sufficient transient current to corrupt their own power supplies if not adequately bypassed. A 33 µF capacitor should be placed within an inch (2.5 cm) of the A/D converter power pins and a 0.1 µF capacitor should be placed as close as possible to each V_A pin, preferably within one-half centimeter. Leadless chip capacitors are preferred because they have low lead inductance.

The V_A and V_{DR} supply pins should be isolated from each other to prevent any digital noise from being coupled into the analog portions of the ADC. A ferrite choke, such as the Bourns FB20009-3B, is recommended between these supply lines when a common source is used for them.

As is the case with all high speed converters, the ADC08B3000 should be assumed to have little power supply noise rejection. Any power supply used for digital circuitry in a system where a lot of digital power is being consumed should not be used to supply power to the ADC08B3000. The ADC supplies should be the same supply used for other analog circuitry, if not a dedicated supply.

Supply Voltage

The ADC08B3000 is specified to operate with a supply voltage of 1.9V ±0.1V. It is very important to note that, while this device will function with slightly higher supply voltages, these higher supply voltages may reduce product lifetime.

No pin should ever have a voltage on it that is in excess of the supply voltage or below ground by more than 150 mV, not even on a transient basis. This can be a problem upon application of power and power shut-down. Be sure that the supplies to circuits driving any of the input pins, analog or digital, do not come up any faster than does the voltage at the ADC08B3000 power pins.

The Absolute Maximum Ratings should be strictly observed, even during power up and power down. A power supply that produces a voltage spike at turn-on and/or turn-off of power can destroy the ADC08B3000. The circuit of Figure 50 will provide supply overshoot protection.

Many linear regulators will produce output spiking at power-on unless there is a minimum load provided. Active devices draw very little current until their supply voltages reach a few hundred millivolts. The result can be a turn-on spike that can destroy the ADC08B3000, unless a minimum load is provided for the supply. The 100Ω resistor at the regulator output of Figure 50 provides a minimum output current during power-up to ensure there is no turn-on spiking. Whether a linear or switching regulator is used, it is advisable to provide a slow start circuit to prevent overshoot of the supply.

In the circuit of Figure 50, an LM317 linear regulator is satisfactory if its input supply voltage is 4V to 5V. If a 3.3V supply is used, an LM1086 linear regulator is recommended.

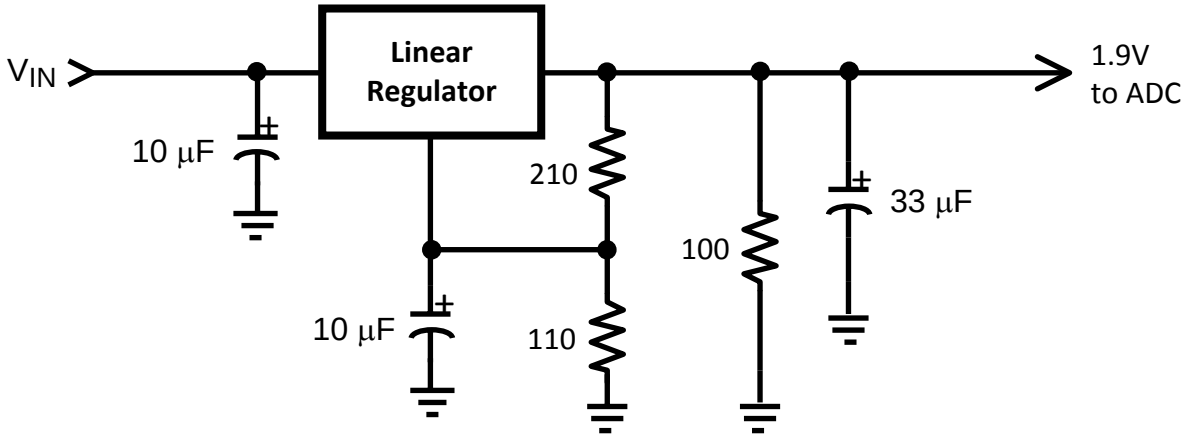


Figure 50. Non-Spiking Power Supply

The output drivers should have a supply voltage, V_{DR}, that is within the range specified in Operating Ratings. This voltage should not exceed the V_A supply voltage and should never spike to a voltage greater than (V_A + 100mV).

If the power is applied to the device without an input clock signal present, the current drawn by the device might be below 200 mA. This is because the ADC08B3000 gets reset through clocked logic and its initial state is unknown. If the reset logic comes up in the "on" state, it will cause most of the analog circuitry to be powered down, resulting in less than 100 mA of current draw. This current is greater than the power down current because not all of the ADC is powered down. The device current will be normal after the input clock is established.

Thermal Management

The ADC08B3000 is capable of impressive speeds and performance at very low power levels for its speed. However, the power consumption is still high enough to require attention to thermal management. For reliability reasons, the die temperature should be kept to a maximum of 130°C. That is, T_A (ambient temperature) plus ADC power consumption times θ_{JA} (junction to ambient thermal resistance) should not exceed 130°C. This is not a problem if the ambient temperature is kept to a maximum of +85°C as specified in Operating Ratings and the exposed pad on the bottom of the package is thermally connected to a large enough copper area of the PC board.

Please note that the following are general recommendations for mounting exposed pad devices onto a PCB. This should be considered the starting point in PCB and assembly process development. It is recommended that the process be developed based upon past experience in package mounting.

The package of the ADC08B3000 has an exposed pad on its back that provides the primary heat removal path as well as excellent electrical grounding to the printed circuit board. The land pattern design for lead attachment to the PCB should be the same as for a conventional HLQFP, but the exposed pad must be attached to the board to remove the maximum amount of heat from the package, as well as to ensure best product parametric performance.

To maximize the removal of heat from the package, a thermal land pattern must be incorporated on the PC board within the footprint of the package. The exposed pad of the device must be soldered down to ensure adequate heat conduction out of the package. The land pattern for this exposed pad should be at least as large as the 5 x 5 mm of the exposed pad of the package and be located such that the exposed pad of the device is entirely over that thermal land pattern. This thermal land pattern should be electrically connected to ground. A clearance of at least 0.5 mm should separate this land pattern from the mounting pads for the package pins.

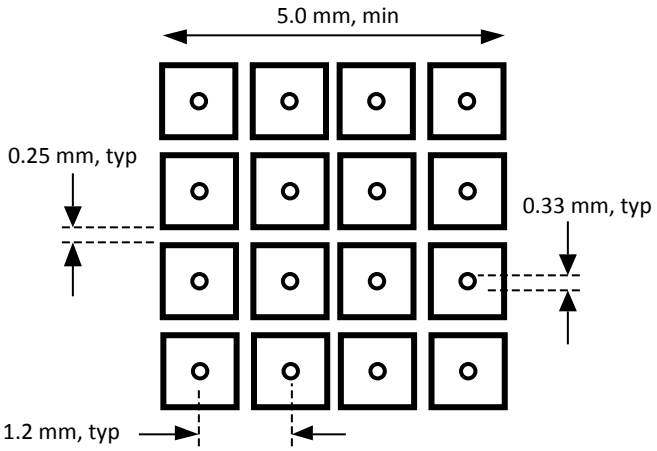


Figure 51. Recommended Package Exposed Pad Land Pattern

Since a large aperture opening may result in poor release, the aperture opening should be subdivided into an array of smaller openings, similar to the land pattern of Figure 51.

To minimize junction temperature, it is recommended that a simple heat sink be built into the PCB. This is done by including a copper area of about 2 square inches (6.5 square cm) on the opposite side of the PCB. This copper area may be plated or solder coated to prevent corrosion, but should not have a conformal coating, which could provide some thermal insulation. Thermal vias should be used to connect these top and bottom copper areas. These thermal vias act as "heat pipes" to carry the thermal energy from the device side of the board to the opposite side of the board where it can be more effectively dissipated. The use of 9 to 16 thermal vias is recommended.

The thermal vias should be placed on a 1.2 mm grid spacing and have a diameter of 0.30 to 0.33 mm. These vias should be barrel plated to avoid solder wicking into the vias during the soldering process as this wicking could cause voids in the solder between the package exposed pad and the thermal land on the PCB. Such voids could increase the thermal resistance between the device and the thermal land on the board, which would cause the device to run hotter.

If it is desired to monitor die temperature, a temperature sensor may be mounted on the heat sink area of the board near the thermal vias. Allow for a thermal gradient between the temperature sensor and the ADC08B3000 die of $\theta_{J\text{-}PAD}$ times typical power consumption = 2.8 x 1.9 = 5.3°C. Allowing for 6.3°C, including some margin for temperature drop from the pad to the temperature sensor, then, would mean that maintaining a maximum pad temperature reading of 123.7°C will ensure that the die temperature does not exceed 130°C, assuming that the exposed pad of the ADC08B3000 is properly soldered down and the thermal vias are adequate. (The inaccuracy of the temperature sensor is additional to the above calculation).

LAYOUT AND GROUNDING

Proper grounding and proper routing of all signals are essential to ensure optimum performance. A single ground plane should be used instead of splitting the ground plane into analog and digital areas.

Since digital switching transients are composed largely of high frequency components, the skin effect tells us that total ground plane copper weight will have little effect upon the logic-generated noise. Total surface area is more important than is total ground plane volume. Coupling between the typically noisy digital circuitry and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

High power digital components should not be located on or near any linear component or power plane that services analog or mixed signal components as the resulting common return current path could cause fluctuation in the analog input “ground” return of the ADC, resulting in excessive noise in the conversion result.

Generally, we assume that analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. The input clock lines should be isolated from ALL other lines, analog AND digital. The generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies is obtained with a short, straight signal path.

The analog input should be isolated from other signal traces to avoid coupling of spurious signals into the input. This is especially important with the low level drive required of the ADC08B3000. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane. All analog circuitry (input amplifiers, filters, etc.) should be separated from any digital components.

DYNAMIC PERFORMANCE

The ADC08B3000 is a.c. tested and its dynamic performance is ensured. To meet the published specifications and avoid jitter-induced noise, the clock source driving the CLK input must exhibit low rms jitter. The allowable jitter is a function of the input frequency and the input signal level, as described in THE SAMPLE CLOCK INPUT.

It is good practice to keep the ADC input clock line as short as possible, to keep it well away from any other signals and to treat it as a transmission line. Other signals can introduce jitter into the input clock signal. The clock signal can also introduce noise into the analog path if not isolated from that path.

Best dynamic performance is obtained when the exposed pad at the back of the package has a good connection to ground. This is because this path from the die to ground is of lower impedance than offered by the package pins.

USING THE SERIAL INTERFACE

The ADC08B3000 may be operated in the non-extended control (non-Serial Interface) mode or in the extended control mode. Table 15 and Table 16, below, describe the functions of pins 3, 4, 14 and 127 in the non-extended control mode and the extended control mode, respectively.

Non-Extended Control Mode Operation

Non-extended control mode operation means that the Serial Interface is not active and all controllable functions are controlled with various pin settings. That is, the output voltage swing, full-scale range and output edge selections are all controlled with pin settings. The non-extended control mode is used by setting pin 14 high or low, as opposed to letting it float. Table 15 indicates the pin functions of the ADC08B3000 in the non-extended control mode.

Table 15. Non-Extended Control Mode Operation (Pin 14 High or Low)

Pin	Low	High	Floating
4	OutEdge = Neg	OutEdge = Pos	DDR
14	600 mV_{P-P} input range	810 mV_{P-P} input range	Extended Control Mode
127	CalDly Low	CalDly High	Serial Interface Enable

Pin 4 can be high or low or can be left floating in the non-extended control mode. In the non-extended control mode, pin 4 high or low defines the edge at which the output data transitions. See NORMAL/EXTENDED CONTROL for more information. If this pin is floating, the output clock (DRDY) is a DDR (Double Data Rate) clock (see Double Data Rate) and the output edge synchronization is irrelevant since data is clocked out on both DRDY edges.

If pin 127 is high or low in the non-extended control mode, if sets the calibration delay time. If pin 14 is floating, the calibration delay is the short one and pin 127 acts as the enable pin for the serial interface input.

Table 16. Extended Control Mode Operation (Pin 14 Floating)

Pin	Function
3	SCLK (Serial Clock)
4	SDATA (Serial Data)
127	$\overline{SCS}$ (Serial Interface Select)

COMMON APPLICATION PITFALLS

Failure to write all register locations when using extended control mode. When using the serial interface, all six address locations must be written at least once with the default or desired values before calibration and subsequent use of the ADC.

Driving the inputs (analog or digital) beyond the power supply rails. For device reliability, no input should go more than 150 mV below the ground pins or 150 mV above the supply pins. Exceeding these limits on even a transient basis may not only cause faulty or erratic operation, but may impair device reliability. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground. Controlling the impedance of high speed lines and terminating these lines in their characteristic impedance should control overshoot.

Care should be taken not to overdrive the inputs of the ADC08B3000. Such practice may lead to conversion inaccuracies and even to device damage.

Incorrect analog input common mode voltage in the d.c. coupled mode. As discussed in The Analog Inputs and THE ANALOG INPUT, the Input common mode voltage must remain within 50 mV of the V_{CMO} output, which has a variability with temperature that must also be tracked. Distortion performance will be degraded if the input common mode voltage is more than 50 mV from V_{CMO}.

Using an inadequate amplifier to drive the analog input. Use care when choosing a high frequency amplifier to drive the ADC08B3000 as many high speed amplifiers will have higher distortion than will the ADC08B3000, resulting in overall system performance degradation.

Driving the V_{BG} pin to change the reference voltage. As mentioned in THE REFERENCE VOLTAGE, the reference voltage is intended to be fixed to provide one of two different full-scale values in the Normal Mode, or a range of full-scale values in the Extended Control Mode. The reference can not be changed by driving the V_{BG} pin, which should not driven.

Driving the clock input with an excessively high level signal. As described in THE SAMPLE CLOCK INPUT, the ADC input clock level should not exceed the level described in Operating Ratings or the input offset could change and a degradation of SFDR and SNR could result.

Inadequate input clock levels. As described in THE SAMPLE CLOCK INPUT, insufficient input clock levels can result in poor performance.

Using a clock source with excessive jitter, using an excessively long input clock signal trace, or having other signals coupled to the input clock signal trace. Any of these will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance.

Driving an LVCMOS input with LVPECL. The common mode voltage of LVPECL is too high, so the ADC08B3000 may not properly interpret the input, so recognition of the intended function may be marginal, intermittent, or non-existent.

Accessing the internal registers while a calibration is in process. As indicated in Calibration and THE SERIAL INTERFACE, the internal registers (via the serial port) should not be accessed during calibration. Doing so will impair the performance of the device until it is re-calibrated correctly.

Failure to strictly observe ADCCLK_RST set-up and hold times. The deassertion edge of the ADCCLK_RST pulse must observe the specified setup and hold times (t_{SR}, t_{SH}). See MULTIPLE ADC SYNCHRONIZATION. Allowing for timing uncertainty in this timing is also important.

Failure to provide adequate heat removal. As described in Thermal Management, it is important to provide adequate heat removal to ensure device reliability. This can be done either with adequate air flow or the use of a simple heat sink built into the board. The backside pad should be grounded for best performance.

REVISION HISTORY

Changes from Revision L (April 2013) to Revision M	Page
• Changed layout of National Data Sheet to TI format	52

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC08B3000CIYB/NOPB	ACTIVE	HLQFP	NNB	128	60	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	ADC08B3000 CIYB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

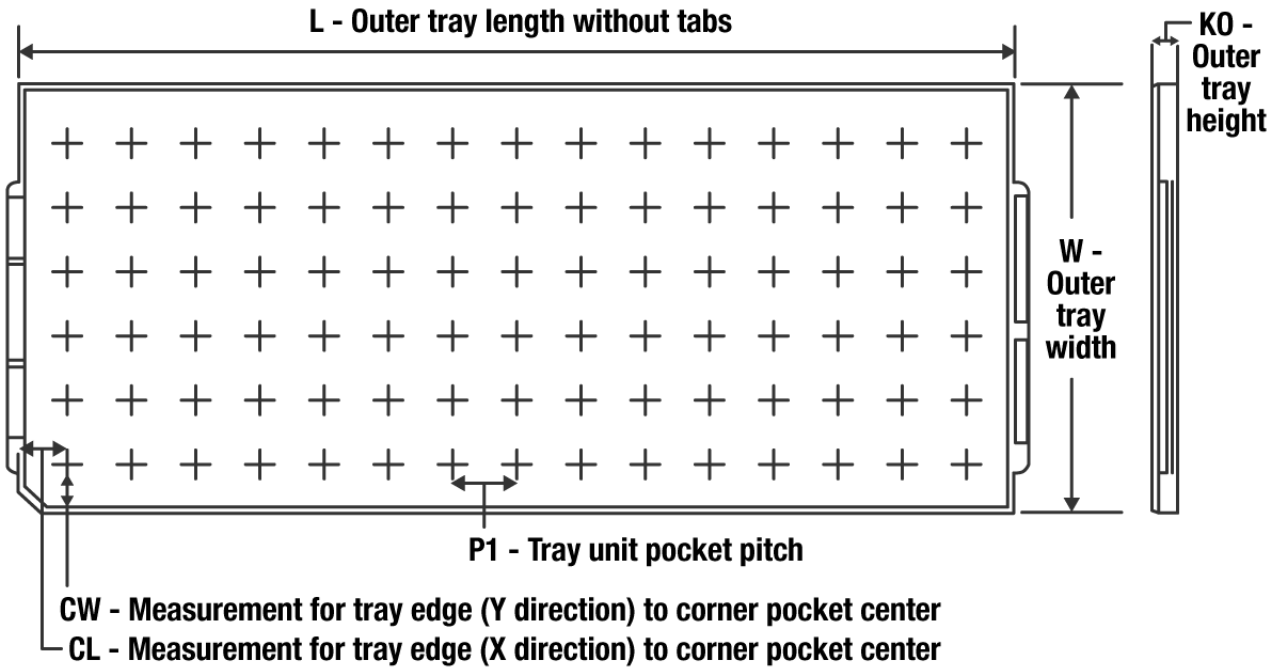
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TRAY

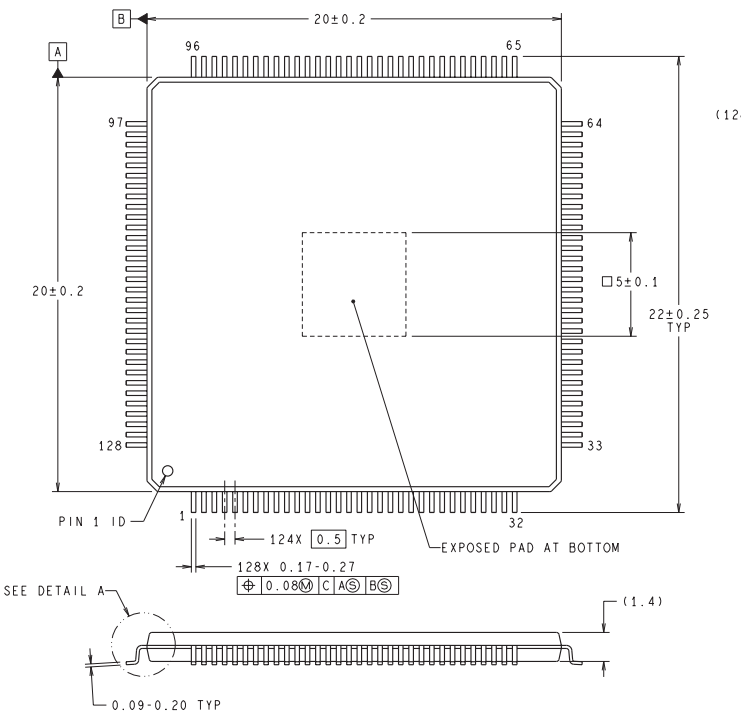


Chamfer on Tray corner indicates Pin 1 orientation of packed units.

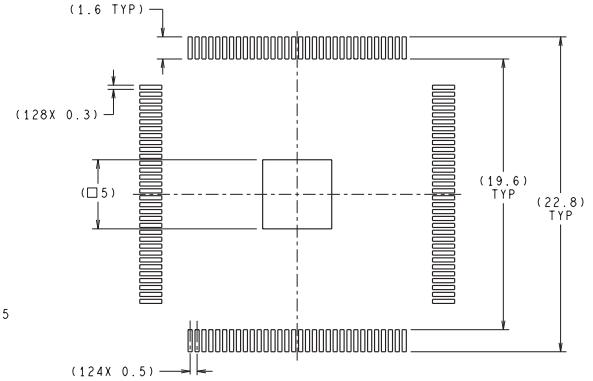
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC08B3000CIYB/NOPB	NNB	HLQFP	128	60	5 X 12	150	322.6	135.9	7620	25.4	17.8	17.55

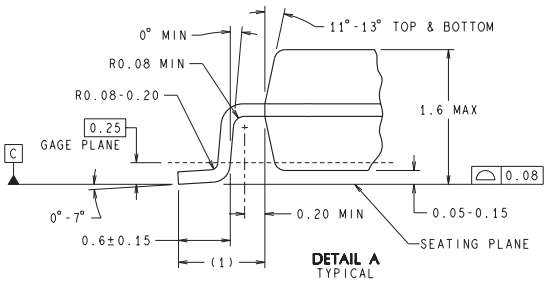
NNB0128A



DIMENSIONS ARE IN MILLIMETERS



RECOMMENDED LAND PATTERN



DETAIL A
TYPICAL

VNX128A (Rev B)

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265