Si5383/84 Reference Manual

Overview

This Reference Manual is intended to provide system, PCB design, signal integrity, and software engineers the necessary technical information to successfully use the Si5383/84 devices in end applications. The official device specifications can be found in the Si5383/84 data sheet.

The Si5383/84 combines the industry's smallest footprint and lowest power network synchronizer clock with unmatched frequency synthesis flexibility and ultra-low jitter. The three independent DSPLLs are individually configurable as a SyncE PLL or a general-purpose PLL for processor/FPGA clocking, and support digitally controlled oscillator (DCO) mode for IEEE 1588 (PTP) clock steering applications. In addition, locking to a 1 pps input frequency is available on DSPLL D. The DCO mode provides precise timing adjustment to 1 part per trillion (ppt). The Si5383/84 can also be used in legacy SETS systems needing Stratum 3/3E compliance. The unique design of the Si5383/84 allows the device to accept a TCXO/OCXO with any frequency, and the reference clock jitter does not degrade output performance. The Si5383/84 is configurable via a serial interface with in-circuit programmable non-volatile memory so it always powers up into a known configuration. Programming the Si5383/84 is easy with ClockBuilder Pro software. Factory pre-programmed devices are also available.

RELATED DOCUMENTS

- Si5383/84 Data Sheet
- Si5383/84 Device Errata
- Si5383-EVB User Guide
- Si5383-EVB Schematics, BOM & Layout
- IBIS models
- To download support files, go to: 16. Accessing Design and Support Collateral

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1. Scope

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1.1 Related Documents

- Si5383/84 Data Sheet
- Si5383/84-EVB User Guide
- SiOCXO1-EVB User Guide

2. Overview

The Si5383/84 is a high performance, jitter attenuating clock multiplier with capabilities to address Telecom Boundary Clock (T-BC), Synchronous Ethernet (SyncE), IEEE-1588 (PTP) slave clock synchronization, and Stratum 3/3E network synchronization applications. The Si5383/84 is well suited for both traditional and packet-based network timing solutions. The Si5383/84 contains three independent DSPLLs allowing for flexible single-chip timing architecture solutions. The Si5383 contains a single DSPLL D that can be configured for 1PPS applications to lock to a 1 Hz input, requiring no additional external circuitry. Each DSPLL contains a digitally controlled oscillator (DCO) for precise timing for IEEE 1588 (PTP) clock steering applications. The Si5383/84 requires both a crystal and a reference input. The TCXO/OCXO reference input determines the frequency accuracy in Free Run and stability in Holdover, while the crystal determines the output jitter performance. The TCXO/OCXO input supports all standard frequencies. Each DSPLL has access to IN0, IN1, and IN2, which are the three main inputs for synchronizing the DSPLLs. DSPLL D has access to two additional CMOS only inputs, IN3 and IN4. Each DSPLL can provide low jitter clocks on any of the device outputs. Based on 4th generation DSPLL technology, these devices provide any-frequency generation. Each DSPLL supports independent free-run and holdover modes of operation, and except for 1PPS inputs, offers automatic and hitless input clock switching. The Si5383/84 is programmable via a serial I2C interface with in-circuit programmable non-volatile memory so that it always powers up with a known configuration. Programming the Si5383/84 is made easy with Skyworks' ClockBuilder Pro software available at https://www.skyworksinc.com/en/application-pages/clockbuilder-pro-software. Factory preprogrammed devices are available.

2.1 Work Flow Using ClockBuilder Pro and the Register Map

The purpose of this reference manual is to describe all the functions and features of the devices in the product family with register map details on how to implement them. Customers should use the ClockBuilder Pro software to provide the initial configuration for the device. Although the register map is documented, all the details of the algorithms to implement a valid frequency plan are fairly complex and are beyond the scope of this document. Real-time changes to the frequency plan and other operating settings are supported by the devices. However, describing all the possible changes is not a primary purpose of this document. Refer to Applications Notes and Knowledge Base article links within the ClockBuilder Pro GUI for information on how to implement the most common, real-time frequency plan changes.

The primary purpose of the software is to enable use of the device without an in-depth understanding of its complexities. The software abstracts the details from the user to allow focus on the high level input and output configuration, making it intuitive to understand and configure for the end application. The software walks the user through each step, with explanations about each configuration step in the process to explain the different options available. The software will restrict the user from entering an invalid combination of selections. The final configuration settings can be saved and written to an EVB, and a custom part number can be created for customers who prefer to order a factory preprogrammed device. The final register maps can be exported to text files, and comparisons can be done by viewing the settings in the register map described in this document.

The Si5383 offers three DSPLLs - A,C,D - and the Si5384 offers DSPLLD exclusively. The Reference Manual includes registers for all DSPLL's however DSPLLA and DSPLLC do not apply to the Si5384. The reference to "Standard Input Mode" applies to input frequencies between 8 kHz and 750 MHz whereas any reference to "1PPS Mode" applies to a 1 Hz input frequency.

2.2 Product Family

The table below lists a comparison of the various Si5383/84 family members.

Table 2.1. Product Selection Guide

Part Number	Max Frequency	Package Type	RoHS/Lead-Free	Temperature Range
Si5383A-Dxxxxx-GM	718.5 MHz	56-Lead 8x8 LGA	Yes	-40 to 85 °C
S5383B-Dxxxxx-GM	350 MHz	56-Lead 8x8 LGA	Yes	-40 to 85 °C
Si5384A-Dxxxxx-GM	718.5 MHz	56-Lead 8x8 LGA	Yes	-40 to 85 °C
Si5384B-Dxxxxx-GM	350 MHz	56-Lead 8x8 LGA	Yes	-40 to 85 ºC
Si5383-EVB		Evaluation Board		
SiOCXO1-EVB		OCXO Reference Clock Evaluation Board for Si5383-EVB (optional)		

3. Functional Description

The Si5383/84 takes advantage of Skyworks' fourth-generation DSPLL technology to offer the industry's most integrated and flexible jitter attenuating clock generator solution. The Si5383 offers three DSPLLs and the Si5384 offers one DSPLL. Each of the DSPLLs operate independently from each other and are controlled through a common serial interface. DSPLLs (A, C, and D) all have access to any of the three inputs (IN0 to IN2), after having been divided down by the input P dividers, which are either fractional or integer. DSPLL D has access to two additional CMOS inputs (IN3 and IN4). Clock selection can be either manual or automatic except for 1PPS inputs which must be controlled by manual clock selection. Any of the output clocks (OUT0 to OUT6) can be configured to connect to any of the DSPLLs using a flexible crosspoint connection, however 1PPS outputs can only be supplied by OUT5. Both a Crystal and a Reference must be installed for the device to operate.

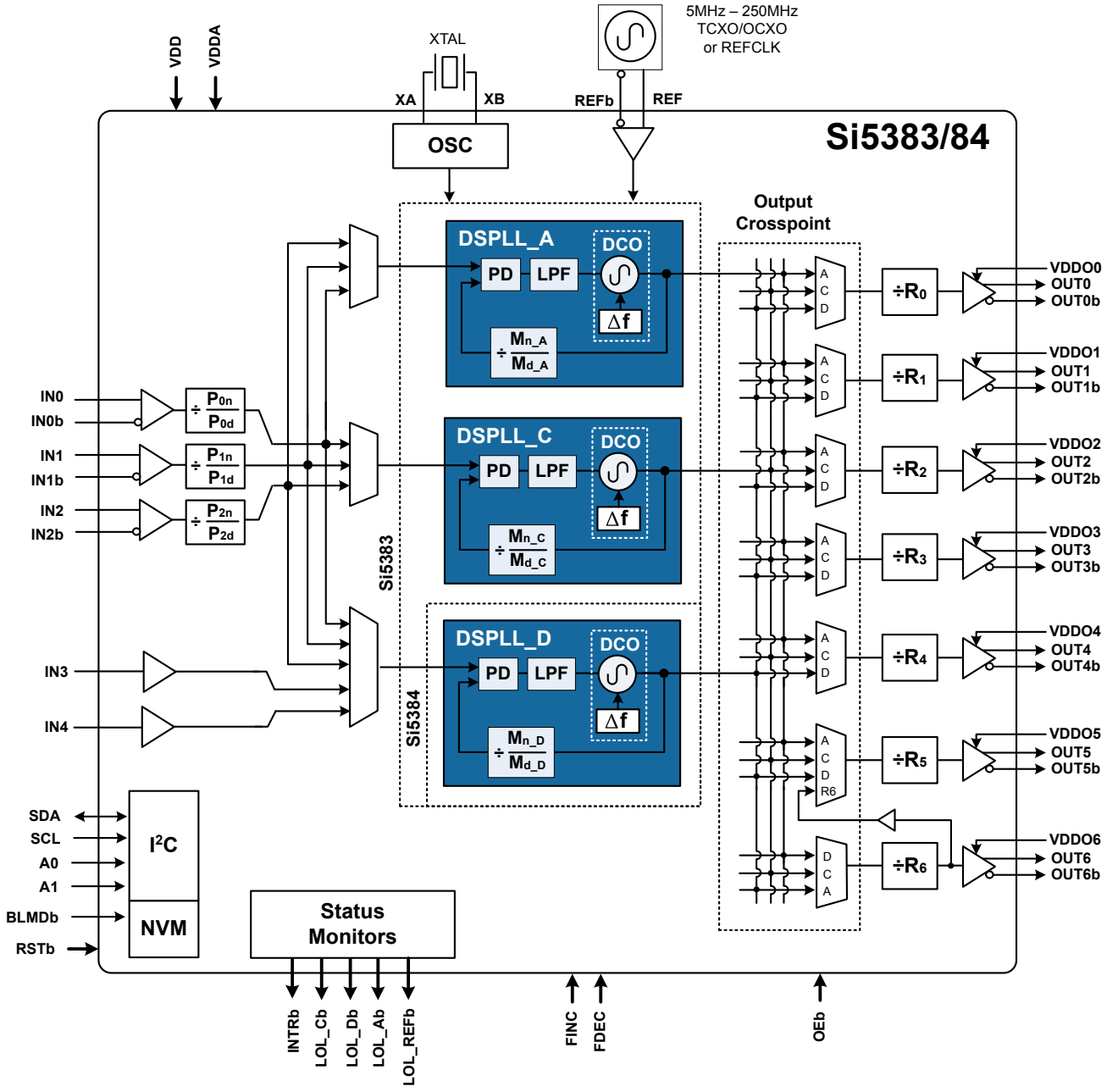


Figure 3.1. Block Diagram

3.1 DSPLL

The DSPLL is responsible for input frequency translation, jitter attenuation and wander filtering. Fractional input dividers (Pn/Pxd) allow the DSPLL to perform hitless switching between input clocks (IN0, IN1, IN2) when in standard input mode. Input switching is controlled manually in 1PPS mode and manuallly or automatically in standard input mode using an internal state machine. Automatic switching applies to any 4 inputs when in non 1PPS mode. The reference input determines the frequency accuracy while in free-run and stability while in holdover modes. The external crystal completes the internal oscillator circuit (OSC) which is used by the DSPLL for intrinsic low-jitter performance. A crosspoint switch connects any of the DSPLLs to any of the outputs. An additional integer divisor (R) determines the final output frequency.

The frequency configuration of the DSPLL is programmable through the I^2C serial interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows the generation of virtually any output frequency on any of the outputs. All divider values for a specific frequency plan are easily determined by using the ClockBuilder Pro software.

Because a jitter reference is required for all applications, either a crystal or an external clock source needs to be connected to the XAXB pins. See Chapter 10. Recommended Crystals and External Oscillators and Chapter 11. Crystal and Device Circuit Layout Recommendations for more information.

3.2 DSPLL Loop Bandwidth

The DSPLL loop bandwidth determines the amount of input clock wander and jitter attenuation. When in standard input mode register configurable DSPLL loop bandwidth settings from 1 mHz up to 4 kHz are available for selection for each of the DSPLLs and for the reference DSPLL (DSPLL B). Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (DSPLL A = 0x0414, REF B = 0x0514, DSPLL C = 0x0614, DSPLL D = 0x0715) must be set high to latch the new values into operation. SOFT_RST_PLLx will not update the BW registers so that BW_UPDATE_PLLx should typically be asserted when SOFT_RST_PLLx is asserted. Note each of these update bits will latch both loop and fastlock bandwidths.

When in 1PPS mode the loop BW selections are 1 mHz and 10 mHz. Since the loop bandwidth is controlled digitally, each of the DSPLLs will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection. All changes to PPS BW settings should take place while PPS mode is disabled, register 0x5320[0].

The higher the PLL bandwidth is set relative to the phase detector frequency (Fpfd), the more chance that Fpfd will cause a spur in the Phase Noise plot of the output clock and increase the output jitter. To guarantee the best phase noise/jitter, it is recommended that the normal PLL bandwidth be kept less than Fpfd/160 although ratios of Fpfd/100 will typically work fine.

Table 3.1. DSPLL Loop Bandwidth Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
BW_PLLA[1]	0408[7:0] - 040D[7:0]	This group of registers determine the loop bandwidth for DSPLL A, C, D and B (reference). They are all independently selectable in the range from 1 mHz up to 4 kHz. Register values determined by ClockBuilderPro.
BW_PLLC[1]	0608[7:0] - 060D[7:0]	
BW_PLLD, (Standard Input Mode)	0709[7:0] - 070E[7:0]	
BW_PLLB	0508[7:0] - 070E[7:0]	
NL_NF, NL_NI, (BW, 1PPS Mode)	0x53D1[3:0], 0x53D2[4:0]	DSPLL D has 2 loop BW settings in 1PPS mode; 1 mHz and 10 mHz.

Note:
1. Si5383 only.

3.2.1 Fastlock

Selecting a low DSPLL loop bandwidth (e.g. 0.1 Hz) will generally lengthen the lock acquisition time. The fastlock feature allows setting a temporary Fastlock Loop Bandwidth that is used during the lock acquisition process. Higher fastlock loop bandwidth settings will enable the DSPLLs to lock faster. Fastlock Loop Bandwidth settings in the range from 100 Hz up to 4 kHz are available. Once lock acquisition has completed, the DSPLL's loop bandwidth will automatically revert to the DSPLL Loop Bandwidth setting. The fastlock feature can be enabled or disabled independently for each of the DSPLLs. If enabled, when LOL is asserted, Fastlock is enabled. When LOL is not asserted, Fastlock is disabled. Note that after changing the bandwidth parameters, the appropriate BW_UPDATE_PLLx bit (0x0414,0x0514, 0x0614, 0x0715) must be set high to latch the new values into operation. Each of these update bits will latch both loop and fastlock bandwidths. For 1PPS input applications, a Smartlock feaure is incorporated instead of fastlock.

Table 3.2. Fastlock Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
FASTLOCK_AUTO_EN_PLLA[1]	042B[0]	Auto Fastlock Enable/Disable. Manual Fastlock must be 0 for this bit to have effect. 0: Disable Auto Fastlock 1: Enable Auto Fastlock (default)
FASTLOCK_AUTO_EN_PLLC[1]	062B[0]	
FASTLOCK_AUTO_EN_PLLD	072C[0]	
FASTLOCK_AUTO_EN_PLLB	052B[0]	
FAST_BW_PLLA[1]	040E[7:0] - 0413[7:0]	Fastlock bandwidth is selectable in the range of 100 Hz up to 4 kHz. Register values determined using ClockBuilder Pro.
FAST_BW_PLLC[1]	060E[7:0] - 0613[7:0]	
FAST_BW_PLLD	070F[7:0] - 0714[7:0]	
FAST_BW_PLLB	050E[7:0] - 0513[7:0]	The reference fastlock bandwidth is selectable in the range of 1mHz to 4kHz
FASTLOCK_EXTEND_EN_PLL(A,B,C,D)	0x00E5[4:7]	Enables FASTLOCK_EXTEND
FASTLOCK_EXTEND_PLLA[1]	[0x00E9[4:0] 0x00E8[7:0] 0x00E7[7:0] 0x00E6[7:0]]	Set by CBPro to minimize phase transients when switching the PLL bandwidth
FASTLOCK_EXTEND_PLLB	[0x00ED[4:0] 0x00EC[7:0] 0x00EB[7:0] 0x00EA[7:0]]	
FASTLOCK_EXTEND_PLLC[1]	[0x00F1[4:0] 0x00F0[7:0] 0x00EF[7:0] 0x00EE[7:0]]	
FASTLOCK_EXTEND_PLLD	[0x00F5[4:0] 0x00F4[7:0] 0x00F3[7:0] 0x00F2[7:0]]	
FASTLOCK_EXTEND_SCL_PLLA[1]	0x0294[3:0]	Set by CBPro
FASTLOCK_EXTEND_SCL_PLLB	0x0294[7:4]	
FASTLOCK_EXTEND_SCL_PLLC[1]	0x0295[3:0]	
FASTLOCK_EXTEND_SCL_PLLD	0x0295[7:4]	
HOLDEXIT_BW_SEL0	0x059B[6]	Set by CBPro
HOLDEXIT_BW_SEL1	0x052C[4]	Set by CBPro
LOL_SLW_VALWIN_SELX_PLL(A,B,C,D)	0x0296[3:0]	Set by CBPro,
FASTLOCK_DLY_ONSW_PLLA[1]	0x02A6[19:0]	Set by CBPro
FASTLOCK_DLY_ONSW_PLLB	0x02A9[19:0]	
FASTLOCK_DLY_ONSW_PLLC[1]	0x02AC[19:0]	
FASTLOCK_DLY_ONSW_PLLD	0x02AF[19:0]	

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
FASTLOCK_DLY_ON-LOL_EN_PLL(A,B,C,D)	0x0299[3:0]	Set by CBPro
FASTLOCK_DLY_ONLOLA[1]	0x029A[19:0]	Set by CBPro
FASTLOCK_DLY_ONLOLB	0x029D[19:0]	
FASTLOCK_DLY_ONLOLC[1]	0x02A0[19:0]	
FASTLOCK_DLY_ONLOLD	0x02A3[19:0]	

Note:
1. Si5383 only.

3.2.2 Smartlock Feature

When operating in 1PPS input mode, the Si5383/84 offers the Smartlock feature to achieve fast locking to 1PPS inputs. The Smartlock feature locks to 1PPS inputs in two phases. During the first phase, large adjustments are made to eliminate the majority of the frequency and phase error. During the second phase, finer adjustments are made until the PLL is locked. Once the PLL is locked, the DSPLLs loop bandwidth will automatically revert to the DSPLL loop bandwidth setting.

Table 3.3. Smartlock Registers

Setting Name	Hex Address [Bit Field]	Function
INIT_ACQ_TYPE	0x5320[4]	Initial Acquisition Lock B Disable - When set, acquisition doesn't wait for DSPLLB to lock before proceeding. Must be set before PPS_EN.
DCO_SCALE	0x5358[2:0]	DCO Scaling Factor -Used to keep DCO tuning range relatively constant over all frequency plans. Must be set before PPS_EN.
PP_CW_LMT	0x535C[7:0] - 0x535F[7:0]	Phase Pull Control Word Limit - - Maximum CW value to ensure DCO doesn't exceed maximum operating frequency (Fvco/10). Must be set before PPS_EN.
PD_ADJ	0x5360[7:0]-0x5363[7:0]	Phase Detector Adjustment - a 2's complement number used to modify DSPLLD outputs phase when in 1PPS mode. This is used to statically zero out or adjust the phase, such as compensating for fixed system delays. Must be set before PPS_EN.
PD_CW_2_ADJ	0x5364[7:0]-0x5367[7:0]	Phase Detector Control Word to Adjustment Conversion - Factor to convert the DCO Control Word to a PD adjustment. Must be set before PPS_EN.
SL_PER_2_ADJ	0x5368[7:0]-0x536B[7:0]	SmartLock Period to Adjustment Conversion - Factor to convert measured period difference to a DCO adjustment. Must be set before PPS_EN.
SL_PE_2_ADJ	0x536C[7:0]-0x536F[7:0]	SmartLock Phase Error to Adjustment Conversion - Factor to convert measured phase error to a DCO adjustment that achieves zero phase error in one second. Must be set before PPS_EN.
SLA_FA_CNT	0x5371[7:0]	SmartLock Frequency Average Count - The number of cycles to average the frequency difference before attempting frequency pull. Must be set before PPS_EN.
SLA_FP_NCYC	0x5372[2:0]	SmartLock Frequency Pull Cycles - The number of cycles (2^N) to complete frequency pull. Must be set before PPS_EN.
SLA_FP_VAL_CNT	0x5373[7:0]	SmartLock Frequency Pull Cycles - The number of consecutive cycles with frequency error below the threshold to complete frequency pull. Must be set before PPS_EN.

Setting Name	Hex Address [Bit Field]	Function
SLA_FE_THR	0x5374[6:0]-0x5377[7:0]	SmartLock Frequency Error Threshold - Threshold specified as the maximum difference in period between the reference and feedback clocks. Must be set before PPS_EN.
SLA_PPn_NCYC	0x5378[4:0]-0x537F[4:0]	SmartLock Phase Pull Cycles - The number of cycles (2^N) to complete phase pull. Must be set before PPS_EN.
SLA_PE_THR	0x5380[5:0]-0x5383[7:0]	SmartLock Frequency Error Threshold - Threshold specified as the maximum difference in phase between the reference and feedback clocks. Must be set before PPS_EN.
SLA_RL1_NF	0x5384[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLA_RL1_NI	0x5385[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN.
SLA_RL1_CNT	0x5386[7:0] - 0x5387[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLA_RL2_NF	0x5388[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLA_RL2_NI	0x5389[4:0]	SmartLock RapidLock, sets the loop BW. Must be set before PPS_EN.
SLA_RL2_CNT	0x538A[7:0] - 0x538B[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLA_RL3_NF	0x538C[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLA_RL3_NI	0x538D[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN.
SLA_RL3_CNT	0x538E[7:0] - 0x538F[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLA_RL4_NF	0x5390[3:0]	Smartlock RapidLock NF, sets the loop BW. Must be set before PPS_EN
SLA_RL4_NI	0x5391[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN
SLA_RL4_CNT	0x5392[7:0] - 0x5393[7:0]	SmartLock RapidLock Count - he number of cycles to remain in RapidLock state. Must be set before PPS_EN.
SLB_FA_CNT	0x53A1[7:0]	SmartLock Frequency Average Count - The number of cycles to average the frequency difference before attempting frequency pull. Must be set before PPS_EN.
SLB_FP_NCYC	0x53A2[2:0]	SmartLock Frequency Pull Cycles - The number of cycles (2^N) to complete frequency pull. Must be set before PPS_EN.

Setting Name	Hex Address [Bit Field]	Function
SLB_FP_VAL_CNT	0x53A3[7:0]	SmartLock Frequency Validation Count. - The number of consecutive cycles with frequency error below the threshold to complete frequency pull. Must be set before PPS_EN.
SLB_FE_THR	0x53A4[6:0]-0x53A7[7:0]	SmartLock Frequency Error Threshold. Threshold specified as the maximum difference in period between the reference and feedback clocks. Must be set before PPS_EN.
SLB_PPn_NCYC	0x53A8[4:0]-0x53AF[4:0]	SmartLock Phase Pull Cycles - The number of cycles (2^N) to complete phase pull. Must be set before PPS_EN.
SLB_PE_THR	0x53B0[5:0]-0x53B3[7:0]	SmartLock Phase Error Threshold - Threshold specified as the maximum difference in phase between the reference and feedback clocks. Must be set before PPS_EN.
SLB_RL1_NF	0x53B4[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLB_RL1_NI	0x53B5[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN.
SLB_RL1_CNT	0x53B6[7:0] - 0x53B7[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLB_RL2_NF	0x53B8[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLB_RL2_NI	0x53B9[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN.
SLB_RL2_CNT	0x53BA[7:0] - 0x53BB[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLB_RL3_NF	0x53BC[3:0]	SmartLock RapidLock NF, sets the loop BW. Must be set before PPS_EN.
SLB_RL3_NI	0x53BD[4:0]	SmartLock RapidLock NI, sets the loop BW. Must be set before PPS_EN.
SLB_RL3_CNT	0x53BE[7:0] - 0x53BF[7:0]	SmartLock RapidLock Count - The number of cycles to remain in the RapidLock state. Must be set before PPS_EN.
SLB_RL4_NF	0x53C0[3:0]	SmartLock Rapid LockNF, sets the loop BW. Must be set before PPS_EN
SLB_RL4_NI	0x53C1[4:0]	SmartLock Rapid LockNF, sets the loop BW. Must be set before PPS_EN
SLB_RL4_CNT	0x53C2[7:0]-0x53C3[7:0]	SmartLock Rapid Count - The number of cycles to remain in RapidLock state. Must be set beore PPS_EN.
NL_NF	0x53D1[3:0]	NormalLock NF - Feed forward coefficient used in NormalLock mode. Must be set before PPS_EN.

Setting Name	Hex Address [Bit Field]	Function
NL_NI	0x53D2[4:0]	NormalLock NI - Integrating coefficient used in NormalLock mode. Must be set before PPS_EN.
HO_EXIT_EN	0x53E0[0]]	Holdover Acquisition Type - When enabled, HOLDOVER will automatically exit and attempt reacquisition when a valid input is detected. When disabled, FORCE_HOLD will be set on entry into holdover and must be manually cleared to exit the holdover state. Must be set before PPS_EN.
FORCE_HOLD	0x53E0[1]	Holdover Force - When asserted, the PPS loop will transition from the FREERUN or LOCKED states to the HOLDOVER state. It will remain in this state until the force is removed.
HO_ACQ_TYPE	0x53E0[5:4]	Holldover Acquisition Type - Determines the acquisition mode when holdover is exited. Must be set before PPS_EN.
HOLD_HIST_LEN	0x53E1[2:0]	Holdover History Length - Specifies the holdover window size. Larger windows provide more averaging. Must be set before PPS_EN.
HOLD_HIST_DELAY	0x53E2[4:0]	Holdover History Lengthy - Specifies the holdover delay time. Delay value allows ignoring corrupt frequency data before the input clock failure. Must be set before PPS_EN.

3.3 Dividers Overview

The frequency configuration for each of the DSPLLs is programmable through the I2C interface and can also be stored in non-volatile memory. The combination of fractional input dividers (Pn/Pd), fractional frequency multiplication (Mn/Md), and integer output division (Rn) allows each of the DSPLLs (A,C,D) to lock to any input frequency and generate virtually any output frequency. All divider values for a specific frequency plan are easily determined using the ClockBuilder Pro utility.

There are five main divider classes within the Si5383/84. See Chapter 3. Functional Description for a block diagram that shows them. Additionally, the DCO step word is used to scale the nominal output frequency in DCO mode. See Chapter 7. Digitally Controlled Oscillator (DCO) Mode for more information and block diagrams on DCO mode.

- PXAXB: XAXB Crystal / Reference input divider (0x0206)
  - XAXB Divide clock by 1, 2, 4, or 8 to obtain an internal clock <= 54 MHz
- P0-P3: Input clock wide range dividers (0x0208-0x022F)
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24} (Fractional-P divisors must be > 5)
  - 48-bit numerator, 32-bit denominator
  - Practical P divider range of (Fin/2 MHz) < P < (Fin/8 kHz)
  - Each P divider has a separate update bit for the new divider value to take effect
- MA-MD: DSPLL feedback dividers (0x0415-0x041F, 0x0515-0x051F, 0x0615-0x061F, 0x0716-0x0720))
  - Integer or Fractional divide values
  - Min. value is 1, Max. value is 2^{24}
  - 56-bit numerator, 32-bit denominator
  - Practical M divider range of (Fdco/2 MHz) < M < (Fdco/8 kHz)
  - Each M divider has a separate update bit for the new divider value to take effect
  - Soft reset will also update M divider values
- FSTEPW: DSPLL DCO step words (0x0423-0x0429, 0x0623-0x0629, 0x0724-0x072A)
  - Positive Integers, where FINC/FDEC select direction
  - Min. value is 0, Max. value is 2^{24}
  - 56-bit step size, relative to 32-bit M numerator
- R0-R6: Output dividers (0x0250-0x026A)
  - Even integer divide values: 2, 4, 6, etc.
  - Min. value is 2, Max. value is 2^{24}
  - 24-bit word where Value = 2 x (Word + 1), for example Word=3 gives an R value of 8

4. Modes of Operation

Once initialization is complete, each of the DSPLLs operates independently in one of four modes: Free-run mode, Lock Acquisition Mode, Locked Mode, or Holdover Mode. A state diagram showing the modes of operation is shown in the figure below. The following sections describe each of these modes in greater detail.

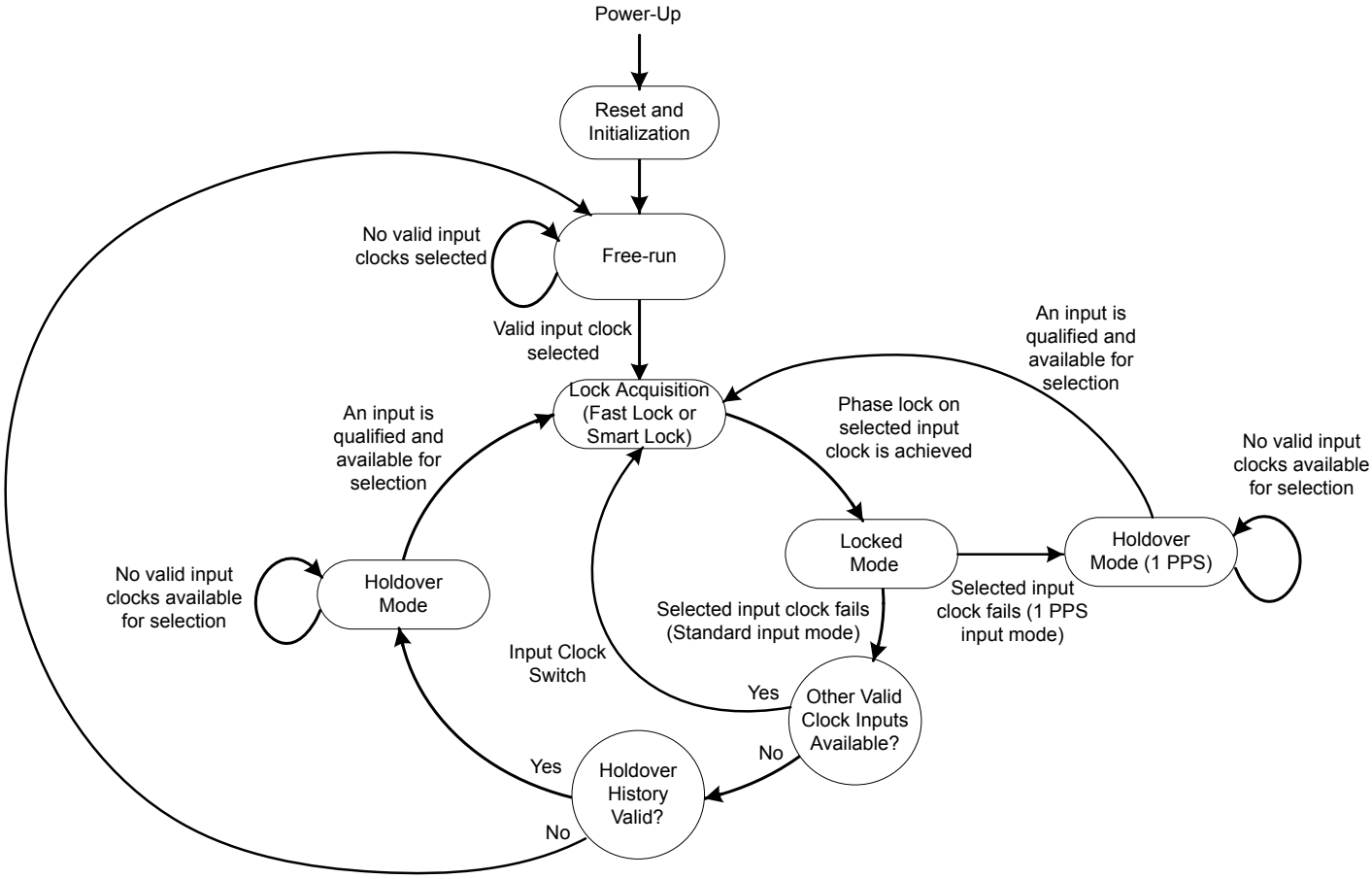


Figure 4.1. Modes of Operation

4.1 Reset and Initialization

Once power is applied, the device begins an initialization period where it downloads default register values and configuration data from NVM and performs other initialization tasks. Communicating with the device through the serial interface is possible once this initialization period is complete. No clocks will be generated until the initialization is complete. It is recommended that the device be held in reset on power-up by asserting the RSTb pin. RSTb should be released once all supplies have reached operational levels. Note, RSTb also functions as an open-drain output and drives low during POR. External devices must be configured as open-drain to avoid contention.

There are two types of resets available. A hard reset is functionally similar to a device power-up. All registers will be restored to the values stored in NVM, and all circuits will be restored to their initial state including the serial interface. A hard reset is initiated using the RSTb pin or by asserting the hard reset bit. A soft reset bypasses the NVM download. It is simply used to initiate register configuration changes. A hard reset affects all DSPLLs, while a soft reset can affect all or each DSPLL individually.

Table 4.1. Reset Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
HARD_RST	5303[0]	Performs the same function as power cycling the device. All registers will be restored to their default values.
SOFT_RST_ALL	001C[0]	Resets the device without re-downloading the register configuration from NVM.
SOFT_RST_PLLA[1]	001C[1]	Performs a soft reset on DSPLL A only.
SOFT_RST_PLLB	001C[2]	Performs a soft reset on DSPLL B, affecting all PLLs.
SOFT_RST_PLLC[1]	001C[3]	Performs a soft reset on DSPLL C only.
SOFT_RST_PLLD	001C[4]	Performs a soft reset on DSPLL D only.

Note:
1. Si5383 only.

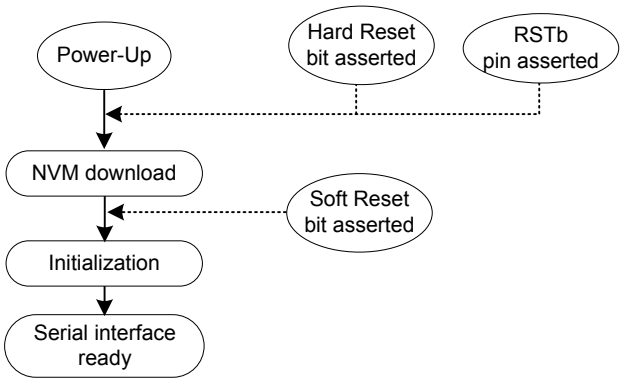


Figure 4.2. Initialization from Hard Reset and Soft Reset

The Si5383/84 is fully configurable using the serial interface (I^2C). At power-up the device downloads its default register values from internal non-volatile memory (NVM). Application specific default configurations can be written into flash memory allowing the device to generate specific clock frequencies at power-up. Writing default values to the flash memory is in-circuit programmable with normal operating power supply voltages applied to its VDD (1.8 V) and VDDA (3.3 V) pins. VDDOx supply is not required to write the flash memory.

4.2 Changing Registers while Device in Operation

ClockBuilder Pro generates all necessary control register writes for the entire device, including the ones described below. This is the case for both “Export” generated files as well as when using the GUI. This is sufficient to cover most applications. However, in some applications it is desirable to modify only certain sections of the device while maintaining unaffected clocks on the remaining outputs. If this is the case, please contact Skyworks Technical Support for further information: https://www.skyworksinc.com/support-ia .

If certain registers are changed while the device is in operation, it is possible for the PLL to become unresponsive (i.e. lose lock indefinitely). The following are the affected registers:

Table 4.2. Registers Affecting PLL Lock Status

Control	Register(s)
XAXB_FREQ_OFFSET	0x0202 – 0x0205
PXAXB	0x0206[1:0]
MXAXB_NUM	0x0235 – 0x023A
MXAXB_DEN	0x023B – 0x023E

The issue can easily be avoided by using the following preamble and post-amble write sequence below when one of these registers is modified or large frequency steps are made. ClockBuilder Pro software adds these writes to the output file by default when Exporting Register Files. Preamble and post-amble writes should be included when writing upon initilization, power-up, hard reset and RSTb.

1. To start, write the preamble by updating the following Write sequences:

Table 4.3. Preamble Sequence

Register	Value
0x0B24	0xC0
0x0B25	0x04
0x0540	0x01

2. Disable 1PPS mode, if used, by writing a 0 to register 5320[0].
3. Wait 300 ms.
4. Then modify all desired control registers.
5. Write 0x01 to Register 0x001C (SOFT_RST_ALL) to perform a Soft Reset once modifications are complete.
6. Write the post-amble by updating the following Write sequences:

Table 4.4. Postamble Sequence

Register	Value
0x0540	0x00
0x0B24	0xC3
0x0B25	0x06

7. Enable 1PPS mode, if used, by writing a 1 to register 5320[1]

Note, however, that this procedure affects all DSPLLs and outputs on the device. For assistance in changing only certain portions of the device without affecting the other outputs while the device is operating, please contact Skyworks technical support using the link on the last page of this document.

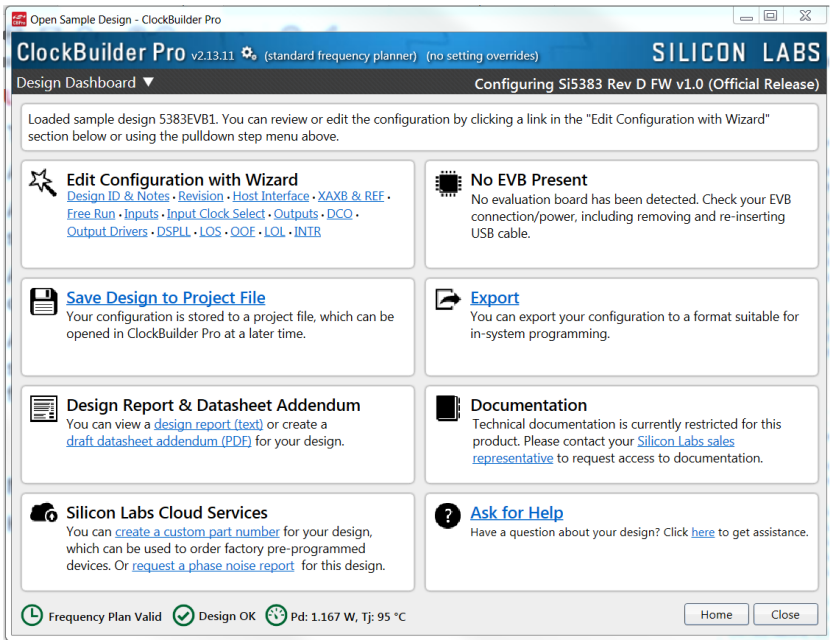
4.3 Flash Update/Programming

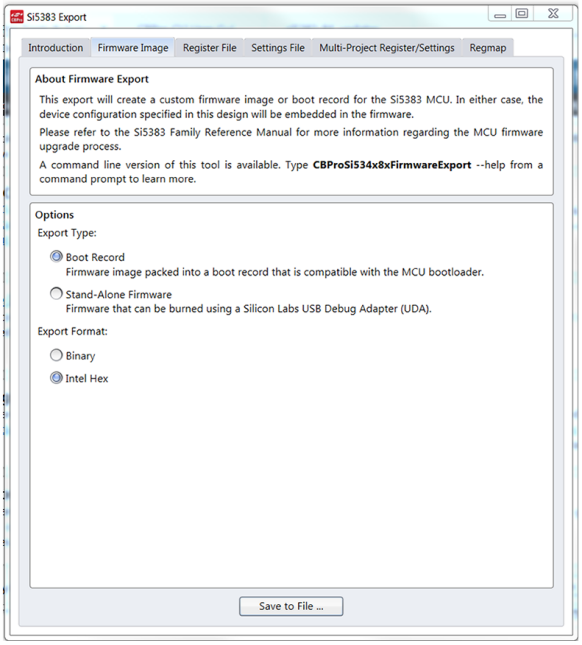
CBPro software is used to generate desired project files which include input/output frequency selection, output logic formats, loop BW values and a variety of associated PLL controls and alarm settings. The CBPro project file and Si5383 EVB can be tested to verify the Si5383/84 works as intended in the application.

Once complete, there are a variety of files which can be saved using the Export command and includes the Firmware Image, Register File, Settings File, Multi-Project Register Settings and RegMap. The Firmware Image should be saved in Boot Record or Stand Alone mode, the most common method would be Boot Record, and in either Intel hex or Binary format. From this, the hex or binary file is loaded into the Si5383/slave to update a frequency plan and firmware update, by using an I2C master. The I2C master is either Skyworks supported - by using the Si5383 EVB or Field Programmer - or by the users I2C master.

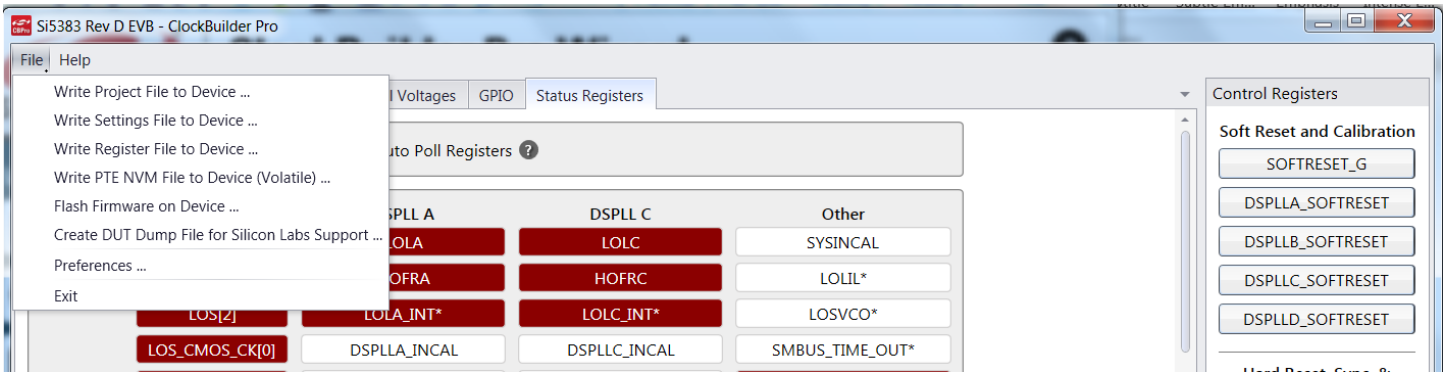
4.3.1 Upgrading Flash Firmware Image using Skyworks Tools

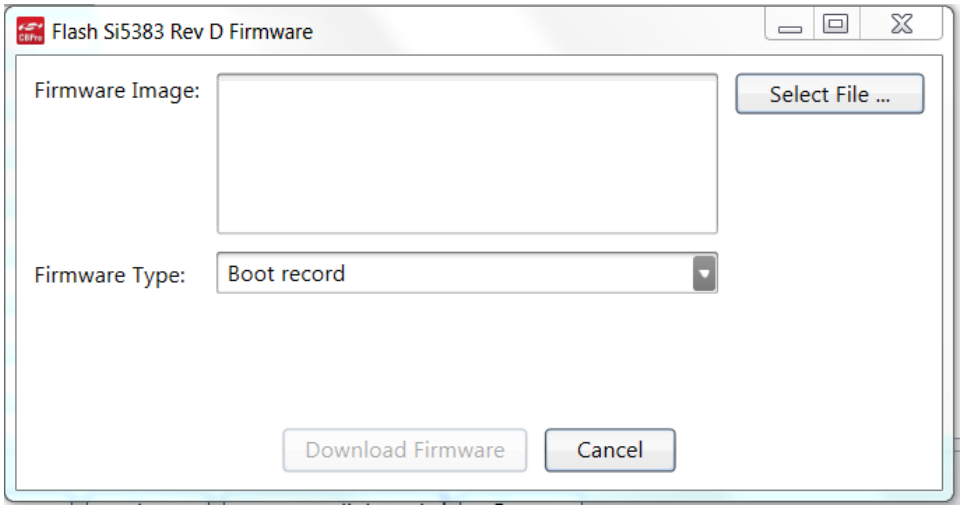
A Firmware Image can be written to an Si5383, on an Si5383 EVB, or by using a CBPROG-Dongle and Si538x4x-56SKT-DK / socket board hardware *(*ClockBuilder Pro Field Programmer*)*with CBPro software or CLI commands. Once a frequency plan has been built and verified, the required Firmware Image should be saved by selecting “Export” then “Firmware Image.” Select “Boot Record” or “Standalone,” and then either “Intel Hex” or “Binary” format. Additionally, Register File, Settings File, RegMap and MultiProject Register Settings, if applicable, can be saved in the Si5383 Export GUIs, as well as saving the Project File and design report (text) in the ClockBuilderPro GUI .





Once the Firmware Image has been saved it can be downloaded to devices by either using CBPro or CLI commands. If using CBPro, open the EVB GUI and select “File “and “Flash Firmware on Device” and locate where the file is located, plus whether it’s a bootloader or a standalone file, then select “Download Firmware”. The Si5383 will now be loaded with a new Firmware Image.





CBpro includes a series of command line interface tools, CLI, which are thoroughly detailed in “CBPro Tools & Support for In-System Programming” and “CBPro CLI User’s Guide”. These are normally downloaded along with CBPro and should be located in `C:\Program Files (x86)\Silicon Laboratories\ClockBuilder Pro\Docs`. A CLI can also be used to flash the Firmware Image, which includes the project plan, and firmware revision updates if applicable.

The CLI tool used to flash the Firmware Image is the “CBProSi534x8xFirmwareExport”. The command line can be located by typing “command prompt” in the window's search tool, and a base directory can be selected by typing `cd C:\` . Once a frequency plan has been built and verified, the required Firmware Image should be saved by selecting the “Export”, “Firmware Image,” and then, in most cases, “Boot Record” – which includes either Intel Hex or Binary format. Additionally, Register File, Settings File, RegMap, and MultiProject Register Settings, if applicable, can be saved for bookkeeping.

The Firmware Image is then downloaded using a command write, as an example `CBProSi53488xFirmwareDownload.exe --bootrecord-file` *`si5383file.hex`* (this is the hex or bin file saved). Below is an example of a successful download.

```
C:\>CBProSi534x8xFirmwareDownload.exe --bootrecord-file si5383_April11-Boot-Reco
rd.hex
Firmware file is si5383_April11-Boot-Record.hex
Parsing firmware file ...
Trying to send device to bootloader mode ...
Success
Flashing firmware ...
0% complete
5% complete
10% complete
15% complete
20% complete
25% complete
30% complete
35% complete
40% complete
45% complete
50% complete
55% complete
60% complete
65% complete
70% complete
75% complete
80% complete
85% complete
90% complete
95% complete
100% complete
Verifying flash ...
Firmware flash complete
Trying to connect to device
Detected Si5383 in program mode
FIRMWARE_TYPE is 0
FIRMWARE_MAJOR_REV is 1
FIRMWARE_MINOR_REV is 0
FIRMWARE_BUILD is 19
DESIGN_IDx is 5383EUB1
```

In this example, the hex file was copied into the `C:\ directory`, otherwise a pathname needs to be identified.

The full Firmware Export command is:

```
CBProSi534x8xFirmwareExport --bootrecord (or standalone)-file --format bin (or hex)
--project pathname --outfile pathname
```

```
The help command is: “CBProSi534x8xFirmwareExport –help”

Additional information on CBProSi534x8xFirmwareExport command options:

--format bin|hex = the file format: binary or Intel Hex.

--outfile pathname = the file to save the firmware to. If this file already exists, it will
be overwritten. You must specify this.

--project pathname = the CBPro project file. The configuration present in this design will
be embedded in the firmware.

--type bootrecord|standalone = the type of firmware image to create: boot record that can be used with
bootloader or stand-alone firmware image.

--version - print this program's version number and exit.
```

The CBProDONGLE and Si538x4x-56SKT-DK socket board can also be used to flash a Firmware Image. See the UG286: ClockBuilderPro Field Programmer Kit for more information. *(*ClockBuilder Pro Field Programmer*).* The CBPro-DONGLE can be used to flash a Firmware Image on a users PCB design as well, if similar pin connections and accommodations are made to the Si5383/84 layout, as those on the Si538x4x-56SKT-DK. The CBProDONGLE, socket board, plus Si5383/4 devices also make it easier to try new DSPLLn modifications, such as design verification or prototyping.

4.3.2 Upgrading Firmware Image Using I²C Master Routine

Updating Firmware Image is a four-step process:

1. Create and verify a Project Plan, saves Firmware Image plans, hex and or bin files etc as previously described.
2. Put the device in bootloader mode, either by write commands or hardware settings (as described in 4.3.2.1 Place in Bootloader Mode).
3. Take the `.bin` or `.hex` file and break up the file into separate boot records, which are a list of arrays. Each boot record starts with a frame start byte (0x24) and then has a data length number, which will allow the boot records to be separated. This is explained in 4.3.2.1 Place in Bootloader Mode.
4. Write in each boot record separately over I²C .

   Note: Either set up ack polling or put in delays of 20 ms for each boot record. The 3rd from last boot record is the CRC check which may take up to 6 seconds to complete. This is explained in 4.3.2.1 Place in Bootloader Mode. After each boot record has been accepted by the bootloader a reply will be sent back. The bootloader reply response codes are described in 4.3.5 Bootloader Reply Response Codes. Details for step 2 -4 follows.

4.3.2.1 Place in Bootloader Mode

The first step to updating the Firmware Image is to put the Si5383/84 in bootloader mode. This is a two-step write process to register 0x05:

- 0x05, 0x57
- 0x05, 0xBA

This two-key sequence is used to avoid putting the Si5383/84 in bootloader mode erroneously upon other writes. After writing the register sequence, the Si5383/84 should be in bootloader mode.

The second method (the hardware method) for putting the device in bootloader mode is to do the following:

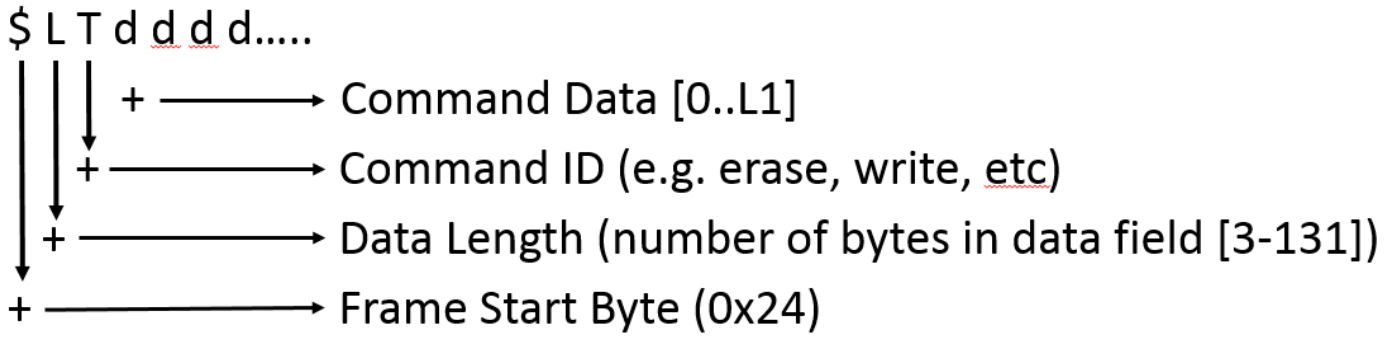
1. Set the BLMDb pin low and the RSTB pin low for greater than 15 µs.
2. Release the RSTb pin followed by the BLMDb pin.

4.3.3 Data Sequence to Write File

The hex file provided from CBPro should be parsed out into separate “records” that will be sent one record at a time from the I2C master to the Si5383/84. This format is similar to that used by the Intel Hex file. The most important thing is to make sure the correct I2C Address is used.

The I2C bootloader commands will be formatted into a binary record format. This simple and consistent format, which is inspired by hex records, is designed to make parsing easy. By including a frame start byte and an explicit length field, a file parser or communication transport code can be written without knowledge of the underlying commands. Also, the format allows command parameters to be added at a future date without impacting backward compatibility.

The following diagram shows the format for the binary boot record.



The communication protocol will work as follows:

1. The I2C host will send one complete record at a time to the Si5383/84 and then will wait for acknowledgment from the Si5383/84.
2. The Si5383/84 will process the record and then produce a one byte response that indicates if the command was successful or failed.

The starting indicator of the record is hex 0x24. This is the record start byte and must be the first byte sent into the IIC Write transaction each time. The next byte indicates how many bytes are to follow.

0x24- Start Indication

Example: 24/07/34/00/00/F4/FF/21/52

0x24: Start Indicator

0x07: Number of Bytes to Follow

34/00/00/F4/FF/21/52: data

4.3.4 ACK Polling or Delay Cycles

The Si5383/84 erase and verify commands can take several milliseconds to complete. The Si5383/84 will be unable to respond while these commands are processing. As a part of the expected protocol, the I2C master should query the Si8384/84 after each write sequence to ensure that the last write sequence was serviced without error. To let the I2C master know that the slave is busy processing the last command the Si5383/84 bootloader has an ACK polling mechanism in place. (This is the same mechanism I2C EEPROM devices use during flash write cycles.) The Si5383/84 bootloader will NAK its slave address while it is processing. The I2C master can poll the Si5383/84 bootloader by attempting to do a master read transfer. If the Si5383/84 slave address is NAK’d the I2C master knows the Si5383/84 bootloader is still busy with the last command. The master should continue to retry the transfer until the Si5383/84 slave address is ACK’d and the read transfer is completed. Then the master can proceed by writing the next boot record.

Otherwise a delay can be used between the write and read cycles. All write cycles typically take 20ms, with the exception of the 3rd last record command which may take up to 6 seconds to complete. This command is the verify sequence, which will check the entire program and compute overall success or failure with a CRC check.

4.3.5 Bootloader Reply Response Codes

The following are responses provided by the Si5383;

1. 0x40: Acknowledged.
2. 0x41: Data Range Error. This error response would indicate that the bootloader sees the targeted address range cannot be written by the bootloader.
3. 0x43: CRC Error if the CRC does not match the expected.

4.4 DSPLL Modes of Operation

4.4.1 Free Run Mode

Once power is applied to the Si5383/84 and initialization is complete, all three DSPLLs will automatically enter freerun mode, generating the frequencies determined by the NVM. The frequency accuracy and stability of the generated output clocks in freerun mode is entirely dependent on the reference clock (REF/REFb), while the external crystal at the XA/XB pins determines the jitter performance of the output clocks. For example, if the reference frequency is ±10 ppm, then all the output clocks will be generated at their configured frequency ±10ppm in freerun mode. Any drift of the reference frequency will be tracked at the output clock frequencies in this mode.

4.4.2 Lock Acquisition Mode

Each of the DSPLLs independently monitors its configured inputs for a valid clock. If at least one valid clock is available for synchronization, a DSPLL will automatically start the lock acquisition process.If the fast lock feature is enabled for inputs $\geq$ 8 kHz, a DSPLL will acquire lock using the Fastlock Loop Bandwidth setting and then transition to the DSPLL Loop Bandwidth setting when lock acquisition is complete. If the input frequency is configured for 1 PPS, the Smartlock mode is used. During lock acquisition the outputs will generate a clock that follows the VCO frequency change as it pulls-in to the input clock frequency.

4.4.3 Locked Mode

Once locked, a DSPLL will generate output clocks that are both frequency and phase locked to their selected input clocks. At this point any XTAL or Ref/Refb frequency drift will not affect the output frequency. Each DSPLL has its own LOL pin and status bit to indicate when lock is achieved.

4.4.4 Holdover Mode

Any of the DSPLLs will automatically enter holdover mode when the selected input clock becomes invalid and no other valid input clocks are available for selection. Each DSPLL calculates a historical average of the input frequency while in locked mode to minimize the initial frequency offset when entering the holdover mode. The averaging circuit for each DSPLL stores several seconds of historical frequency data while locked to a valid clock input. The final averaged holdover frequency value is calculated from a programmable window within the stored historical frequency data. Both the window size and the delay are programmable as shown in the figure below and should be modified to match the application requirements. The window size determines the amount of holdover frequency averaging. The delay value allows ignoring frequency data that may be corrupt just before the input clock failure. Each DSPLL computes its own holdover frequency average to maintain complete holdover independence between DSPLLs.

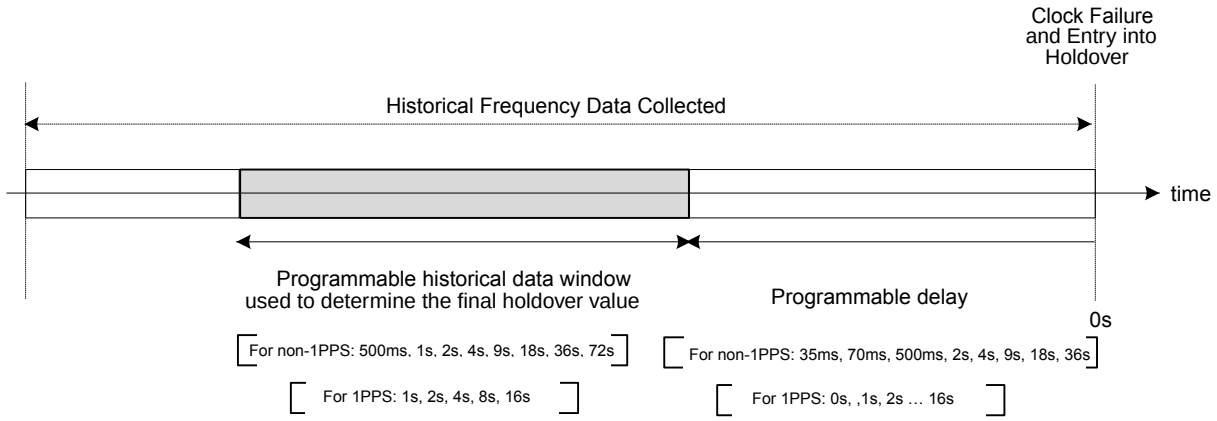


Figure 4.3. Programmable Holdover Window

When entering holdover, a DSPLL will pull its output clock frequency to the calculated averaged holdover frequency. While in holdover, the output frequency drift is entirely dependent on the external reference clock connected to the REF/REFb pins. If the clock input becomes valid, a DSPLL will automatically exit the holdover mode and re-acquire lock to the new input clock. This process involves pulling the output clock frequencies to achieve frequency and phase lock with the input clock. This pull-in process is glitchless. Note that because DSPLL B will always have a TCXO/OCXO as its clock input, under normal operation DSPLLB will never enter holdover. The holdover register bits below are listed for completeness.

The recommended mode of exit from holdover for non 1PPS applications is a ramp in frequency. Just before the exit begins, the frequency difference between the output frequency while in holdover and the desired, new output frequency is measured. It is quite possible (even likely) that the new output clock frequency will not be the same as the holdover output frequency because the new input clock frequency might have changed and the holdover history circuit may have changed the holdover output frequency. The ramp logic calculates the difference in frequency between the holdover frequency and the new, desired output frequency. Using the user selected ramp rate, the correct ramp time is calculated. The output ramp rate is then applied for the correct amount of time so that when the ramp ends, the output frequency will be the desired new frequency. Using the ramp, the transition between the two frequencies is smooth and linear. The ramp rate can be selected to be very slow (0.2 ppm/sec), very fast (40,000 ppm/sec) or any of ~40 values that are in between. The loop BW values do not limit or affect the ramp rate selections (and vice versa). CBPro defaults to ramped exit from holdover. Ramped exit from holdover is also used for ramped input clock switching for non 1PPS applications.

Table 4.5. DSPLL Holdover Control and Status Registers, Standard Input Mode

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
Holdover Status		
HOLD_PLL(D,C,A)	000E[7:4]	Holdover status indicator. Indicates when a DSPLL is in holdover or free-run mode and is not synchronized to the input reference. The DSPLL goes into holdover only when the historical frequency data is valid, otherwise the DSPLL will be in free-run mode.
HOLD_FLG_PLL(D,C,A)	0013[7:4]	Holdover status monitor sticky bits. Sticky bits will remain asserted when an holdover event occurs until cleared. Writing a zero to a sticky bit will clear it.

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
HOLD_HIST_VALID_PLLA[1]	043F[1]	Holdover historical frequency data valid. Indicates if there is enough historical frequency data collected for valid holdover value.
HOLD_HIST_VALID_PLLC[1]	063F[1]	
HOLD_HIST_VALID_PLLD	0740[1]	
Holdover Control and Settings		
HOLD_HIST_LEN_PLLA[1]	042E[4:0]	Window Length time for historical average frequency used in Holdover mode. Window Length in seconds (s): Window Length = $((2^{HOLD_HIST\text{-}LEN_PLLx}) – 1 \times 8/3/(10^7)$Win
HOLD_HIST_LEN_PLLC[1]	062E[4:0]	
HOLD_HIST_LEN_PLLD	072F[4:0]	
HOLD_HIST_DELAY_PLLA[1]	042F[4:0]	Delay Time to ignore data for historical average frequency in Holdover mode. Delay Time in seconds (s): Delay Time = $(2^{HOLD\_HIST\text{-}DELAY\_PLLx}) \times 2/3/(10^7)$
HOLD_HIST_DELAY_PLLC[1]	062F[4:0]	
HOLD_HIST_DELAY_PLLD	0730[4:0]	
FORCE_HOLD_PLLA[1]	0435[0]	These bits allow forcing any of the DSPLLs into holdover
FORCE_HOLD_PLLC[1]	0635[0]	
FORCE_HOLD_PLLD	0736[0]	
HOLD_EXIT_BW_SEL_PLLA[1]	042C[4]	Selects the exit from holdover bandwidth. Options are: 0: Exit of holdover using the fastlock bandwidth 1: Exit of holdover using the DSPLL loop bandwidth
HOLD_EXIT_BW_SEL_PLLC[1]	062C[4]	
HOLD_EXIT_BW_SEL_PLLD	072D[4]	
HOLD_RAMP_EN_PLLA[1]	042C[3]	Must be set to 1 for normal operation.
HOLD_RAMP_EN_PLLC[1]	062C[3]	
HOLD_RAMP_EN_PLLD	072D[3]	

Note:
1. Si5383 only.

Table 4.6. DSPLLD Holdover Control and Status, 1PPS Mode

Setting Name	Hex Address [Bit Field]	Function
HOLD_HIST_VALID	0x5321[0]	Indicates holdover filter acquired adequate data for calculation.
HOLD_FLG	0x5324[7]	Holdover status monitor sticky bit. Bit will will be asserted on entry into holdover and will remain asserted until holdover mode is exited and the bit is cleared. Writing a zero to a sticky bit will clear it.
HOLD	0x5324[3]	Hold status
HO_ACQ_TYPE	0x53E0[5:4]	Determines the acquisition mode when holdover is exited. Must be set before PPS_EN.

Setting Name	Hex Address [Bit Field]	Function
FORCE_HOLD	0x53E0[1]	When asserted, the PPS loop will transition from the FREERUN or LOCKED states to the HOLDOVER state. It will remain in this state until the force is removed.
HO_EXIT_EN	0x53E0[0]	When enabled, HOLDOVER will automatically exit and attempt reacquisition when a valid input is detected. When disabled, FORCE_HOLD will be set on entry into holdover and must be manually cleared to exit the holdover state.
HOLD_HIST_LEN	0x53E1[2:0]	Specifies the holdover window size. Larger windows provide more averaging. Must be set before PPS_EN.
HOLD_HIST_DELAY	0x53E2[4:0]	Specifies the holdover delay time. Delay value allows ignoring corrupt frequency data before the input clock failure. Must be set before PPS_EN.

5. Clock Inputs (IN0, IN1, IN2, IN3, IN4)

There are three inputs that can be used to synchronize any of the DSPLLs. The inputs accept both differential and single-ended clocks. A crosspoint between the inputs and the DSPLLs allows any of the inputs (IN0, IN1, and IN2) to be connected to any of the DSPLLs as shown in the figure below. DSPLL D has two additional iputs (IN3 and IN4) that support LVCMOS input format only. If both IN3 and IN4 are used, they must be the same frequency. Automatic clock selection can be used on any four inputs for PLLD when operating in Standard Input mode, if 5 inputs are required then they must be manually selected.

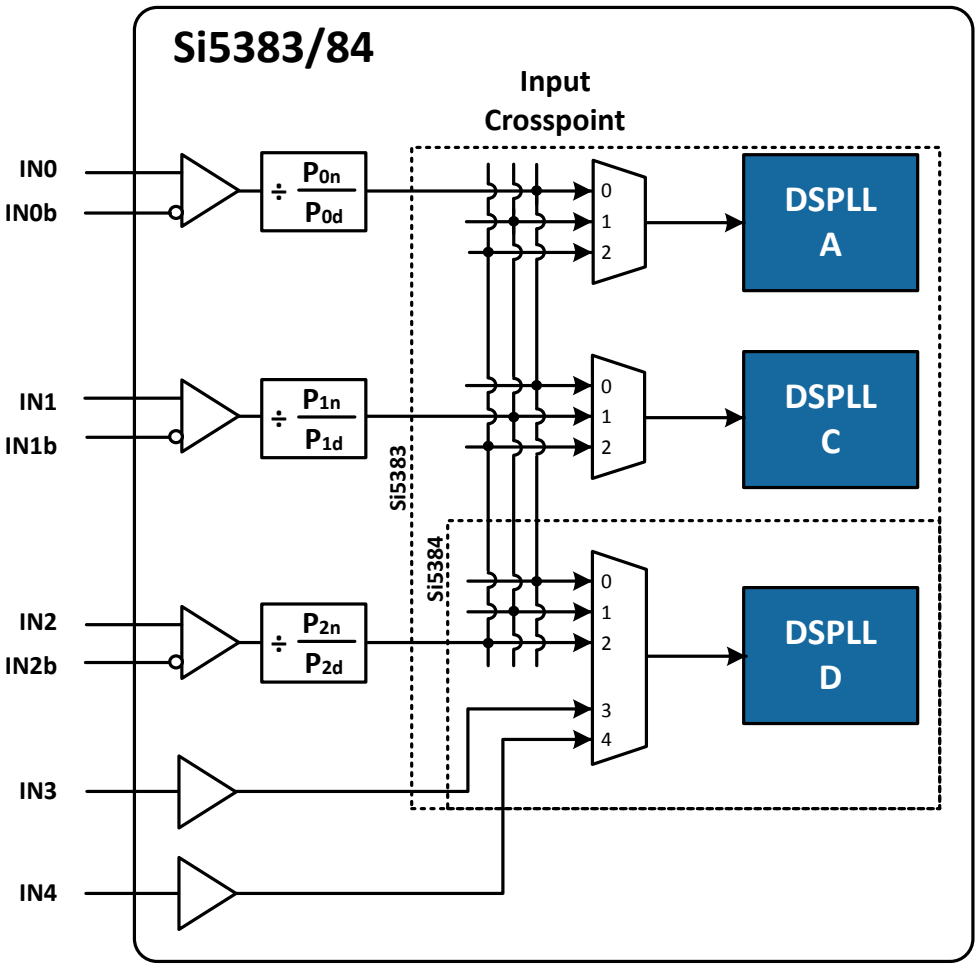


Figure 5.1. DSPLL Input Selection Crosspoint

5.1 Input Source Selection

Input source selection for each of the DSPLLs can be made manually through register control or automatically, when operating in standard input mode, using an internal state machine. 1PPS inputs can only be selected for DSPLL D.

Table 5.1. Manual or Automatic Input Clock Selection Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
CLK_SWITCH_MODE_PLLA[1]	0436[1:0]	Selects manual or automatic switching mode for DSPLL A, C, D. 0: For manual 1: For automatic, non-revertive 2: For automatic, revertive 3: Reserved
CLK_SWITCH_MODE_PLLC[1]	0636[1:0]	
CLK_SWITCH_MODE_PLLD	0737[1:0]	
CONFIGx_CMOS_PLLD	7AA[5:4] and [2:0]	Selects which 4 inputs (max) are used in automatic clock selection

Note:
1. Si5383 only.

In manual mode the input selection is made by writing to a register. If there is no clock signal on the selected input, the DSPLL will automatically enter holdover mode, or free run mode depending on device configuration.

Table 5.2. Manual Input Select Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
IN_SEL_PLLA[1]	042A[1:0]	Selects the clock input used to synchronize DSPLL A, C, or D. Selections are: IN0, IN1, IN2 corresponding to the values 0, 1, and 2. Note that for PLL A and PLL C the selections are IN0-IN2, while for PLL D the selections are IN0-IN4.
IN_SEL_PLLC[1]	062A[1:0]	
IN_SEL_PLLD	072B[2:0]	

Note:
1. Si5383 only.

When configured in automatic mode, the DSPLL automatically selects a valid input that has the highest configured priority. The priority arrangement is independently configurable for each DSPLL and supports revertive or non-revertive selection. All inputs are continuously monitored for loss of signal (LOS) and IN0, IN1 and IN2 are monitored for an invalid frequency range (OOF). By default, inputs asserting either or both LOS or OOF cannot be selected as a source for any DSPLL. However, these restrictions may be removed by writing to the registers described below. If there is no valid input clock, the DSPLL will enter either Holdover or Free Run mode depending on whether the holdover history is valid at that time or not.

Note that PLLA and PLLC have 3 available inputs - IN0, IN1 and IN2 - and all three can be used in automatic selection. PLLD has 5 available inputs - IN0, IN1, IN2, IN3 and IN4 - of which 4 can be selected using automatic input control. If all 5 clock inputs are used in a PLLD application or PPS mode is enabled then manual clock selection must be used

Table 5.3. Automatic Input Select Control Registers

Setting Name	Function
IN(2,1,0)_PRIORITY_PLLA[1]	Selects the automatic selection priority for [IN2, IN1, IN0] for each DSPLL A, C, D. Selections are: 1st, 2nd, 3rd, or never select. Default is IN0=1st, IN1=2nd, IN2=3rd.
IN(2,1,0)_PRIORITY_PLLC[1]	
IN(3,2,1,0)_PRIORITY_PLLD	PLLD allows a 4th input, any combination of 5 inputs.
IN(2,1,0)_LOS_MSK_PLLA[1]	Determines if the LOS status for [IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, C, D. Default is LOS is enabled (un-masked).
IN(2,1,0)_LOS_MSK_PLLC[1]	
IN(3,2,1,0)_LOS_MSK_PLLD	PLLD allows a 4th input, any combination of 5 inputs.
IN(2,1,0)_OOF_MSK_PLLA[1]	Determines if the OOF status for [IN2, IN1, IN0] is used in determining a valid clock for the automatic input selection state machine for DSPLL A, C, D. Default is enabled (un-masked).
IN(2,1,0)_OOF_MSK_PLLC[1]	
IN(3,2,1,0)_OOF_MSK_PLLD	PLLD allows a 4th input, any combination of 5 inputs.
IN_OOF_MSK_PLLB	Default is set to mask the Reference Input.

Note:
1. Si5383 only.

5.2 Types of Inputs

Each of the three different inputs IN0-IN2 are compatible with standard LVDS, LVPECL, HCSL, CML, and single-ended LVCMOS formats, or for a low duty cycle use a pulsed CMOS format. The pulsed CMOS format is also used for 1PPS inputs on IN0-IN2. The standard format inputs have a nominal 50% duty cycle, must be ac-coupled and use the “Standard” Input Buffer selection as these pins are internally dc-biased to approximately 0.83 V. The pulsed CMOS input format allows pulse-based inputs, such as frame-sync, 1PPS and other synchronization signals having a duty cycle much less than 50%. These pulsed CMOS signals are dc-coupled and use the “Pulsed CMOS” Input Buffer selection. In all cases, the inputs should be terminated near the device input pins as shown in the figure below. The resistor divider values given below will work with up to 1 MHz pulsed inputs. In general, following the “Standard AC Coupled Single Ended” arrangement shown below will give superior jitter performance.

IN3 and IN4 are standard 3.3V CMOS inputs, with VIL and VIH input specifications listed in the datasheet, and are DC coupled as shown below. A series resistor is normally placed at the source and value is determined by the output impedance and matching to a 50 ohm trace impedance, eg 27 ohms might be a typical value.

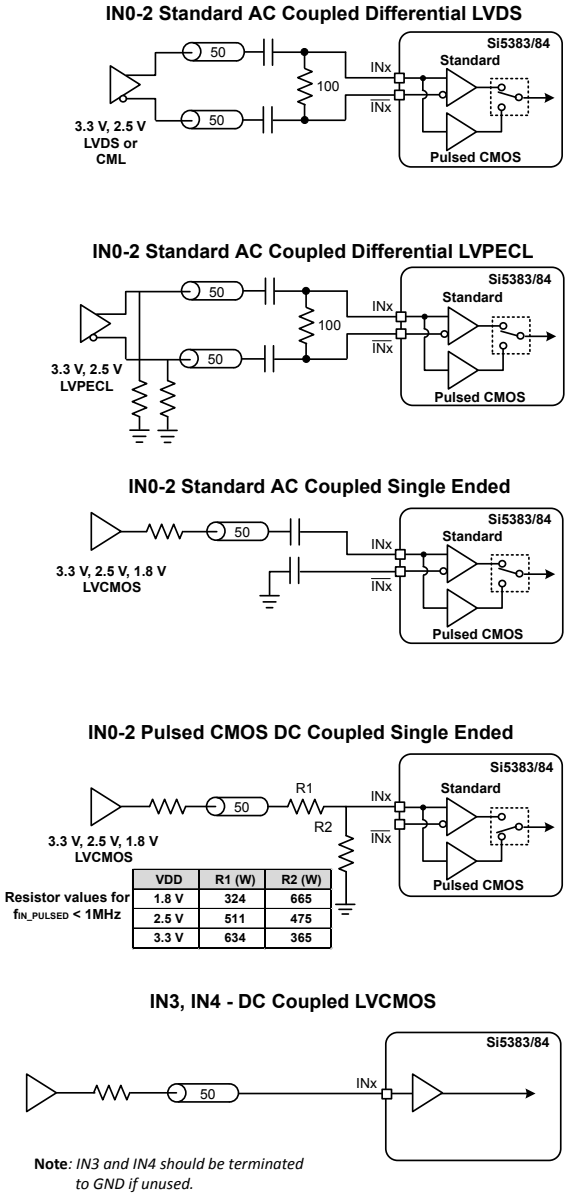


Figure 5.2. Input Termination for Standard and Pulsed CMOS Inputs

Input clock buffers are enabled by setting the IN_EN 0x0949[3:0] bits appropriately for Ref, IN2, IN1 and IN0. Unused clock inputs for IN2, IN1 and IN0 may be powered down and left unconnected at the system level. IN3 and IN4 must be terminated to GND when unused. For standard mode inputs, both input pins must be properly connected as shown in the figure above, including the “Standard AC Coupled Single Ended” case. In Pulsed CMOS mode, it is not necessary to connect the inverting INx input pin. To place the input buffer into Pulsed CMOS mode, the corresponding bit must be set in IN_PULSED_CMOS_EN 0x0949[7:4] for Reference, IN2, IN1 and IN0.

Table 5.4. Input Clock Control and Configuration Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
IN_EN	0x0949[3:0]	Enable each of the input clock buffers for reference (REF) and IN2 through IN0.
IN_PULSED_CMOS_EN	0x0949[7:4]	Enable Pulsed CMOS mode for each input reference (REF) and IN2 through IN0.

Note: For Standard Mode Input Applications:

A LOS or OOF alarm on IN0 can affect DSPLLD only when manually selecting IN3.

A LOS or OOF alarm on IN1 can affect DSPLLD only when manually selecting IN4.

1. If IN3 is selected then set bits 0 and 4 of register 0x0738h. If IN3 is de-selected then return bits 0 and 4 of register 0x0738h to the IN0 settings. Under these conditions DSPLLD will lock and track as expected.If IN4 is selected then set bits 1 and 5 of register 0x0738h.
2. If IN4 is de-selected then return bits 1 and 5 of register 0x0738h to the IN1 settings. Under these conditions DSPLLD will lock and track as expected.
3. Holdover should be forced, by setting register 0x0736[0] = 1, if IN3 or IN4 is selected and the associated IN3 or IN4 becomes invalid and the clock input will not be switched.
4. Forced holdover should be relinquished by setting 0x0736[0] = 1 when switching to a valid input clock.

The above does not apply to 1PPS input applications.

5.2.1 Hitless Input Switching

Hitless switching is a feature that prevents a phase change from propagating to the output when switching between two clock inputs that have exactly the same frequency and a fixed phase relationship. In practice, this means that either one of the clocks must be frequency-locked to the other or that both must be frequency-locked to the same source. When hitless switching is enabled, the DSPLL absorbs the phase difference between the two input clocks during a input switch by enabling phase buildout. When disabled, the phase difference between the two inputs is propagated to the output at a rate determined by the DSPLL Loop Bandwidth. The hitless switching feature supports clock frequencies down to the minimum input frequency of 8 kHz. Hitless switching can be enabled on a per DSPLL basis. If a fractional P divider is used on an input, the input frequency must be 5 MHz or higher in order to ensure proper hitless switching.

Table 5.5. DSPLL Hitless Switching Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
HSW_EN_PLLA[1]	0436[2]	Hitless Switching Enable/Disable for DSPLL A, C, D. Hitless switching is enabled by default.
HSW_EN_PLLC[1]	0636[2]	
HSW_EN_PLLD	0737[2]	
RAMP_SWITCH_EN_PLLA[1]	0x04A6[3]	Enable frenquency ramping on an input switch.
RAMP_SWITCH_EN_PLLC[1]	0x06A6[3]	
RAMP_SWITCH_EN_PLLD	0x07A6[3]	
HSW_MODE_PLLA[1]	0x043A[1:0]	Hitless switching mode select.
HSW_MODE_PLLC[1]	0x063A[1:0]	
HSW_MODE_PLLD	0x073A[1:0]	

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	

Note:
1. Si5383 only.

5.2.2 Glitchless Input Switching

The DSPLLs have the ability to switch between two input clock frequencies that are up to ±500 ppm apart for input frequencies ≥ 8kHz, and +/-10ppm for 1PPS inputs.

When operating in standard mode (non 1PPS) and switching between input clocks that are not exactly the same frequency (i.e. are plesiochronous), ramped switching should be enabled to ensure a smooth transition between the two input frequencies. In this situation, it is also advisable to enable phase buildout to minimize the input-to-output clock skew after the clock switch ramp has completed.

When ramped clock switching is enabled, the Si5383 will very briefly go into holdover and then immediately exit from holdover. This means that ramped switching will behave the same as an exit from holdover. This is particularly important when switching between two input clocks that are not the same frequency because the transition between the two frequencies will be smooth and linear. Ramped switching should be turned off when switching between input clocks that are always frequency locked (i.e. are the same exact frequency). Because ramped switching avoids frequency transients and over shoot when switching between clocks that are not the same frequency, CBPro defaults to ramped clock switching. The same ramp rate settings are used for both exit from holdover and clock switching. For more information on ramped exit from holdover including the ramp rate, see Section 4.4.4 Holdover Mode.

Note: The Si5383/84 should be set to "Holdover" before switching inputs operating in 1PPS mode.

5.2.3 Synchronizing to Gapped Input Clocks

When operating in standard input mode the DSPLL supports locking to a gapped input clock with missing clock edges for input frequencies > 10 MHz. The purpose of gapped clocking is to modulate the frequency of a periodic clock by selectively removing some of its edges. Gapping a clock significantly increases its jitter so a phase-locked loop with high jitter tolerance and low loop bandwidth is required to produce a low-jitter, periodic clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. For example, an input clock of 100 MHz with one cycle removed every 10 cycles will result in a 90 MHz periodic non-gapped output clock. A valid gapped clock input must have a minimum frequency of 10 MHz with a maximum of 2 missing cycles out of every 8.

When properly configured, locking to a gapped clock will not trigger the LOS, OOF, and LOL fault monitors. Clock switching between gapped clocks may violate the hitless switching specification of up to 1.5 ns for a maximum phase transient, when the switch occurs during a gap in either input clocks. The figure below shows a 100 MHz clock with one cycle removed every 10 cycles that results in a 90 MHz periodic non-gapped output clock.

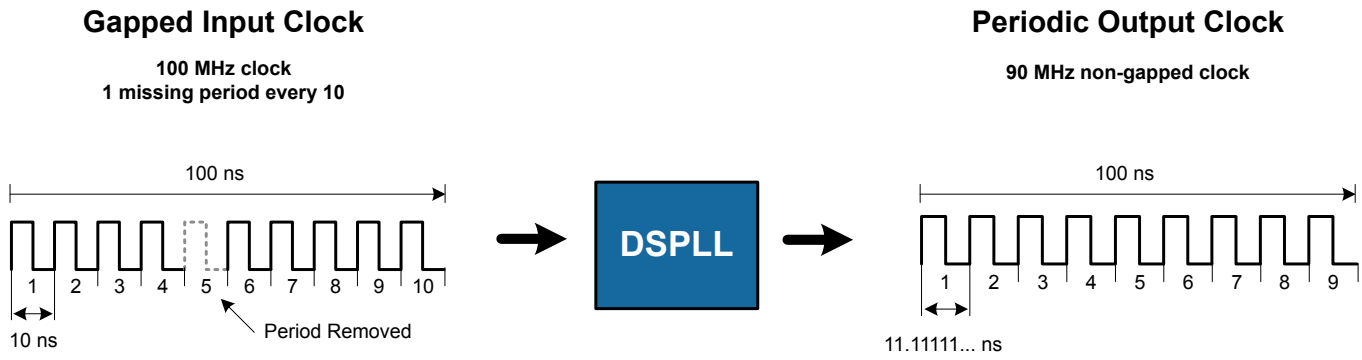


Figure 5.3. Gapped Input Clock Use

5.3 Fault Monitoring

Input clocks (IN0, IN1, IN2) and the reference input REF/REFb are monitored for loss of signal (LOS) and out-of-frequency (OOF) as shown in the figure below. The reference at the XA/XB pins is also monitored for LOS since it provides a critical reference clock for the DSPLLs. Each of the DSPLLs also has a Loss Of Lock (LOL) indicator which is asserted when synchronization is lost with their selected input clock. Note that IN3 and IN4 are monitored for LOS only.

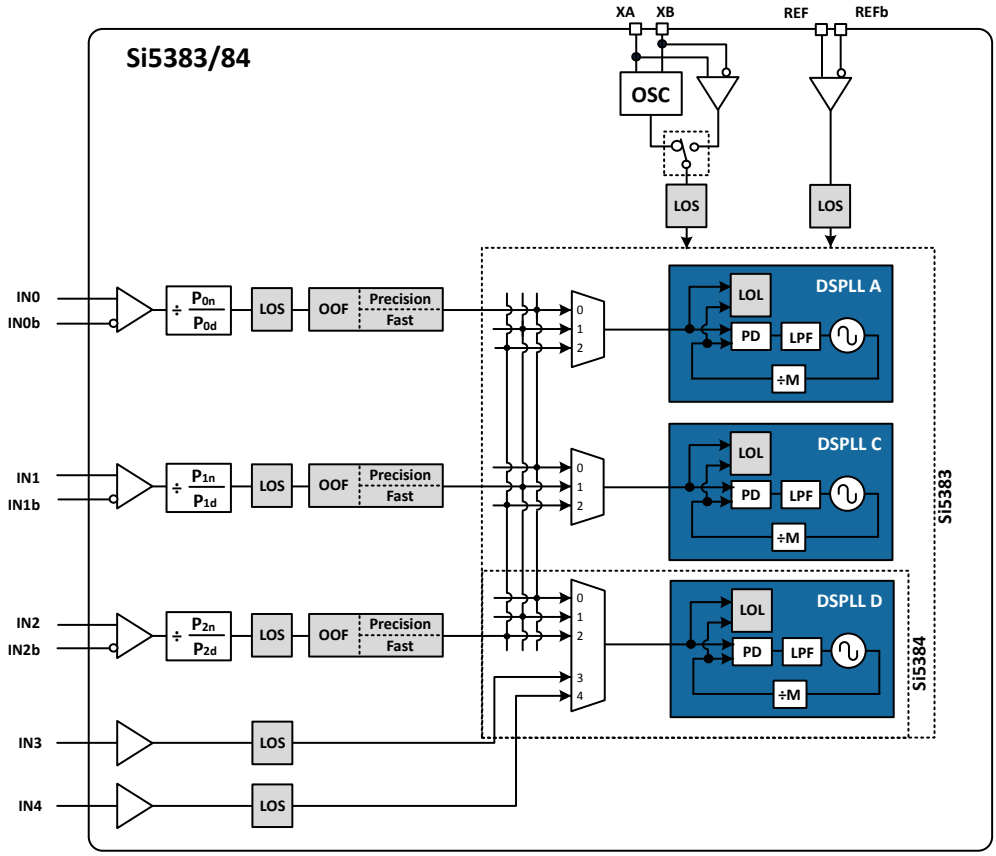


Figure 5.4. Fault Monitors

5.3.1 Input LOS Detection

The loss of signal monitor measures the period of each input clock cycle to detect phase irregularities or missing clock edges. Each of the input LOS circuits has its own programmable sensitivity which allows ignoring missing edges or intermittent errors. Loss of signal sensitivity is configurable using the ClockBuilder Pro utility. The LOS status for each of the monitors is accessible by reading a status register. The live LOS register always displays the current LOS state and a sticky register, when set, always stays asserted until cleared.

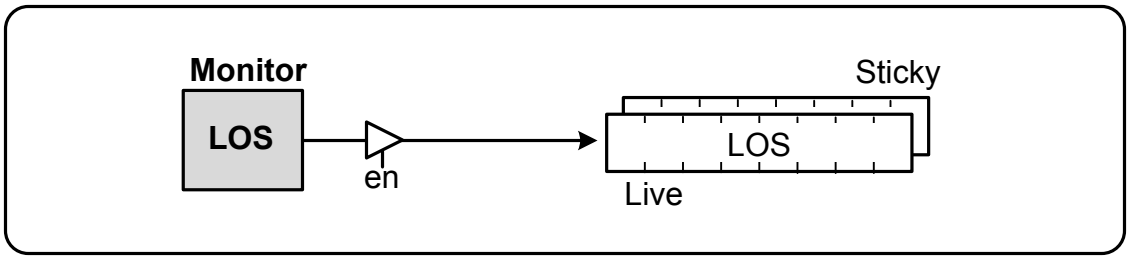


Figure 5.5. LOS Status Indicator

5.3.2 XA/XB LOS Detection

A LOS monitor is available to ensure that the external crystal or reference clock is valiid. By default the output clocks are disabled when XAXB_LOS is detected. This feature can be disabled such that the device will continue to produce output clocks when XAXB_LOS is detected.

Table 5.6. LOS Status Monitor Registers

Setting Name	Hex Address [Bit Field]	Function
LOS (Ref, 2,1,0)	000D[3:0]	LOS Status monitor for Reference (Ref), IN2, In1, IN0. Indicates if a valid clock is detected or if a LOS condition is present
LOS_CMOS (1,0)	000C[7:6]	LOS Status monitor for IN3 and IN4. Indicates if a valid clock is detected or if a LOS condition is present
LOSXAXB	000C[1]	LOS status monitor for the XTAL at the XAXB pins.
LOS (Ref, 2,1,0)_FLG	0012[3:0]	LOS Status monitor sticky bits for Reference (Ref), IN2, IN1, IN0. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS_CMOS_FLG (1,0)	0011[7:6]	LOS Status monitor sticky bits for IN3 and IN4. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOSXAXB_FLG	0011[1]	LOS Status monitor sticky bits for XAXB. Sticky bitss will remain asserted when an LOS event occurs until cleared. Writing a zero to a sticky bit will clear it.
LOS Fault Monitor Controls and Settings		
LOS (Ref,2,1,0)_EN	002C[3:0]	LOS monitor enable for Reference (Ref), IN2, IN1, IN0. Allows disabling the monitor if unused
LOS_CMOS_EN (4,3)	02BC[2:1]	LOS monitor enable for In3 and IN4. Allows disabling the monitor if unused
LOS(Ref,2,1,0)_TRG_THR	002E[7:0]-0035[7:0]	LOS monitor enable for Reference (Ref), IN2, IN1, IN0. Allows disabling the monitor if unused
LOS_CMOS(1,0)_TRG_THR	02BE[7:0]-02C0[7:0]	LOS monitor enable for Reference IN3 and IN2. Allows disabling the monitor if unused
LOS(Ref,2,1,0)_CLR_THR	0036[7:0]-003D[7:0]	Sets the LOS trigger threshold and clear sensitivity fr the Reference, IN4,IN3, IN2, IN1 and IN0. These 16 bit values are determined in ClockBuilder Pro.
LOS_CMOS(1,0)_CLR_THR	02C2[7:0]-02C4[7:0]	
LOS_CMOS_VAL_TIME	02BD[3:0]	LOS clear validation time for IN3 and IN3. This sets the time that an input must have a valid clock before the LOS conditions are cleared. Setting 2 ms, 100 ms, 300 ms and 2 s are available.

Table 5.7. LOS Status Monitor Registers, 1PPS Mode

Setting Name	Hex Address [Bit Field]	Function
LOS_EN_1HZ	0x003E[1:0]	Enables 1Hz LOS monitor
LOS_CMOS_EN_1HZ	0x02BC[5:4]	Enables 1Hz LVCMOS LOS monitor
LOS_EN	0x5330[3]	Enables the Si5383 LOS detector
LOS_EXT_EN	0x5330[1]	Enables an external device to control the LOS status via the I2C I/F.
LOS_EXT	0x5330[0]	External LOS control.
LOS_PPS_FLG	0x5323[4]	Sticky indication that LOS occurred.
LOS_PPS	0x5323[0]	Indicates LOS status of the selected PPS signal.

5.3.3 OOF Detection

In standard input mode, input clocks IN0, IN1and IN2 are monitored for frequency accuracy with respect to a OOF reference which it considers as its "0 ppm" reference. The final OOF status is determined by the combination of both a precise OOF monitor and a fast OOF monitor as shown in the figure below. An option to disable either monitor is also available. The live OOF register always displays the current OOF state and its sticky register bit stays asserted until cleared.

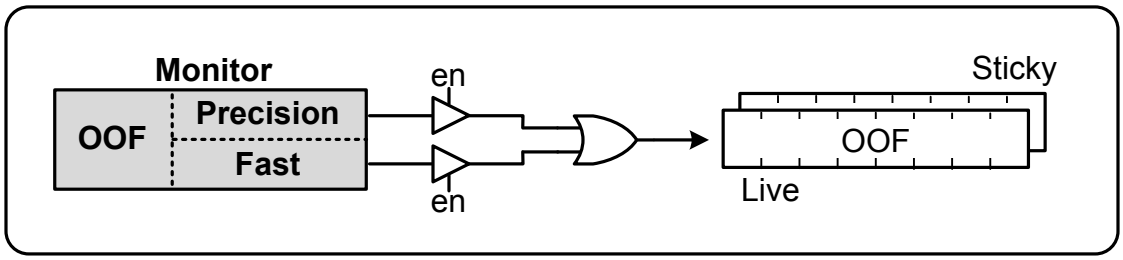


Figure 5.6. OOF Status Indicator

5.3.4 LOL Detection (Standard Input Mode)

There is a loss of lock (LOL) monitor for each of the DSPLLs. The LOL monitor asserts a LOL register bit when a DSPLL has lost synchronization with its selected input clock. There is also a dedicated loss of lock pin that reflects the loss of lock condition for each of the DSPLLs (LOL_Ab, LOL_Cb, LOL_Db) and the Reference (LOL_Bb). There are two LOL frequency monitors, one that sets the LOL indicator (LOL Set) and another that clears the indicator (LOL Clear). An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. A block diagram of the LOL monitor is shown in the following figure. The live LOL register always displays the current LOL state and a sticky register always stays asserted until cleared. The LOL pin reflects the current state of the LOL monitor.

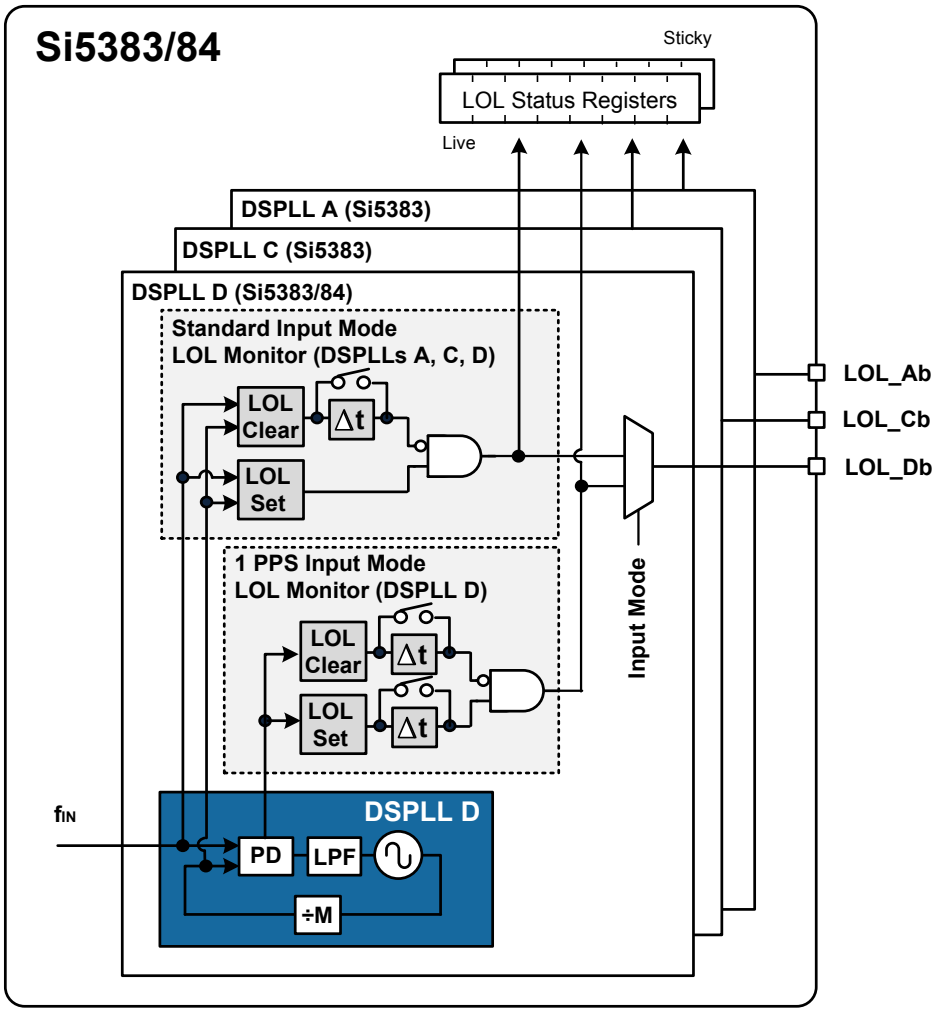


Figure 5.7. LOL Status Indicators

Each of the LOL frequency monitors has an adjustable set sensitivity which is register configurable from 1 ppm to 10000 ppm and a clear threshold from 0.1 to 1000 ppm. Having two separate frequency monitors allows for hysteresis to help prevent chattering of LOL status. An example configuration where LOCK is indicated when there is less than 1 ppm frequency difference at the inputs of the phase detector and LOL is indicated when there's more than 10 ppm frequency difference is shown in the figure below.

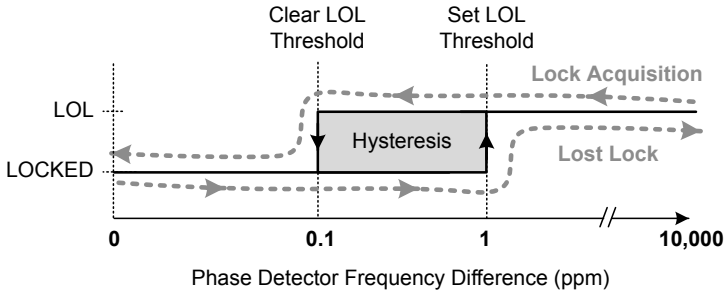


Figure 5.8. LOL Set and Clear Thresholds

An optional timer is available to delay clearing of the LOL indicator to allow additional time for the DSPLL to completely lock to the input clock. The timer is also useful to prevent the LOL indicator from toggling or chattering as the DSPLL completes lock acquisition. The configurable delay value depends on frequency configuration and loop bandwidth of the DSPLL and is automatically calculated using the ClockBuilder Pro utility.

It is important to know that, in addition to being status bits, LOL enables Fastlock.

Table 5.8. LOL Status Monitor Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
LOL Status Indicators		
LOL_PLL(D,C,B,A)	000E[3:0]	Status bit that indicates if DSPLL A, B (Reference), C, or D is locked to an input clock.
LOL_FLG_PLL(D,C,B,A)	0013[3:0]	Sticky bits for LOL_[D,C,B,A]_STATUS register. Writing a zero to a sticky bit will clear it.
LOL Fault Monitor Controls and Settings		
LOL_SET_THR_PLL(D,C,B,A)	009E[7:0] - 009F[7:0]	Configures the loss of lock set thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 0.2 ppm.
LOL_CLR_THR_PLL(D,C,B,A)	00A0[7:0] - 00A1[7:0]	Configures the loss of lock clear thresholds for DSPLL A, B, C, D. Selectable as 0.2, 0.6, 2, 6, 20, 60, 200, 600, 2000, 6000, 20000. Values in ppm. Default value is 2 ppm.
LOL_CLR_DELAY_PLL(D,C,B,A)	00A3[7:0] - 00B6[7:0]	This is a 35-bit register that configures the delay value for the LOL Clear delay. Selectable from 4 ns over 500 seconds. This value depends on the DSPLL frequency configuration and loop bandwidth. It is calculated using ClockBuilder Pro utility.
LOL_TIMER_EN_PLL(D,C,B,A)	00A2[3:0]	Allows bypassing the LOL Clear timer for DSPLL A, B, C, D. 0- bypassed, 1-enabled

The settings in the table above are handled by ClockBuilder Pro. Manual settings should be avoided.

5.3.5 LOL Detection in PPS Mode

DSPLLD implements a phase-based LOL detector when operating in PPS mode. The current status is reflected in a register bit (LOL) and on a dedicated status pin (LOL_Db). In addition, the host interface includes a sticky bit (LOL_FLG) which is set on LOL assertion and is cleared by writing a 0 when the underlying condition is negated. Two independent phase error thresholds are included: one for LOL trigger (LOL_TRG_THR) and one for LOL clear (LOL_CLR_THR). Having two separate phase error thresholds allows for hysteresis to help prevent chattering of the LOL status. An additional level of filtering is provided with trigger (LOL_TRG_CNT) and clear (LOL_CLR_CNT) counters. These counters represent the number of consecutive clock cycles a threshold must be met before the LOL alarm changes state. These counters prove useful when dealing with transient events, fault conditions, and locking to inputs with noise. For example, the DSPLL may see a large phase error between the time the input signal is lost and the LOS alarm is raised. The user must ensure LOF does not occur during this time to guarantee entry into holdover. This is accomplished by adjusting the LOL_TRG_CNT to a larger value to compensate for this interval.

Table 5.9. LOL Fault Monitor Controls and Settings, 1PPS Mode

Setting Name	Hex Address [Bit Field]	Function
LOL_ACQ_TYPE	0x5340[5:4]	Determines the acquisition mode when LOL occurs. Must be set before PPS_EN.
LOL_TRG_CNT	0x5342[7:0]-0x5343[7:0]	The number of consecutive polls the trigger threshold is exceeded before the LOL alarm is raised. Must be set before PPS_EN.
LOL_CLR_CNT	0x5344[7:0]-0x5345[7:0]	The number of consecutive polls the clear threshold is exceeded before the LOL alarm is raised. Must be set before PPS_EN.
LOL_TRG_THR	0x5348[7:0]-0x534B[7:0]	Phase error threshold that causes LOL to be asserted (after soaking). Must be set before PPS_EN
LOL_CLR_THR	0x534C[7:0]-0x534F[7:0]	Phase error threshold that causes LOL to be negated (after soaking). Must be set before PPS_EN.

5.3.6 LOT Detection in PPS Mode

DSPLLD includes a loss of tracking (LOT) alarm when operating in the 1PPS mode. The current status is reflected in a register bit (LOT) as well as a sticky bit (LOT_FLG). LOT_FLG is set on LOT assertion and is cleared by writing a 0 when the underlying condition is negated.

LOT is an indication that DSPLLD has lost the ability to track the input under closed loop operation. Exceeding the dynamic range of the PD, loop filter, or the DCO will set the LOT alarm. This is not expected to occur under normal operation, but could happen if there are out-of-spec input transients. When LOT occurs, DSPLLD will require the input signal using SmartLock acquisition.

Table 5.10. Loss of Tracking Registers, 1PPS Mode

Setting Name	Hex Address [Bit Field]	Function
LOT	0x5304[0]	Loss of Tracking
LOL_FLG	0x5304[4]	Sticky version of LOT
LOT_HO_CNT	0x5309[7:0]	The number of polls after LOT is asserted before reaquisition occurs

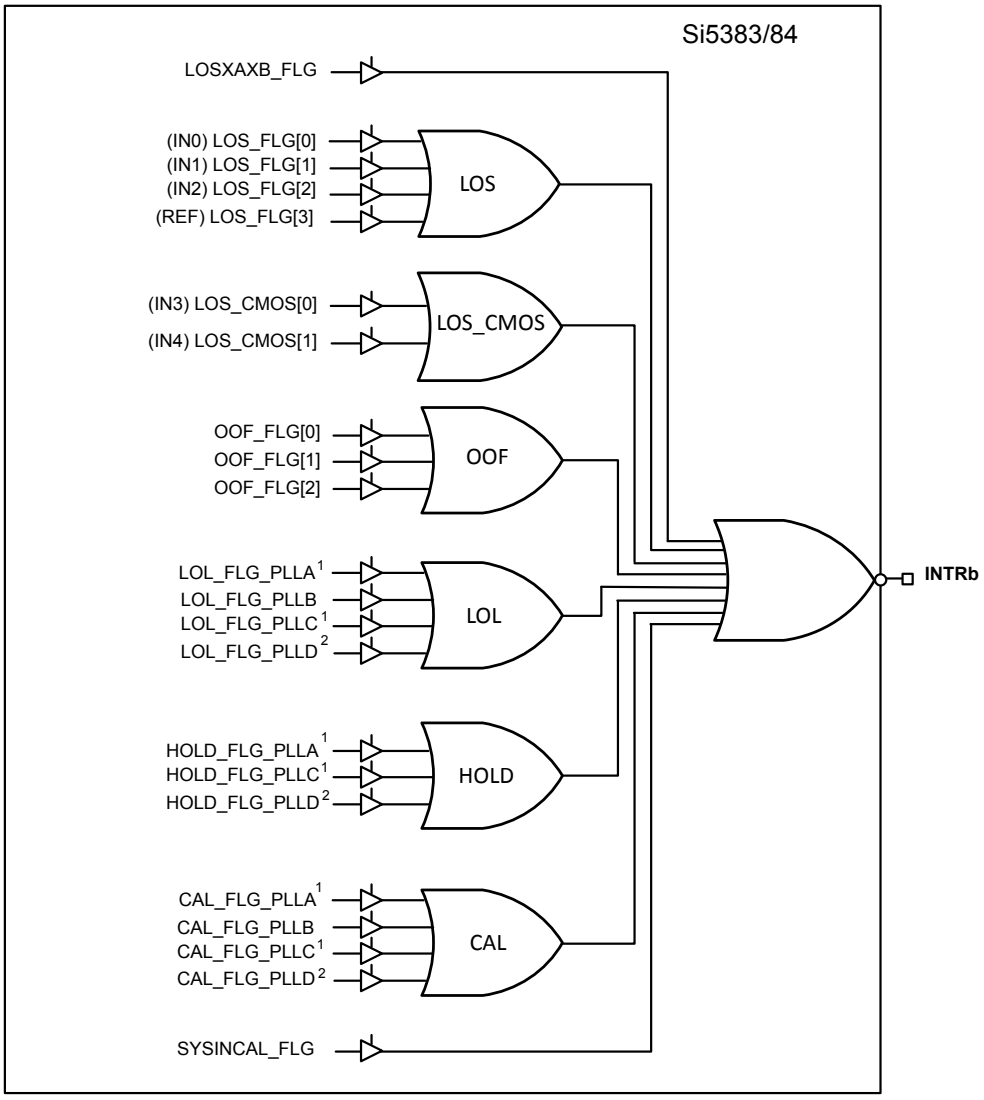
5.3.7 Interrupt Pin (INTRb)

An interrupt pin (INTRb) indicates a change in state with any of the status indicators for any of the DSPLLs. All status indicators are maskable to prevent assertion of the interrupt pin. The state of the INTRb pin is reset by clearing the sticky status registers.

Table 5.11. Interrupt Mask Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
LOS_INTR_MSK	0018[3:0]	Prevents Reference (REF), IN2, IN1, IN0 LOS from asserting the INTRb pin
OOF_INTR_MSK	0018[7:4]	Prevents REF, IN2, IN1, IN0 OOF from asserting the INTRb pin
LOSXAXB_INTR_MSK	0017[1]	Prevents XAXB LOS from asserting the INTRb pin
LOL_INTR_MSK_PLL(D,B,C,A)	0019[3:0]	Prevents DSPLL D, B,C, A LOL from asserting the INTRb pin
HOLD_INTR_MSK_PLL(D,C,A)	0019[7:4]	Prevents DSPLL D, C, A HOLD from asserting the INTRb pin

Note:
1. DSPLL A and C do not apply to the Si5384.



Notes:
1. Si5383 only
2. Standard input mode only

Figure 5.9. Interrupt Triggers and Masks

The _FLG bits are "sticky" versions of the alarm bits and will stay high until cleared. A _FLG bit can be cleared by writing a zero to the _FLG bit. When a _FLG bit is high and its corresponding alarm bit is low, the _FLG bit can be cleared.

During run time, the source of an interrupt can be determined by reading the _FLG register values and logically ANDing them with the corresponding _MSK register bits (after inverting the _MSK bit values). If the result is a logic one, then the _FLG bit will cause an interrupt.

For example, if LOS_FLG[0] is high and LOS_INTR_MSK[0] is low, then the INTRb pin will be active (low) and cause an interrupt. If LOS[0] is zero and LOS_MSK[0] is one, writing a zero to LOS_MSK[0] will clear the interrupt (assuming that there are no other interrupt sources). If LOS[0] is high, then LOS_FLG[0] and the interrupt cannnot be cleared.

6. Output Clocks

6.1 Outputs

The Si5383/84 supports seven differential output drivers. Each driver has a configurable voltage amplitude and common mode voltage covering a wide variety of differential signal formats including LVPECL, LVDS, HCSL, with CML-compatible amplitudes. In addition to supporting differential signals, any of the outputs can be configured as dual single-ended LVCMOS (3.3 V, 2.5 V, or 1.8 V) providing up to 14 single-ended outputs, or any combination of differential and single-ended outputs.

6.1.1 Output Crosspoint

A crosspoint allows any of the output drivers to connect with any of the DSPLLs as shown in the figure below. The crosspoint configuration is programmable and can be stored in NVM so that the desired output configuration is ready at power up.

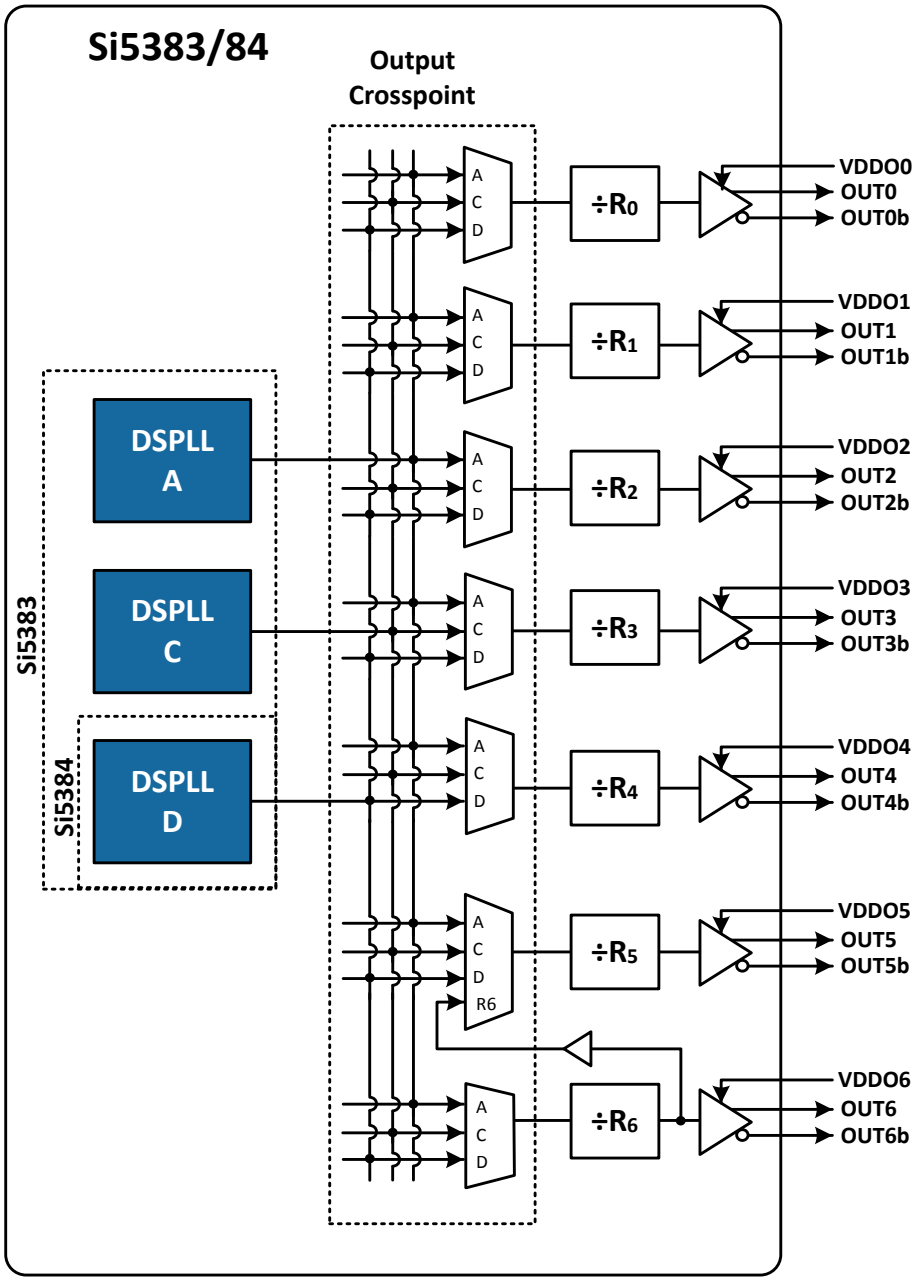
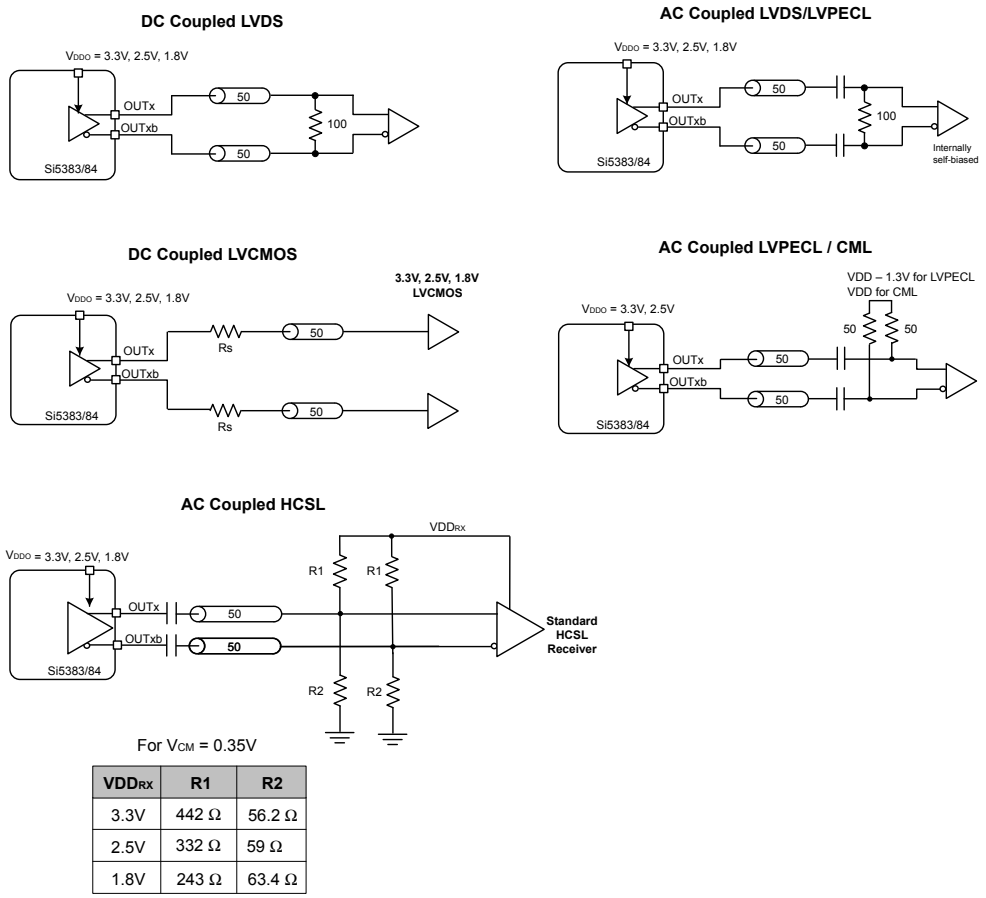


Figure 6.1. DSPLL to Output Driver Crosspoint

6.1.2 Output Terminations

The differential output drivers support both ac coupled and dc coupled terminations as shown in the figure below.



For V_{CM} = 0.35V

VDD_{RX}	R1	R2
3.3V	442 Ω	56.2 Ω
2.5V	332 Ω	59 Ω
1.8V	243 Ω	63.4 Ω

Figure 6.2. Output Terminations for Differential and LVCMOS Outputs

Note: Unused CMOS outputs can include a 50-Ω series resistor and AC coupling capacitor to GND to optimize phase noise on the other outputs.

6.1.3 Output Divider (R) Synchronization

All the output R dividers are reset to a known state during the power-up initialization period. This ensures consistent and repeatable phase alignment. Resetting the device using the RSTb pin or asserting the hard reset bit 0x5303[0] will give the same result. Soft reset does not affect output alignment.

6.1.4 Support for 1 Hz Output (1PPS)

Output 5 of the Si5383/84 can be configured to generate a 1PPS clock. This is done by cascading the R5 and R6 dividers, done internal to the Si5383/84 as shown in the figure below, and easily set when using CBPro. Output 6 is still usable in this case but is limited to a frequency of 33.5 MHz or less. ClockBuilder Pro automatically determines the optimum configuration when generating a 1 Hz output. Power must be applied to VDDO6 for a 1PPS/VDDO5 output.

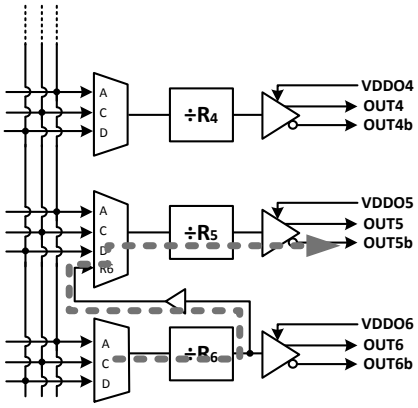


Figure 6.3. Generating a 1 Hz Output using the Si5383/84

6.2 Performance Guidelines for Outputs

Whenever a number of high frequency, fast rise time, large amplitude signals are all close to one another, the laws of physics dictate that there will be some amount of crosstalk. The jitter generation of the Si5383/84 is so low that crosstalk can become a significant portion of the final measured output jitter. Some of the crosstalk will come from the Si5383/84, and some will be introduced by the PCB. It is difficult (and possibly irrelevant) to allocate the jitter portions between these two sources since the Si5383/84 must be attached to a board in order to measure jitter.

For extra fine tuning and optimization in addition to following the usual PCB layout guidelines, crosstalk can be minimized by modifying the arrangements of different output clocks. For example, consider the following lineup of output clocks in the table that follows.

Table 6.1. Example of Output Clock Placement

Output	Not Recommended (Frequency MHz)	Recommended (Frequency MHz)
0	155.52	155.52
1	156.25	155.52
2	155.52	622.08
3	156.25	Not used
4	622.08	156.25
5	625	156.25
6	Not used	625

Using this example, a few guidelines are illustrated:

1. Avoid adjacent frequency values that are close. For example, a 155.52 MHz clock should not be placed next to a 156.25 MHz clock. If the jitter integration bandwidth goes up to 20 MHz then keep adjacent frequencies at least 20 MHz apart.
2. Adjacent frequency values that are integer multiples of one another are allowed, and these outputs should be grouped together when possible. Noting that because 155.52 MHz x 4 = 622.08 MHz and 156.25 MHz x 4 = 625 MHz, it is okay to place each pair of these frequency values close to one another.
3. Unused outputs can be used to separate clock inputs that might otherwise interfere with one another. In this case, see OUT3.

If some outputs have tight jitter requirements while others are relatively loose, rearrange the clock outputs so that the critical outputs are the least susceptible to crosstalk. These guidelines need to be followed by those applications that wish to achieve the highest possible levels of jitter performance. Because CMOS outputs have large pk-pk swings, are single ended, and do not present a balanced load to the VDDO supplies, CMOS outputs generate much more crosstalk than differential outputs. For this reason, CMOS outputs should be avoided in jitter-sensitive applications. When CMOS clocks are unavoidable, even greater care must be taken with respect to the above guidelines.For more information on these issues, see AN862: "Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems."

The ClockBuilder Pro "Clock Placement Wizard" is an easy way to reduce crosstalk for a given frequency plan. The "Clock Placement Wizard" feature can be accessed on the "Define Output Frequencies" page of ClockBuilder Pro in the lower left hand corner of the GUI. It is recommended to use this tool after each project frequency plan change.

6.2.1 Output Crosspoint and Differential Signal Format Selection

The differential output swing and common mode voltage are both fully programmable and compatible with a wide variety of signal formats, including LVDS, LVPECL, HCSL, and CML. The differential formats can be either normal- or low-power mode. Low-power format uses less power for the same amplitude but has the drawback of slower rise/fall times. See Section 15. Custom Differential Amplitude Controls for register settings to implement variable amplitude differential outputs. In addition to supporting differential signals, any of the outputs can be configured as LVCMOS (3.3, 2.5, or 1.8 V) drivers providing up to 20 single-ended outputs or any combination of differential and single-ended outputs. Note also that CMOS can create much more crosstalk than differential outputs, so extra care must be taken in their pin placement so that other clocks that need the lowest jitter are not on nearby pins. With all outputs, see “AN862: Optimizing Si534x Jitter Performance in Next Generation Internet Infrastructure Systems” for additional information on frequency planning considerations.

Table 6.2. Output Crosspoint Selection Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_MUX_SEL	0115[2:0]	Selects the DSPLL that each of the outputs are connected to. Options are DSPLL_A, DSPLL_C, or DSPLL_D. Only DSPLL_D is allowed for the Si5384.
OUT1_MUX_SEL	011A[2:0]	
OUT2_MUX_SEL	011F[2:0]	
OUT3_MUX_SEL	0129[2:0]	
OUT4_MUX_SEL	012E[2:0]	
OUT5_MUX_SEL	0133[2:0]	
OUT6_MUX_SEL	013D[2:0]	

Table 6.3. Output Signal Format Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_FORMAT	0113[2:0]	Selects the output signal format as differential or LVCMOS.
OUT1_FORMAT	0118[2:0]	
OUT2_FORMAT	011D[2:0]	
OUT3_FORMAT	0127[2:0]	
OUT4_FORMAT	012C[2:0]	
OUT5_FORMAT	0131[2:0]	
OUT6_FORMAT	013B[2:0]	

6.3 Differential Outputs

6.3.1 Differential Output Amplitude Controls

The differential amplitude of each output can be controlled with the following registers. See Chapter 15. Custom Differential Amplitude Controls for register settings for non-standard amplitudes.

Table 6.4. Differential Output Voltage Amplitude (Swing) Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_AMPL	0114[6:4]	Sets the differential voltage swing (amplitude) for the output drivers in both normal and low-power modes. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 48 recommended settings. .
OUT1_AMPL	0119[6:4]	
OUT2_AMPL	011E[6:4]	
OUT3_AMPL	0128[6:4]	
OUT4_AMPL	012D[6:4]	
OUT5_AMPL	0132[6:4]	
OUT6_AMPL	013C[6:4]	

6.3.2 Differential Output Common Mode Voltage Selection

The common mode voltage (VCM) for differential output normal and low-power modes is selectable depending on the supply voltage provided at the output's VDDO pin. See Chapter 15. Custom Differential Amplitude Controls for recommended OUTx_CM settings when using custom output amplitude.

Table 6.5. Differential Output Common Mode Voltage Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_CM	0114[3:0]	Sets the common mode voltage for the differential output driver. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 48 recommended settings.
OUT1_CM	0119[3:0]	
OUT2_CM	011E[3:0]	
OUT3_CM	0128[3:0]	
OUT4_CM	012D[3:0]	
OUT5_CM	0132[3:0]	
OUT6_CM	013C[3:0]	

6.3.3 Recommended Settings for Differential LVPECL, LVDS, HCSL, and CML

Each differential output has four settings for control:

1. Normal or Low Power Format
2. Amplitude (sometimes called Swing)
3. Common Mode Voltage
4. Stop High or Stop Low

The Normal mode setting includes an internal 100 Ω resistor between the OUT/OUTb pins. In Low Power mode, this resistor is removed, resulting in a higher output impedance. The increased impedance creates larger amplitudes for the same power while reducing edge rates that may increase jitter or phase noise. In either mode, the differential receiver must be properly terminated to the PCB trace impedance for good system signal integrity. Note that ClockBuilder Pro does not provide low-power mode settings. Contact Skyworks Technical Support for assistance with low-power mode use.

Amplitude controls are as described in the previous section and also in more detail in Chapter 15. Custom Differential Amplitude Controls. Common mode voltage selection is also described in more detail in Chapter 15. Custom Differential Amplitude Controls. The Stop High or Stop Low choice is described above.

Table 6.6. Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML

Standard	VDDOx (V)	Mode	OUTx_FORMAT (dec)	OUTx_CM (dec)	OUTx_AMPL (dec)
LVPECL	3.3	Normal	1	11	6
LVPECL	2.5	Normal	1	11	6
LVPECL	3.3	Low-Power	2	11	3
LVPECL	2.5	Low-Power	2	11	3
LVDS	3.3	Normal	1	3	3
LVDS	2.5	Normal	1	11	3
Sub-LVDS [1]	1.8	Normal	1	13	3
LVDS	3.3	Low-Power	2	3	1
LVDS	2.5	Low-Power	2	11	1
Sub-LVDS [1]	1.8	Low-Power	2	13	1
HCSL[2]	3.3	Low-Power	2	11	3
HCSL[2]	2.5	Low-Power	2	11	3
HCSL[2]	1.8	Low-Power	2	13	3

Note:

1. The Sub-LVDS common mode voltage is not compliant with LVDS standards. Therefore, AC coupling the driver to an LVDS receiver is highly recommended.
2. Creates HCSL compatible signals, see HCSL receiver biasing network in Figure 16.

The output differential driver can also produce a wide range of CML compatible output amplitudes. See Chapter 15. Custom Differential Amplitude Controls for additional information.

6.4 LVCMOS Outputs

6.4.1 LVCMOS Output Terminations

LVCMOS outputs may be ac- or dc-coupled, although it is expected that 1 Hz outputs will be DC coupled as shown in the figure in Section . AC coupling is recommended for best jitter and phase noise performance. For dc-coupled LVCMOS, as shown again in the figure below, series termination resistors are required in order to increase the total source resistance to match the trace impedance of the circuit board. LVCMOS outputs can be set to in-phase or complementary.

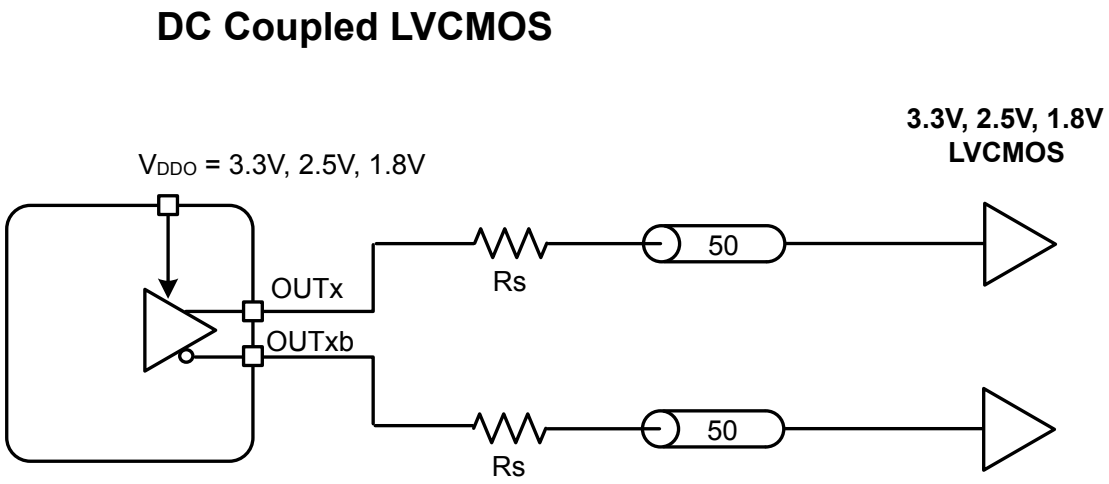


Figure 6.4. LVCMOS Output Terminations

6.4.2 LVCMOS Output Impedance and Drive Strength Selection

Each LVCMOS driver has a configurable output impedance to accommodate different trace impedances and drive strengths. A series source termination resistor (Rs) is recommended close to the output to match the selected output impedance to the trace impedance (i.e. Rs = Trace Impedance – Zs). There are multiple programmable output impedance selections for each VDDO option as shown in the table below. Generally, the lowest impedance for a given supply voltage is preferable, since it will provide the fastest edge rates.

Table 6.7. LVCMOS Output Impedance and Drive Strength Selections

VDDO	OUTx_CMOS_DRV	Source Impedance (Zs)	Drive Strength (Iol/Ioh)
3.3 V	0x01	38 Ω	10 mA
	0x02	30 Ω	12 mA
	0x03*	22 Ω	17 mA
2.5 V	0x01	43 Ω	6 mA
	0x02	35 Ω	8 mA
	0x03*	24 Ω	11 mA
1.8 V	0x02	46 Ω	4 mA
	0x03*	31 Ω	5 mA

Note:
1. Use of the lowest impedance setting is recommended for all supply voltages for best edge rates.

Table 6.8. LVCMOS Drive Strength Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_CMOS_DRV	0113[7:6]	LVCMOS output impedance. See the table above.
OUT1_CMOS_DRV	0118[7:6]	
OUT2_CMOS_DRV	011D[7:6]	
OUT3_CMOS_DRV	0127[7:6]	
OUT4_CMOS_DRV	012C[7:6]	
OUT5_CMOS_DRV	0131[7:6]	
OUT6_CMOS_DRV	013B[7:6]	

6.4.3 LVCMOS Output Signal Swing

The signal swing (V_{OL}/V_{OH}) of the LVCMOS output drivers is set by the voltage on the VDDO pins. Each output driver has its own VDDO pin allowing a unique output voltage swing for each of the LVCMOS drivers. Each output driver voltage is set by the OUTx_VDD_SEL setting.

6.4.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output it generates a clock signal on both pins (OUTx and OUTxb). By default the clock on the OUTx pin is generated with the same polarity (in phase) with the clock on the OUTxb pin. The polarity of these clocks is configurable enabling complimentary clock generation and/or inverted polarity with respect to other output drivers.

Table 6.9. LVCMOS Output Polarity Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_INV	0115[7:6]	Controls output polarity of the OUTx and OUTxb pins when in LVCMOS mode. Selections are:
OUT1_INV	011A[7:6]	
OUT2_INV	011F[7:6]	
OUT3_INV	0129[7:6]	
OUT4_INV	012E[7:6]	
OUT5_INV	0133[7:6]	
OUT6_INV	013D[7:6]	

6.5 Output Enable/Disable

The Si5383/84 OEb pin provides a convenient method of disabling or enabling the output drivers. When the OEb pin is held high, all outputs are disabled. When held low, the outputs are enabled. Outputs in the enabled state can be individually disabled through register control.

6.5.1 Output Disable State Selection

When the output driver is disabled, the outputs will drive either logic high or logic low, selectable by the user. The output common mode voltage is maintained while the driver is disabled, reducing enable/disable transients.

By contrast, powering down the driver rather than disabling it increases output impedance and shuts off the output common mode voltage. For all output drivers connected in the system, it is recommended to use Disable rather than Powerdown to reduce enable/disable common mode transients. Unused outputs may be left unconnected, powered down to reduce current draw, and, with the corresponding VDDOx, left unconnected.

6.5.2 Output Disable During LOL

By default a DSPLL that is out of lock will generate an output clock . In standard input mode, there is an option to disable the outputs when a DSPLL is out of lock (LOL). This option can be useful to force a downstream PLL into holdover.

6.5.3 Output Disable During XAXB_LOS

The internal oscillator circuit, in combination with the external crystal, provides a critical function for the operation of the DSPLLs. In the event of a crystal failure the device will assert an XAXB_LOS alarm. By default all outputs will be disabled during assertion of the XAXB_LOS alarm.

6.5.4 Output Driver State When Disabled

The disabled state of an output driver is register-configurable as disable low or disable high.

Table 6.10. Output Enable/Disable Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUTALL_DISABLE_LOW	0102[0]	Allows disabling all output drivers: 0 - all outputs disabled, 1 - all outputs controlled by the OUTx_OE bits. Note that if the OEb pin is held high (disabled), then all assigned outputs will be disabled regardless of the state of this register bit.
OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE	0112[1] 0117[1] 011C[1] 0126[1] 012B[1] 0130[1] 013A[1]	Allows enabling/disabling individual output drivers. Note that the OEb pin must be held low in order to enable an output with these register bits.
OUT_DIS_MASK_LOL_PLL(D,C,B,A)	0142[3:0]	Determines if the outputs are disabled during an LOL condition. 0 = outputs disable on LOL, 1 = outputs remain enabled during LOL (default). This option is independently configured for each DSPLL. See DRVx_DIS_SRC registers.
OUT_DIS_MSK_LOSXAXB	0141[6]	Determines if outputs are disabled during an LOSXAXB condition. 0 = all outputs disabled on LOSXAXB (default), 1 = outputs remain enabled during LOSXAXB condition.

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_DIS_STATE	0113[5:4]	Sets the state for the outputs when they are disabled.
OUT1_DIS_STATE	0118[5:4]	
OUT2_DIS_STATE	011D[5:4]	
OUT3_DIS_STATE	0127[5:4]	
OUT4_DIS_STATE	012C[5:4]	
OUT5_DIS_STATE	0131[5:4]	
OUT6_DIS_STATE	013B[5:4]	

6.5.5 Synchronous/Asynchronous Output Selection

Outputs can be configured to enable and disable either synchronously or asynchronously. In synchronous disable mode the output will wait until a clock period has completed before the driver is disabled. This prevents unwanted runt pulses from occurring when disabling an output. In asynchronous disable mode, the output clock will disable immediately without waiting for the period to complete.

Table 6.11. Synchronous/Asynchronous Disable Control Registers

Setting Name	Address: 0xXX:XX[Bit]	Function
	Si5383/84	
OUT0_SYNC_EN	0113[3]	Selects Synchronous or Asynchronous output disable. 1= synchronous, 0 = asynchronous. Default is asynchronous mode.
OUT1_SYNC_EN	0118[3]	
OUT2_SYNC_EN	011D[3]	
OUT3_SYNC_EN	0127[3]	
OUT4_SYNC_EN	012C[3]	
OUT5_SYNC_EN	0131[3]	
OUT6_SYNC_EN	013B[3]	

6.5.6 Output Driver Disable Source Summary

There are a number of conditions that may cause the outputs to be automatically disabled. The user may mask out unnecessary disable sources to match the system requirements. Any one of the unmasked sources may cause the outputs to be disabled; this is more powerful but similar in concept to open source “wired-OR” configurations. The table below summarizes the output disable sources with additional information for each source.

Table 6.12. Output Driver Disable Sources Summary

Output Driver Disable Source	Disable Outputs when Source	Individually Assignable?	Maskable?	Related Registers[Bits] (Hex)	Comments
				Si5383/84	
OUTALL_DISABLE_LOW	Low	N	N	0102[0]	User Controllable

Output Driver Disable Source	Disable Outputs when Source	Individually Assignable?	Maskable?	Related Registers[Bits] (Hex)	Comments
				Si5383/84	
OUT0_OE OUT1_OE OUT2_OE OUT3_OE OUT4_OE OUT5_OE OUT6_OE	Low	Y	N	0112[1] 0117[1] 011C[1] 0126[1] 012B[1] 0130[1] 013A[1]	User Controllable
LOL_PLL[D:A]	High	Y	Y	000D[3:0], 0142[3:0]	Maskable separately for each DSPLL. Should not be used when operating in PSS Mode.
LOS_XAXB	High	N	Y	000C[1], 0141[6]	Maskable
SYSINCAL	High	N	N	000C[0]	Automatic, not user-controllable or maskable

6.5.7 Output Buffer Voltage Selection

The power supply setting is used to calculate VCM and amplitude levels for the various output logic options. The OUTx_VDD_SEL_EN is always enabled and set to a logic 1. The power supply voltages on the VDDOx pins should match the voltage settings used in CBPro. Register values should be updated if any changes are made to the VDDOx voltages.

Table 6.13. Output Driver Voltage Selection

Setting Name	Reg Address	Descrption
OUT0_VDD_SEL_EN	0x0115 [3]	These bits are set to 1 and should not be changed.
OUT1_VDD_SEL_EN	0x011A [3]	
OUT2_VDD_SEL_EN	0x011F [3]	
OUT3_VDD_SEL_EN	0x0129 [3]	
OUT4_VDD_SEL_EN	0x012E [3]	
OUT5_VDD_SEL_EN	0x0133 [3]	
OUT6_VDD_SEL_EN	0x013D [3]	
OUT0_VDD_SEL	0x0115 [5:4]	These bits are set by CBPro to match the expected VDDOx voltage.
OUT1_VDD_SEL	0x011A [5:4]	00: 3.3 V
OUT2_VDD_SEL	0x011F [5:4]	01: 1.8 V
OUT3_VDD_SEL	0x0129 [5:4]	10: 2.5 V
OUT4_VDD_SEL	0x012E [5:4]	11: Reserved
OUT5_VDD_SEL	0x0133 [5:4]	
OUT6_VDD_SEL	0x013D [5:4]	

7. Digitally Controlled Oscillator (DCO) Mode

Digital controlled oscillator, DCO, mode is designed to provide small glitchless output frequency changes. The Si5383/84 DCO can be used in two different modes. The first is when the PLL is locked and the frequency is adjusted, by either register writes or hardware pin updates. Typical applications include FIFO management, frequency margining, direct digital synthesizer (DDS), numerically controlled oscillator (NCO) or a variable local oscillator as examples. The other mode is when DSPLLD is not locked and DCO control is external such as IEEE1588 / APTS applications. NOTE, this mode of operation doesn't achieve perfect frequency accuracy and is intended to be used with closed loop control only.

The DSPLLs support a DCO mode where the output frequencies are adjustable in pre-defined step values set by frequency step words (FSTEPW). The frequency adjustments are controlled through the I2C interface commands or by pin control using frequency increments (FINC) or decrements (FDEC) for Standard Input mode (does not apply to 1PPS input applications). An FINC will add the frequency step word to the DSPLL, increasing the output frequency, while a FDEC will decrement it. CBPro provides all the necessary configurations for Frequency Increment/Decrement via FINC/FDEC register and pin control. Alternatively, the step size value can be calculated and variable step size adjustments made by direct registers writes to M_NUM_PLLn. See AN909 for additional details, with the exception that DSPLLB is not normally modified.

Utlizing DCO mode when the PLL is unlocked is mainly used in IEEE1588 (PTP) applications, where a clock needs to be generated and timed based on recovered timestamps. In this case timestamps are recovered by the PHY/MAC. A processor containing servo loop software controls the DCO phase/frequency to close the timing loop between the master and slave IEEE1588 nodes. The processor has the option of using the FINC/FDEC pin controls to update the DCO frequency, for DSPLLA /C and DSPLLD exluding 1PPS opertation, or by controlling it through the serial interface.

When operating in 1PPS input mode, an additional enhanced DCO mode is enabled in the holdover state to facilitate DCO steering. In this case, DCO steering is accomplished I2C interface/writes and the step size is determined when building project plans in CBPro, in this case AN909 does not apply. DCO mode is useful for applications that require Assisted Partial Timing Support (APTS).

DCO mode can be envoked on DSPLLA, DSPLLC and DSPLLD while in standard input mode and when locked, but not when in Free Run or Holdover modes. Contact Applications Engineering if DCO mode is required in these cases. When the input(s) are 1PPS, then DSPLLD can operate in DCO mode when in FreeRun or Holdover but not locked.

Note that the maximum FINC/FDEC update rate, by either hardware or software, is 1 MHz. Please contact Factory Applications support for DCO operation when the Project file results in PFD values < 30 kHz. You must ensure that FINC or FDEC writes don't result in exceeding the DCO range.

7.1 Frequency Increment/Decrement Using Pin Controls

Controlling the output frequency with pin controls (FINC/FDEC) is available on the Si5383/84 when operating in Standard Input mode. This feature involves asserting the FINC or FDEC pins to increment or decrement the DSPLL frequency. The DSPLL selection is done through I2C commands M_FSTEP_MSK_PLLx. A set of mask bits selects the DSPLL(s) that is affected by the frequency change. The frequency step words (FSTEPW) defines the amount of frequency change for each FINC or FDEC. The FSTEPW may be written once or may be changed after every FINC/FDEC assertion. Both the FINC and FDEC inputs are rising-edge-triggered and must meet the Minimum Pulse Width specifications. The FINC and FDEC pins can also be used to trigger a frequency change. Note that both the FINC and FDEC register bits are rising-edge-triggered and self-clearing.

Note: FINC and FDEC should be connected to GND when unused.

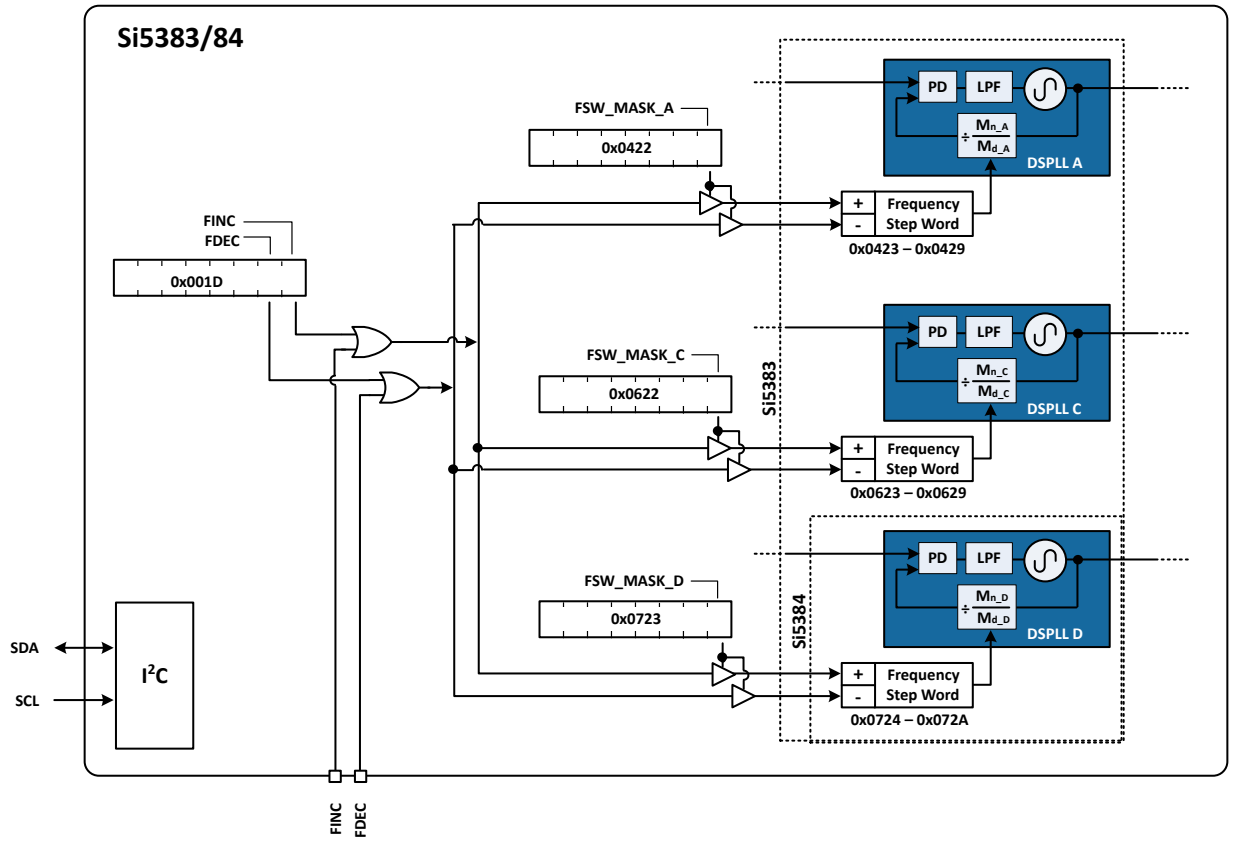


Figure 7.1. Controlling the DCO Mode by Serial Interface

Table 7.1. Frequency Increment/Decrement Control Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
FINC	001D[0]	Asserting this bit will increase the DSPLL output frequency by the frequency step word.
FDEC	001D[1]	Asserting this bit will decrease the DSPLL output frequency by the frequency step word.
M_FSTEPW_PLLA[1]	0423[7:0] - 0429[7:0]	This is a 56-bit frequency step word for DSPLL A, C, D. The FSTEPW will be added or subtracted to the DSPLL output frequency during assertion of the FINC/FDEC bits or pins. The FSTEPW is calculated based on the frequency configuration and is easily calculated using ClockBuilder Pro utility.
M_FSTEPW_PLLC[1]	0623[7:0] - 0629[7:0]	
M_FSTEPW_PLLD	0724[7:0] - 072A[7:0]	
M_FSTEP_MSK_PLLA[1]	0422[0]	This mask bit determines if a FINC or FDEC affects DSPLL A, C, D. 0 = FINC/FDEC will increment/decrement the FSTEPW to the DSPLL. 1 = Ignores FINC/FDEC.
M_FSTEP_MSK_PLLC[1]	0622[0]	
M_FSTEP_MSK_PLLD	0723[0]	

Note:
1. Si5383 only.

Table 7.2. Frequency Increment/Decrement Control Registers, 1PPS Mode

Setting Name	Hex Address [Bit Field]	Function
DCO_FSTEPW	0x5350[6:0]-0x5353[7:0]	This values specifies the DCO adjustment to be used on the next increment/decrement.
DCO_STEPW_CMD	0x5354[1:0]	DCO Frequency Step Command - Command returns to 00 when complete.

8. Serial Interface

Configuration and operation of the Si5383/84 is controlled by reading and writing registers using the I²C serial interface. The Si5383/84 only supports communication with a 3.3 V host. See Figure 8.1 for supported mode of operation and settings. The I²C pins are open drain and are ESD clamped to 3.3 V.

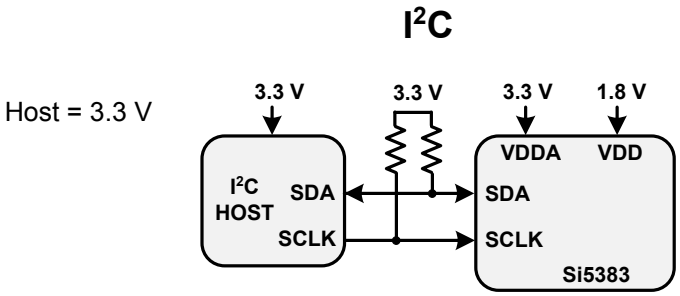


Figure 8.1. I²C Device Connectivity Configurations

If the serial interface is not used, pull pins SDA and SCL low. Note that the Si5383/84 is not I²C failsafe upon loss of power. Applications that require failsafe operation should isolate the device from a shared I²C bus.

8.1 I²C Interface

The I²C serial interface operates in slave mode with 7-bit addressing and can operate in Standard-Mode (100 kbps) or Fast-Mode (400 kbps) and supports burst data transfer with auto address increments. Note that clock stretching may be used above 100 kbps. The I²C bus consists of a bidirectional serial data line (SDA) and a serial clock input (SCL) as shown in the figure 8.4. Both the SDA and SCL pins must be connected to a supply via an external pull-up (4.7 kΩ) as recommended by the I²C specification as shown in the figure below.

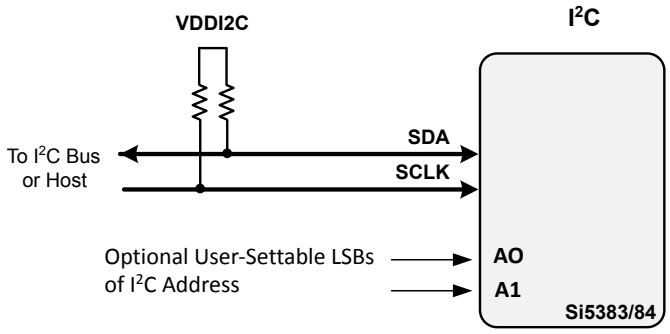


Figure 8.2. I²C Configuration

The 7-bit slave device address of the Si5383/84 consists of a 5-bit fixed address plus two pins that are selectable for the last two bits as shown below. When generating an OPN, the upper 5-bits are configurable and there is even an option to create a 7-bit fixed address for applications that do not desire the A1/A0 flexibility.

	6	5	4	3	2	1	0
User-Settable Slave Address	1	1	0	1	1	A1	A0

Figure 8.3. 7-bit I²C Slave Address Bit-Configuration

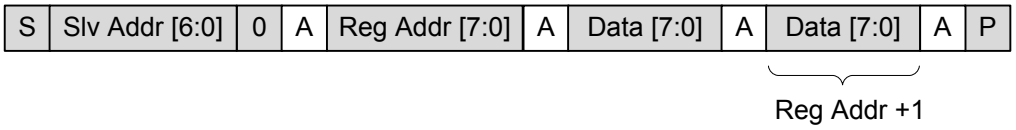
The A0 and A1 pins determine the two lower bits of the I²C slave address. They function as inputs during reset assertion with the state latched on reset negation. Post reset, these pins function as outputs. As a result, these signals should be set to the desired value with pullup/pulldown resistors and not an active driver. The upper 5 bits are 0x6C, but can be configurable in CBPro and then devices are supplied under an OPN.

A 4.7 kΩ pull-up to V_{DDA} or a 4.7 kΩ pull-down to ground should be used to set two lower bits of the I²C slave address.

Data is transferred MSB first in 8-bit words as specified by the I²C specification. A write command consists of a 7-bit device (slave) address + a write bit, an 8-bit register address, and 8 bits of data as shown in the figure titled I²C Write Operation. A write-burst operation is also shown where subsequent data words are written using to an auto-incremented address.

Write Operation – Single Byte

Write Operation - Burst (Auto Address Increment)



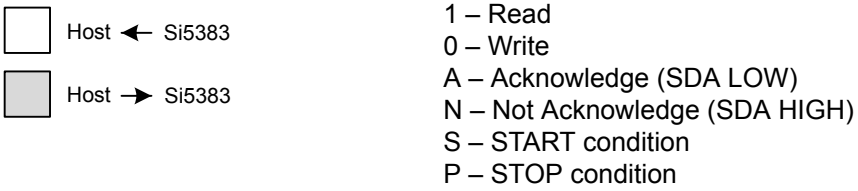
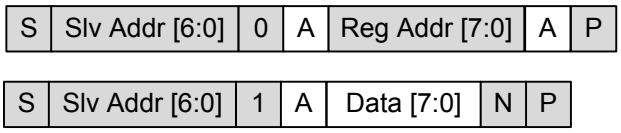


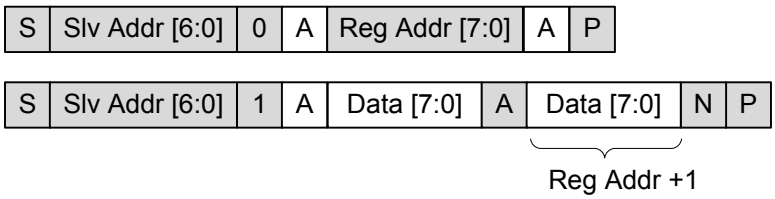
Figure 8.4. I²C Write Operation

A read operation is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. A read burst operation is also supported. This is shown in the figure below.

Read Operation – Single Byte



Read Operation - Burst (Auto Address Increment)



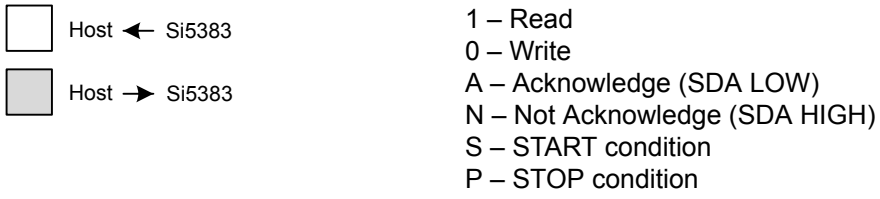


Figure 8.5. I²C Read Operation

9. Field Programming

To simplify design and software development of systems using the Si5383/84, a field programmer is available in addition to the evaluation board. The ClockBuilder Pro Field Programmer supports both “in-system” programming (for devices already mounted on a PCB), as well as “in-socket” programming of Si5383/84 devices.

10. Recommended Crystals and External Oscillators

10.1 External Reference (XA/XB, REF/REFb)

The external crystal at the XA/XB pins determines jitter performance of the output clocks, and the external reference clock at the REF/REFb pins determines the frequency accuracy during free-run and stability in holdover modes. Jitter from the external clock on the REF/REFb pins will have little to no effect on the output jitter performance, depending upon the selected bandwidth. This allows using a TCXO/OCXO with a higher phase noise floor, but good close-in phase noise performance, resulting in good MTIE and TDEV as well as phase jitter performance.

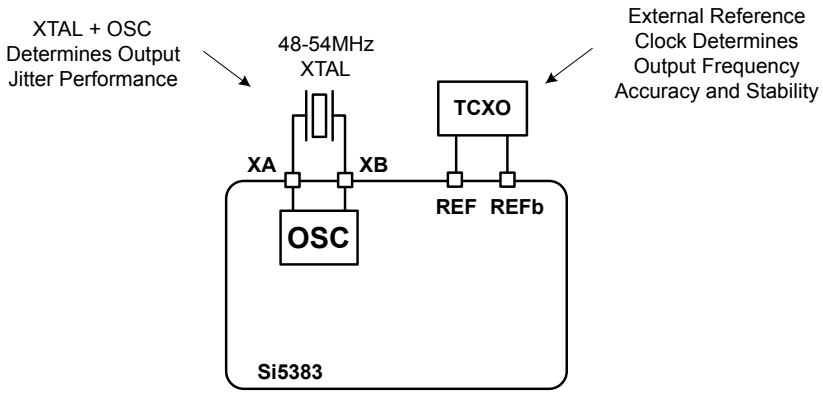


Figure 10.1. External Reference Connections

10.2 Performance of External References

An external standard non-pullable crystal (XTAL) is recommended in combination with the internal oscillator (OSC) to produce an ultra low phase noise reference clock for the DSPLL, as well as providing a stable reference for the Freerun and Holdover modes. Simplified connection diagrams are shown below. The device includes internal 8 pF crystal loading capacitors which eliminates the need for external capacitors and also has the benefit of reduced noise coupling from external sources. In most applications, using the internal OSC with an external crystal provides the best phase noise performance. Although the device includes built-in XTAL load capacitors (CL) of 8 pF, crystals with load capacitances up to 18 pF can also be accommodated. Frequency offsets due to CL mismatch can be adjusted using the frequency adjustment feature which allows frequency adjustments of ±1000 ppm. See AN905: Si534x External References; Optimizing Performance for more information on the performance of various XO's with these devices. The recommended crystal suppliers are listed in the table titled Recommended Crystals in Section 10.3 Recommended Crystals with PCB layout recommendations for the crystal to ensure optimum jitter performance in Chapter 11. Crystal and Device Circuit Layout Recommendations.

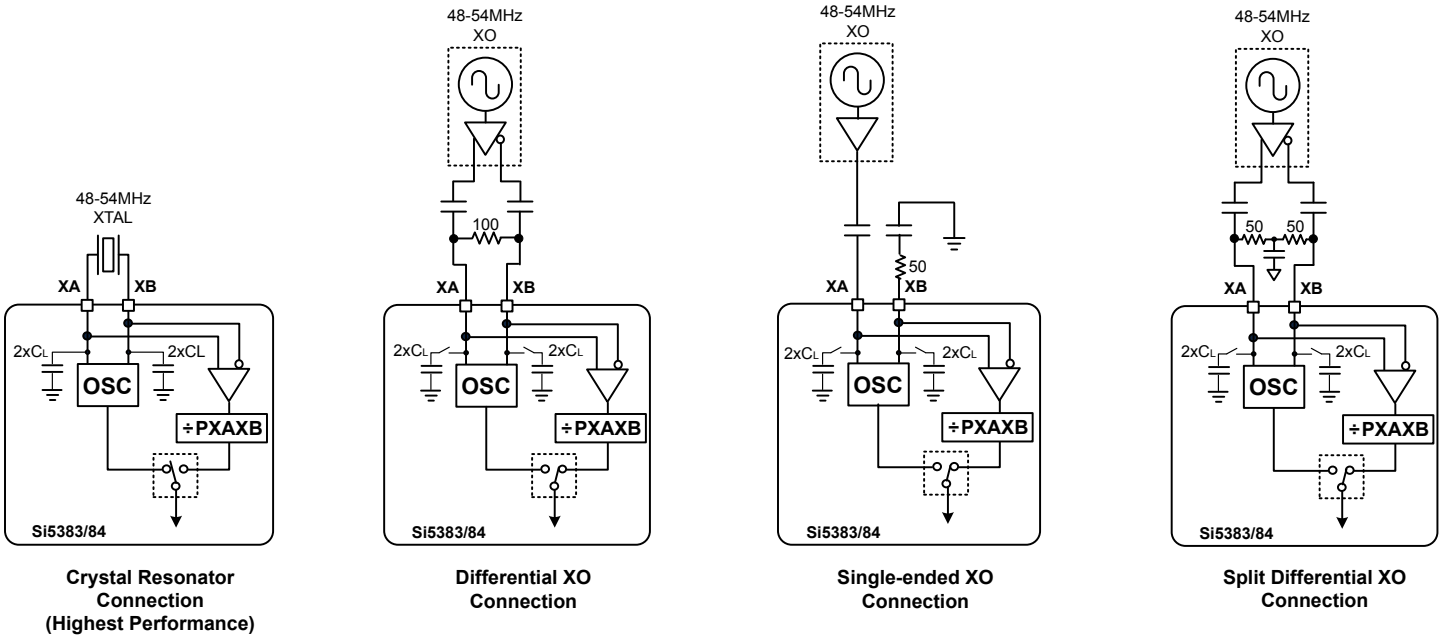


Figure 10.2. XAXB Crystal Resonator and External Reference Clock Connections

Although the Si5383/84 can accept an external clock signal on its XA/XB pins, for best possible jitter performance, it is strongly recommended that an approved crystal be used. There is essentially no jitter attenuation from the XA/XB pins to the output clocks and ony the best XOs will avoid a jitter penalty compared to using an approved crystal. If an XO must be used, a differential connection is suggested for best performance.

10.3 Recommended Crystals

See the Si534x/8x Jitter Attenuators Recommended Crystal, TCXO and OCXOs Reference Manual for recommended crytsal, TCXO, and OCXO sources.

10.4 Recommended Oscillators for the Ref / Refb inputs.

The external REF/REFb performance will determine the Si5383/84's output frequency accuracy and stability under Free Run operation, stability under Holdover as well as performance under locked conditions such as MTIE/TDEV noise generation. This reference is usually a TCXO or OCXO, which nomially have a single ended CMOS output, and are connected per the figures below. The TCXO or OCXO initial tolerance will determine the Si5383/84 output frequency accuracy under Free Run while the temperature performance will dominate stability under Free Run and Holdover over temperature. The TCXO and OCXO close-in phase noise performance and superior short term stability are critical to MTIE/TDEV noise generation/output phase stability performance. The OCXO and TCXO phase noise performance/short and long term stability become even more critical at lower loop BW's, therefore close attention to the selected OCXO/TCXO performance is required to ensure it meets system requirements when operating with low loop bandwidths. The TCXO/OCXO frequency can be any value between 5 MHz to 250 MHz, however using a higher frequency will not improve the Si5383/84 phase jitter performance and will most likely increase cost and degrade aging performance. Common low frequencies for consideration include 10 MHz, 12.800 MHz and 20 MHz.

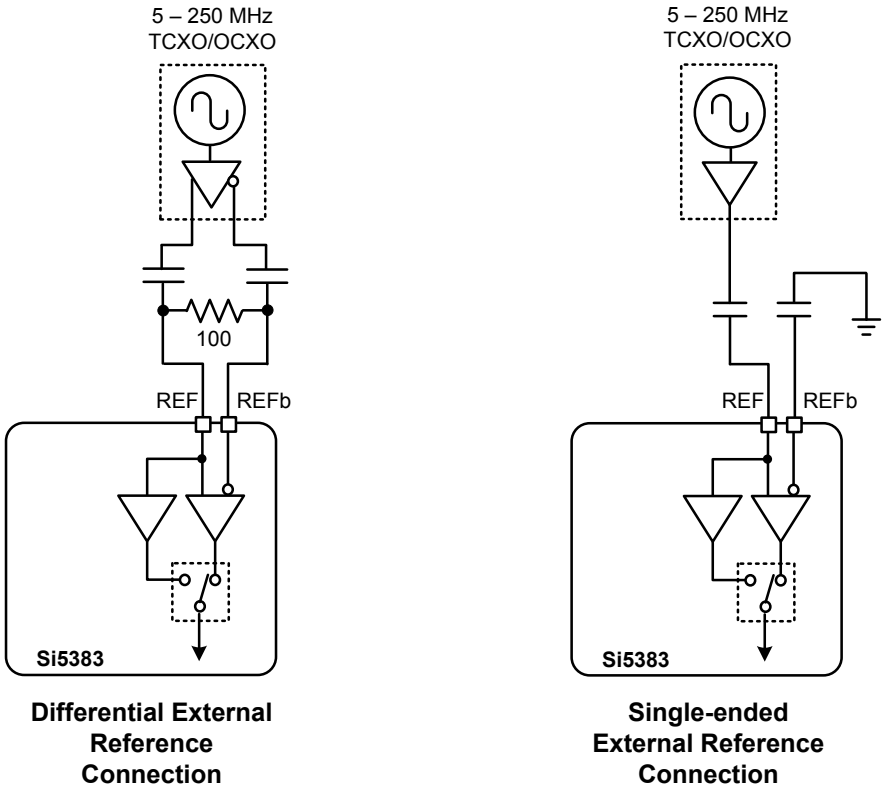


Figure 10.3. Reference Input Connections

10.5 Register Settings to Configure for External XTAL Reference

The following registers can be used to control and make adjustments for the external reference source used.

10.5.1 XAXB_FREQ_OFFSET Frequency Offset Register

Table 10.1. Crystal External Oscillator Selection

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
XAXB_EXTCLK_EN	0x0090E [0]	Selects between using an external crystal versus crystal oscillator.

The internal crystal loading capacitors (CL) are disabled when an external clock source is selected.

Table 10.2. Pre-Scale Divide Ratio Register

Setting Name	Hex Address [Bit Field]	Function
PXAXB	0x0206[1:0]	This is a two bit value that sets the divider value.

Table 10.3. XAXB Frequency Offset Registers

Setting Name	Hex Address [Bit Field]	Function
XAXB_FREQ_OFFSET	0x0202[7:0]-0x0205[7:0]	32-bit number which allows adjustment to the center frequency of the XTAL in the range of ±1000ppm. A SOFT_ RST is required in XAXB_FREQ_OFFSET is modified.

11. Crystal and Device Circuit Layout Recommendations

The main layout issues that should be carefully considered include the following:

- Number and size of the ground vias for the Epad (see Section 12.4 Grounding Vias.)
- Output clock trace routing
- Input clock trace routing
- Control and Status signals to input or output clock trace sampling
- Xtal signal coupling
- Xtal layout

If the application uses a crystal for the XAXB inputs a shield should be placed underneath the crystal connected to the X1 and X2 pins to provide the best possible performance. The shield should not be connected to the ground plane(s), and the layers underneath should have as little cooper under the shield as possible. It may be difficult to do this for all the layers, but it is important to do this for the layers that are closest to the shield.

Go to https://www.skyworksinc.com/search?q=si538%20evaluation to obtain Si5383-EVB schematics, layouts, and component BOM files.

11.1 56-Lead LGA Si5383/84 Layout Recommendations

This section details the recommended guidelines for the crystal layout of the 56-pin Si5383/84 device using an example 6-layer PCB. The following are the descriptions of each of the eight layers.

- Layer 1: Device layer, with low speed CMOS control/status signals
- Layer 2: RF route and ground
- Layer 3: Ground plane
- Layer 4: Power distribution and ground
- Layer 5: RF route and ground
- Layer 6: Low speed CMOS and ground

The following figure shows the top layer layout of the Si5383/84 device mounted on the top PCB layer. The crystal area is outlined with the white box around it. In this case, the top layer is flooded with ground. Note that this layout has a resistor in series with each pin of the crystal. In typical applications, these resistors should be removed.

11.1.1 Si5383/84 Crystal Guidelines

The following are five recommended crystal guidelines:

1. Place the crystal as close as possible to the XA/XB pins.
2. *Do not* connect the crystal's X1 or X2 pins to PCB ground.
3. Connect the crystal's GND pins to the DUT's X1 and X2 pins via a local crystal shield placed around and under the crystal. Notice in the top and 2nd layer figures below that create a crystal shield below the crystal by placing vias connecting the top layer traces to the shield layer underneath.
4. Minimize traces adjacent to the crystal/oscillator area especially if they are clocks or frequently toggling digitial signals.
5. In general do not route GND, power planes/traces, or locate components on the other side, below the crystal GND shield. As an exception if it is absolutely necessary to use the area on the other side of the board for layout or routing, then place the next reference plane in the stack-up at least two layers away or at least 0.05 inches away. The Si5383/84 should have all layers underneath the ground shield removed.

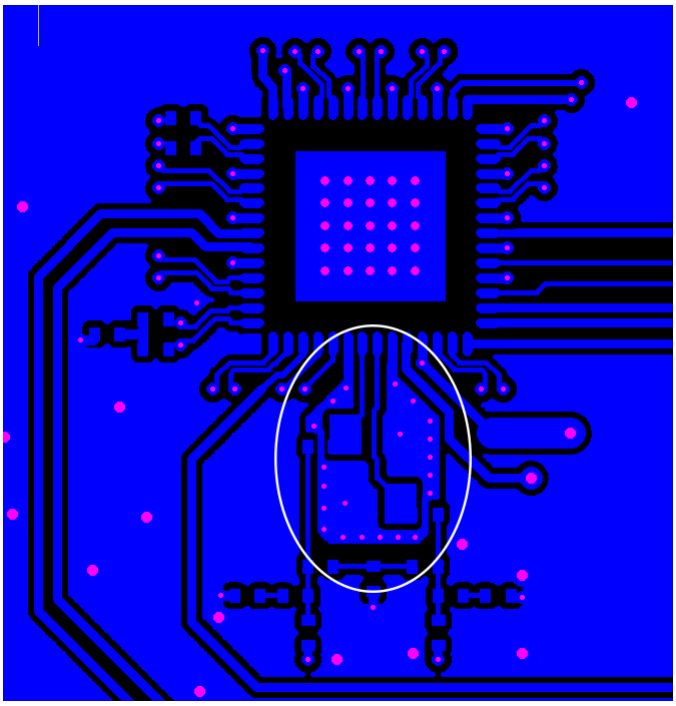


Figure 11.1. 56-lead Si5383/84 Crystal Layout Recommendations Top Layer (Layer 1)

The layer below is the shielding ground layer for the crystal. Notice the shield immediately under the crystal shown in the white circle. The clock output pins also go to this layer. The clock outputs go to layer 2 immediately using vias to avoid crosstalk. As soon as the clock outputs are on layer 2 they have a ground shield above below and on the sides for protection.

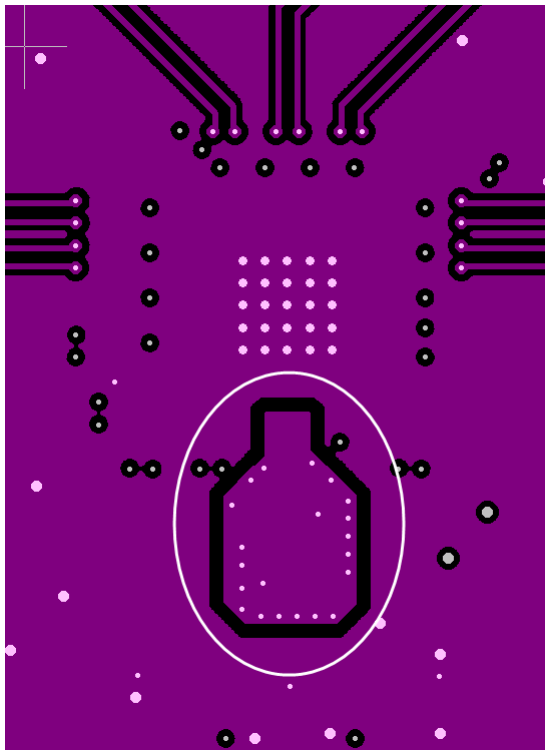


Figure 11.2. 56-lead Si5383/84 Crystal Layout Recommendations 2nd Layer with Ground Shield (Layer 2)

The figure above shows the layer that implements the shield underneath the crystal. The shield extends underneath the entire crystal and the X1 and X2 pins.

The figure below left is the ground plane and shows a void underneath the crystal shield. The figure below right is a power plane and shows the clock output power supply traces. The void underneath the crystal shield is continued.

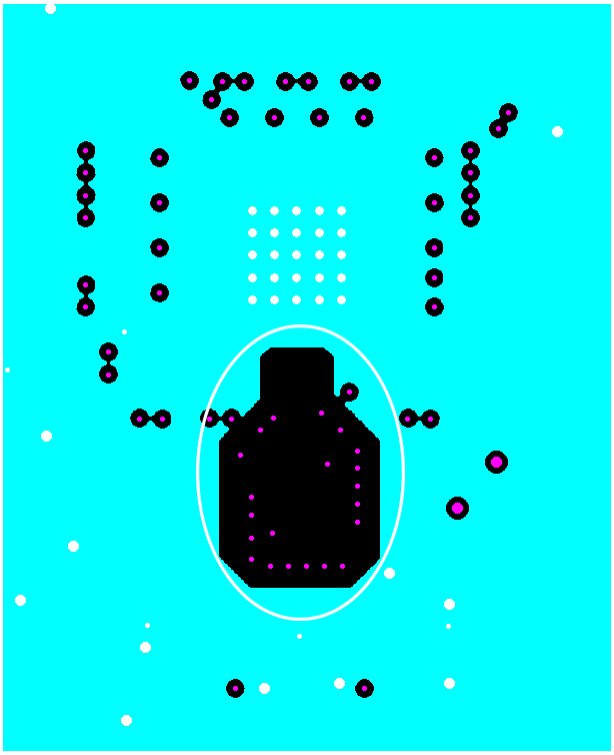


Figure 11.3. Crystal Ground Plane (Layer 3)

The figure below shows layer 4, is the power plane with the power routed to the clock output power pins.

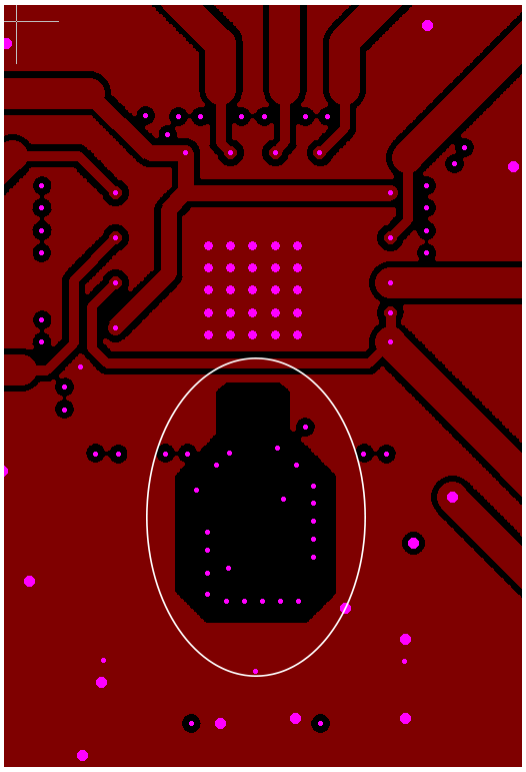


Figure 11.4. Power Plane (Layer 4)

This layer 5 is another ground layer. The clock input pins go to layer 5 using vias to avoid crosstalk. As soon as the clock inputs are on layer 5 they have a ground shield above below and on the sides for protection.

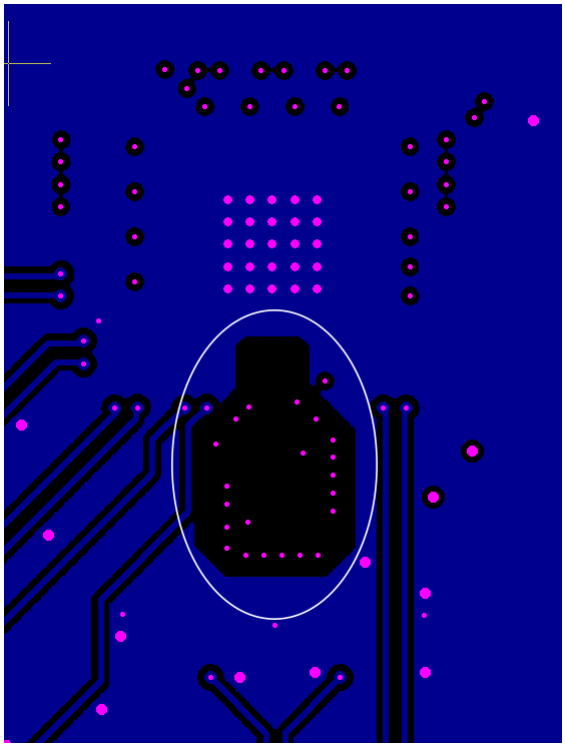


Figure 11.5. Layer 5 Ground Plane and Clock input Signals (Layer 5)

The figure below is the bottom layer of the board as a ground plane.

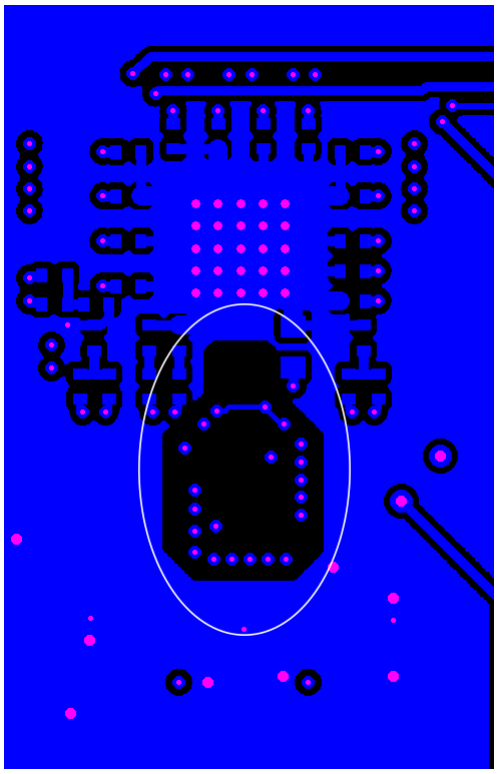


Figure 11.6. Ground Plane (Layer 6)

11.1.2 Si5383/84 Output Clocks

The figure below shows the output clocks. Similar to the input clocks, the output clocks have vias that immediately go to a buried layer with a ground plane above them and a ground flooded bottom layer. There is a ground flooding between the clock output pairs to avoid crosstalk. There shouuld be a line of vias through the ground flood on either side of the output clocks to ensure that the ground flood immediately next to the differential paris has a low inductance path to the ground plane on layers 1 and 3.

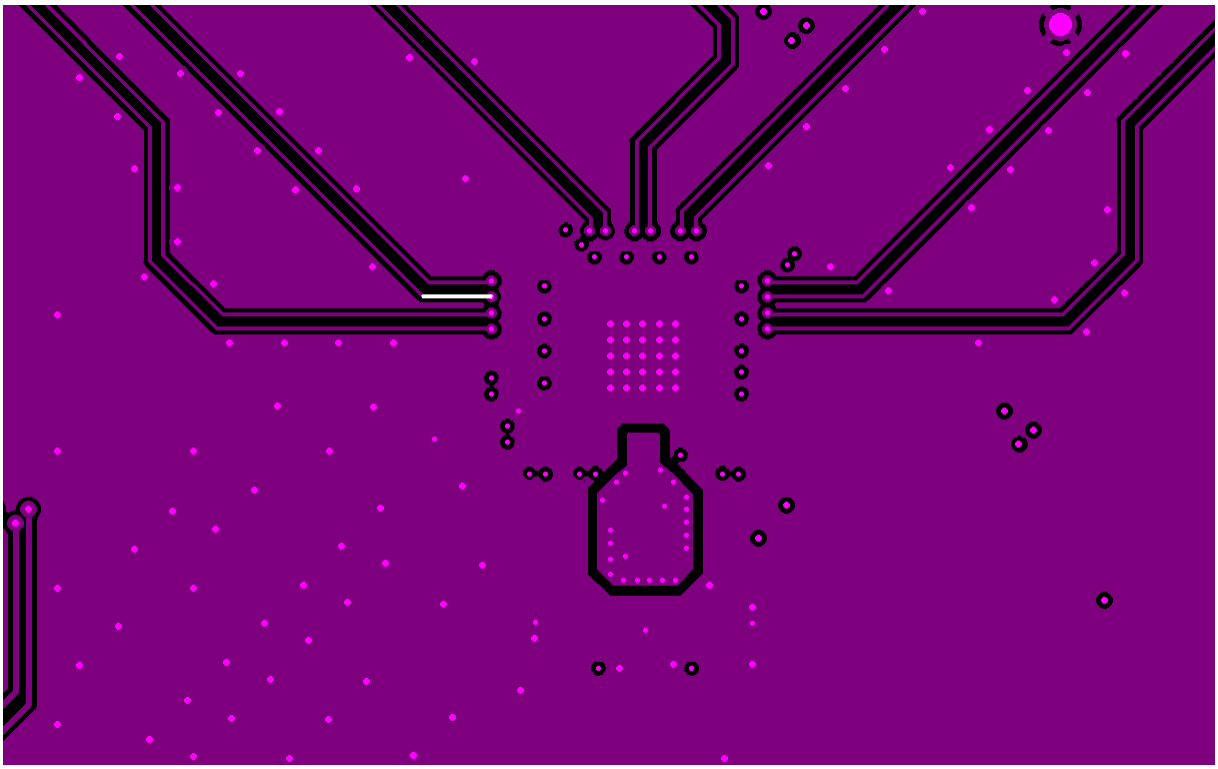


Figure 11.7. Output Clock Layer (Layer 2)

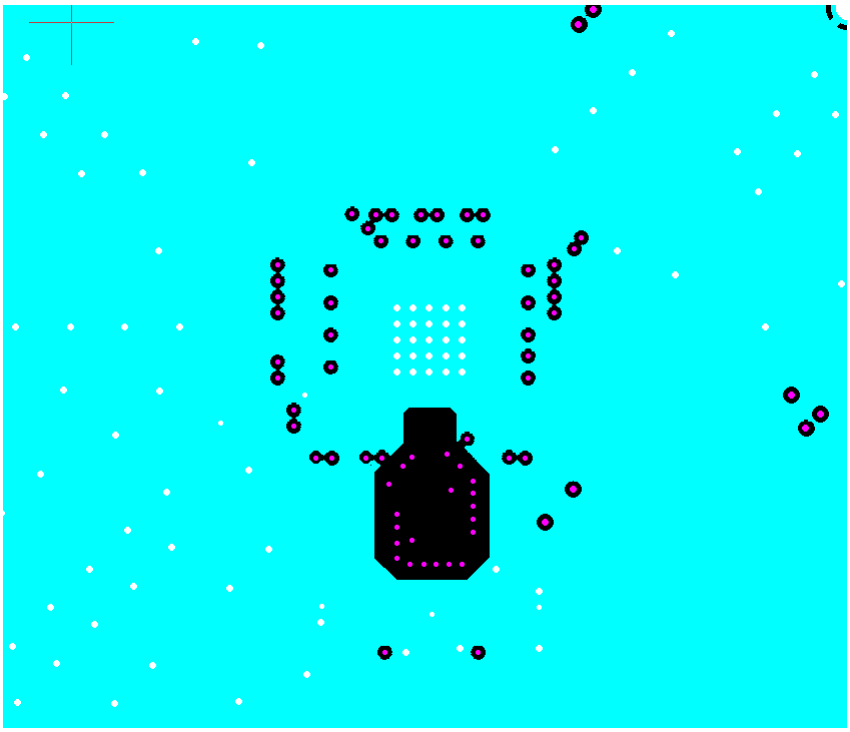


Figure 11.8. Bottom Layer Ground Flooded (Layer 3)

12. Power Management

12.1 Power Management Features

Several unused functions can be powered down to minimize power consumption. The registers listed in the table below are used for powering down different features.

Table 12.1. Power Management Registers

Setting Name	Hex Address [Bit Field]	Function
	Si5383/84	
OUT0_PDN	0x0112[0]	Logic 1 powers down unused clock outputs.
OUT1_PDN	0x0117[0]	
OUT2_PDN	0x011C[0]	
OUT3_PDN	0x0126[0]	
OUT4_PDN	0x012B[0]	
OUT5_PDN	0x0130[0]	
OUT6_PDN	0x013A[0]	
OUT_PDN_ALL	0x0145[0]	Power down all output drivers

12.2 Power Supply Recommendations

The power supply filtering generally is important for optimal timing performance. The Si5383/84 devices have multiple stages of on-chip regulation to minimize the impact of board level noise on clock jitter. Following conventional power supply filtering and layout techniques will further minimize signal degradation from the power supply.

It is recommended to use a 1 µF 0402 ceramic capacitor on each VDD for optimal performance. It is also suggested to include an optional, single 0603 (resistor/ferrite) bead in series with each supply to enable additional filtering if needed.

12.3 Power Supply Sequencing

Four classes of supply voltages exist on the Si5383/84:

1. VDD = 1.8 V ± 5% (Core digital supply)
2. VDDA = 3.3 V ± 5% (Core digital and analog supply)
3. VDDOx = 1.8/2.5/3.3 V ± 5% (Clock output supply)

There is no requirement for power supply sequencing unless the output clocks are required to be phase aligned with each other. In this case, the VDDO of each clock which needs to be aligned must be powered up before VDD and VDDA. If output-to-output alignment is required for applications where it is not possible to properly sequence the power supplies, then the output clocks can be aligned by asserting the SOFT_RST_ALL 0x001C[0] or Hard Reset 0x5303[0] register bits or driving the RSTb pin for more than 15 µs. Note that using a hard reset will reload the register with the contents of the NVM and any unsaved changes will be lost.

Note: One may observe that when powering up the VDD = 1.8 V rail first, that the VDDA = 3.3 V rail will initially follow the 1.8 V rail. Likewise, if the VDDA rail is powered down first then it will not drop far below VDD until VDD itself is powered down. This is due to the pad I/O circuits which have large MOSFET switches to select the local supply from either VDD or VDDA rails. These devices are relatively large and yield a parasitic diode bewteen VDD and VDDA. Please allow for both VDD and VDDA to power-up and power-down before measuring their respective voltages.

12.4 Grounding Vias

The pad on the bottom of the device functions as both the sole electrical ground annd prmary heat transfer path. Hence it is important to minmize the inductance and maximize the heat transfer from this pad to the internal ground plane of the PCB. Use no fewer than 25 vias from the center pad to a ground plane under the device. In general, more vias will perform better. Having the ground plane near the top layer will also help to minimize the via inductance from the device to ground and maximize the heat transfer away from the device.

13. Base vs. Factory Preprogrammed Devices

The Si5383/84 devices can be ordered as "base" or "factory-preprogrammed" (also known as "custom OPN") versions.

13.1 "Base" Devices (Also Known as "Blank" Devices)

- Example "base" orderable part numbers (OPNs) are of the form "Si5383A-Dxxxxx-GM" or "Si5383B-Dxxxxx-GM".
- Base devices are available for applications where volatile reads and writes are used to program and configure the device for a particular application.
- Base devices do not power up in a usable state (all output clocks are disabled).
- Base devices are, however, configured by default to use a 48 MHz crystal on the XAXB reference and a 3.3V compatible I/O voltage setting for the host I^2C interface.
- Additional programming of a base device is mandatory to achieve a usable configuration.
- See the online lookup utility at https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize to access the default configuration plan and register settings for any base OPN.

13.2 "Factory Preprogrammed" (Custom OPN) Devices

- Factory preprogammed devices using a "custom OPN", such as Si5383A-B-xxxxx-GM, where "xxxxx" is a sequence of characters assigned by Skyworks for each customer-specific configuration. These characters are referred to as the "OPN ID." Customers must initiate custom OPN creation using the ClockBuilder Pro software.
- Many customers prefer to order devices which are factory preprogrammed for a particular application that includes specifying the XAXB reference frequency/type, the input reference, the clock input frequencies, the clock output frequencies, as well as the other options, such as automatic clock selection, loop BW, etc. CBPro software is required to select among all of these options and to produce a project file that Skyworks uses to preprogram all devices with custom orderable part number ("custom OPN").
- Custom OPN devices contain all of the initialization information in their non-volatile memory (NVM) so that it powers up fully configured and ready to go.
- Because preprogrammed device applications are inherently quite different from one another, the default power up values of the register settings can be determined using the custom OPN utility at: https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize.
- Custom OPN devices include a device top mark that includes the unique OPN ID. Refer to the device data sheet's Ordering Guide and Top Mark sections for more details.

Both "base" and "factory preprogrammed" devices can have their operating configurations changed at any time using volatile reads and writes to the registers. Both types of devices can also have their current register configuration written to the flash based NVM multiple times (see Section).

14. Register Map

Si5383/84 registers reside in both direct memory space and indirect memory space. Direct registers are accessed by the host via the I2C interface as detailed in Section 8.1. Indirect registers are accessed by the host via a bridge function implemented by the direct registers. Indirect addressing expands the standard 256-byte address space supported by the I2C protocol to the 64-Kbyte address space required by the Si5383/84 registers.

14.1 Direct Memory Map

The direct memory map includes the Device Ready register (Table 14.1), the Write Bridge (Table 14.2), and the Read Bridge (Table 14.3). DEVICE_READY is a read-only byte that indicates the current state of the device. A value of 0x0F indicates the device is ready to accept register read/writes. Any value other than 0x0F indicates the device is not ready. The host should poll DEVICE_READY following a reset (POR, RSTb, or HARD_RST) to determine when it can safely configure/monitor the device.

Table 14.1. Si5383/84 Device Ready Register

Reg Address	Bit Field	Type	Name	Description
0xFE	7:0	R	DEVICE_READY	Device Ready - Register bit pattern indicates if the device is operational (i.e. ready). 8'h0F = Operational Others = Not Operational

The bridges are the conduit between the host and the indirect registers. It is via these bridge functions that the host performs indirect register accesses. Both read and write bridges utilize a command/polling protocol and support multi-byte transfers between 1 and 8 bytes. In addition, the write bridge supports command extensions that accelerate DCO mode updates. Detailed below are the steps required to access indirect registers.

Write Procedure

1. Host writes the 16-bit starting register address into WR_ADDR.
2. Host writes the desired register data into WR_DATAn (n = 0-7). The number of bytes written is a function of the transfer length. A 1-byte transfer requires only WR_DATA0, a 2-byte transfer requires both WR_DATA0 and WR_DATA1, and so on. When the write is triggered, WR_DATA0 will be written to WR_ADDR, WR_DATA1 will be written to WR_ADDR + 1, and so on.
3. Host writes the byte transfer length into WR_LENGTH. The value written should be one less than the desired number of bytes to transfer. For example, 0 would be written to transfer 1-byte, 1 would be written to transfer 2-bytes, and so on. It is recommended that this bit-field is written in the same cycle as WR_CMD to minimize overhead.
4. Host writes the desired write opcode (see Table 14.2) into WR_CMD. This triggers the indirect register write(s). WR_CMD returns to zero when the operation completes.
5. Host polls/waits for WR_CMD to return to zero indicating the indirect write operation has completed.

Read Procedure

1. Host writes the 16-bit starting register address into RD_ADDR
2. Host writes the transfer length into RD_LENGTH. The value written should be one less than the desired number of bytes to transfer. For example, 0 would be written to transfer 1-byte, 1 would be written to transfer 2-bytes, and so on. It is recommended that this bit-field is written in the same cycle as RD_CMD to minimize overhead
3. Host writes the read opcode into RD_CMD. This triggers the indirect register read(s). RD_CMD returns to zero when the operation completes
4. Host polls/waits for RD_CMD to return to zero indicating the indirect read operation has completed
5. Host reads the readback register data from RD_DATAn (n = 0-7). The number of bytes read is a function of the transfer length. A 1-byte transfer updates only RD_DATA0, a 2-byte transfer updates both RD_DATA0 and RD_DATA1, and so on. When the read is triggered, RD_DATA0 gets the value from RD_ADDR, RD_DATA1 gets the value from RD_ADDR + 1, and so on

The procedures detailed above are best illustrated with an example. Detailed below are the steps required to write/read P0_DEN[31:0] (Address = 0x020E – 0x0211). The value written in this example is 0x44332211.
Note, most multi-byte bit-fields such as P0_DEN[31:0] are stored in memory in little-endian format (LSB first). However, multi-byte bit-fields located in Page 0x53 and Page 0x54, such as LOL_CLR_THR[31:0] are stored in memory in big-endian format (MSB) format. Care must be taken when accessing these bit-fields to ensure proper byte ordering

Write Example

1. Write MSB of starting register address (0x02) to WR_ADDR[15:8] (0x20)
2. Write LSB of starting register address (0x0E) to WR_ADDR[7:0] (0x21)
3. Write data0 (0x11) to WR_DATA0 (0x22)
4. Write data1 (0x22) to WR_DATA1 (0x23)
5. Write data2 (0x33) to WR_DATA2 (0x24)
6. Write data3 (0x44) to WR_DATA3 (0x25)
7. Trigger a 4-byte write by writing 0x31 to the register occupied by WR_LENGTH and WR_CMD (0x2A)
8. Poll/wait for WR_CMD (0x2A) to return to zero

Read Example

1. Write MSB of starting register address (0x02) to RD_ADDR[15:8] (0x30)
2. Write LSB of starting register address (0x0E) to RD_ADDR[7:0] (0x31)
3. Trigger a 4-byte read by writing 0x31 to the register occupied by RD_LENGTH and RD_CMD (0x32)
4. Poll/wait for RD_CMD (0x32) to return to zero
5. Read data0 (0x11) from RD_DATA0 (0x33)
6. Read data1 (0x22) from RD_DATA1 (0x34)
7. Read data2 (0x33) from RD_DATA2 (0x35)
8. Read data3 (0x44) from RD_DATA3 (0x36)

Table 14.2. Si5383/84 Write Bridge Registers

Reg Address	Bit Field	Type	Name	Description
0x20	15:8	R/W	WR_ADDR	16-Bit Starting Write Address
0x21	7:0	R/W	WR_ADDR	
0x22	7:0	R/W	WR_DATA0	8-bit Write Data Data is written in order starting at WR_ADDR
0x23	7:0	R/W	WR_DATA1	
0x24	7:0	R/W	WR_DATA2	
0x25	7:0	R/W	WR_DATA3	
0x26	7:0	R/W	WR_DATA4	
0x27	7:0	R/W	WR_DATA5	
0x28	7:0	R/W	WR_DATA6	
0x29	7:0	R/W	WR_DATA7	
0x2A	7	R/W	RSVD	Reserved Write with 0 and ignore on reads
0x2A	6:4	R/W	WR_LENGTH	Write Transfer Length 0 = 1 byte 1 = 2 bytes … 7 = 8 bytes
0x2A	3	R/W	RSVD	Reserved Write with 0 and ignore on reads
0x2A	2:0	R/W	WR_CMD	Write Command – Returns to zero when write operation is complete 0 = Idle 1 = Write 2 = Write with auto FDEC 3 = Write with auto FINC 4 = Write with auto M_UPDATE_PLLA 5 = Write with auto M_UPDATE_PLLC 6 = Write with auto M_UPDATE_PLLD 7 = Reserved

Table 14.3. Si5383/84 Bridge Read Registers

Reg Address	Bit Field	Type	Name	Description
0x30	15:8	R/W	RD_ADDR	16-bit Starting Read Address
0x31	7:0	R/W	RD_ADDR	
0x32	7	R/W	RSVD	Reserved Write with 0 and ignore on reads

Reg Address	Bit Field	Type	Name	Description
0x32	6:4	R/W	RD_LENGTH	Read Transfer Length 0 = 1 byte 1 = 2 bytes … 7 = 8 bytes
0x32	3:2	R/W	RSVD	Reserved Write with 0 and ignore on reads
0x32	0	R/W	RD_CMD	Read Command – Returns to zero when write operation is complete 0 = Idle 1 = Read
0x33	7:0	R/W	RD_DATA0	8-bit Read Data Data is read from device in order starting at RD_ADDR
0x34	7:0	R/W	RD_DATA1	
0x35	7:0	R/W	RD_DATA2	
0x36	7:0	R/W	RD_DATA3	
0x37	7:0	R/W	RD_DATA4	
0x38	7:0	R/W	RD_DATA5	
0x39	7:0	R/W	RD_DATA6	
0x3A	7:0	R/W	RD_DATA7	

14.2 Indirect Memory Map

The indirect memory map includes all Si5383/84 configuration and status registers. A 16-bit address yields 64-Kbytes of addressable registers, however not all are used. The MSBy of the address is used to divide the register map into separate “Pages” of register banks. There are 256 pages each with a length of 256 bytes. These pages are used to organize the device functions within the register map as illustrated in Table 14.4.

It is recommended to use dynamic Read-Modify-Write methods when writing to registers which contain multiple settings, such as register 0x0011. To do this, first read the current contents of the register. Next, update only the select bit or bits that are being modified. This may involve using both logical AND and logical OR operations. Finally, write the updated contents back to the register. Writing registers or bits not documented below may cause undesired behavior in the device.

Details of the register and settings information are organized hierarchically below. To find the relevant information for your application, first identify the page of the desired function in Table 14.4. Then, choose the section associated with that page to obtain details of the relevant register(s).
Default register contents and settings differ for each device part number, or OPN. This information may be found by searching for the Custom OPN for your device using the link below. Both Base/Blank and Custom OPNs are available there. See the previous section on “Base vs. Factory Preprogrammed Devices" for more information on part numbers. The Private Addendum to the datasheet lists the default settings and frequency plan information. You must be logged into the Skyworks website to access this information. The Public addendum gives only the general frequency plan information

https://www.skyworksinc.com/en/Application-Pages/Timing-Lookup-Customize.

Table 14.4. Register Map Page Descriptions

Page	Start Address (Hex)	Start Address (Decimal)	Contents
Page 0	0000h	0	Alarms, interrupts, reset, and other configuration
Page 1	0100h	256	Output clock configuration
Page 2	0200h	512	P and R dividers, user scratch area
Page 3	0300h	768	Internal divider value updates
Page 4[2]	0400h	1024	DSPLLA
Page 5	0500h	1280	DSPLLB (Reference DSPLL)
Page 6[2]	0600h	1536	DSPLLC
Page 7	0700h	1792	DSPLLD
Page 9	0900h	2304	Control IO configuration
Page A	0A00h	2560	Internal divider enables
Page B	0B00h	2816	Internal clock disables and control
Page D	0D00h	3329	Phase Readout Registers
Page 53	5300h	21248	reset, I^2C address, IO configurations, and user scratch area
Page 53	5320h	21280	PPS Loop control, configuration and status
Page 54	5400h	21504	Phase Readout Registers, 1PPS loop

Note:

1. General comments:
   - R = Read Only
   - R/W = Read Write
   - S = Self Clearing
   - Registers that are sticky are cleared by writing “0” to the bits that have been set in hardware. A self-clearing bit will clear on its own when the state has changed.
2. Si5383 only.

14.3 Si5383/84 Register Map

14.3.1 Page 0 Registers Si5383/84

Table 14.5. Register 0x0000 Die Rev

Reg Address	Bit Field	Type	Setting Name	Description
0x0000	3:0	R	DIE_REV	4- bit Die Revision Number

Table 14.6. Register 0x0001 Page

Reg Address	Bit Field	Type	Setting Name	Description
0x0001	7:0	R/W	PAGE	Selects one of 256 possible pages.

The “Page Select” register is located at address 0x01 on every page, with exception of page 0x53 and 0x54. When read, it indicates the current page. When written, it will change the page to the value entered. There is a page register at address 0x0001, 0x0101, 0x0201, 0x0301, … etc.

Table 14.7. Register 0x0002-0x0003 Base Part Number

Reg Address	Bit Field	Type	Setting Name	Value	Description
0x0002	7:0	R	PN_BASE	0x83	Four-digit "base" part number, one nibble per digit. Example: Si5383A-B-GM. The base part number (OPN) is 5383, which is stored in this register.
0x0003	15:8	R	PN_BASE	0x53	

Table 14.8. Register 0x0004 Device Grade

Reg Address	Bit Field	Type	Setting Name	Description
0x0004	7:0	R	GRADE	One ASCII character indicating the device speed/synthesis mode. 0 = A 1 = B 2 = C 3 = D

Refer to the device data sheet Ordering Guide section for more information about device grades.

Table 14.9. Register 0x0005 Device Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x0005	7:0	R	DEVICE_REV	One ASCII character indicating the device revision level. 0 = A; 1 = B, etc. Example Si5383A-**B**12345-GM, the device revision is B and stored as 1.

Table 14.10. Register 0x0006-0x000A NVM Identifier, Pkg ID

Reg Address	Bit Field	Type	Setting Name	Description
0x0006	3:0	R	SPECIAL	ClockBuilder Pro version that was used to generate the NVM image. Major.Minor.Revision.Special
0x0006	7:4	R	REVISION	
0x0007	7:0	R	MINOR	
0x0008	0	R	MINOR	
0x0008	4:1	R	MAJOR	
0x0008	7:5	R	TOOL	
0x0009	7:0	R	TEMP_GRADE	Device temperature grading 0 = Industrial (-40 °C to 85 °C) ambient conditions.
0x000A	7:0	R	PKG_ID	Package ID 0 = 9x9 mm 64 QFN

Table 14.11. Register 0x000B RSVD

Reg Address	Bit Field	Type	Setting Name	Description
0x000B	6:0	R/W	RSVD	Write 0 and ignore on reads

Table 14.12. Register 0x000C Internal Status Bits

Reg Address	Bit Field	Type	Setting Name	Description
0x000C	0	R	SYSINCAL	1 if the device is calibrating.
0x000C	1	R	LOSXAXB	1 if there is no signal at the XAXB pins.
0x000C	3	R	LOLIL_ERR	1 if there is a problem locking to the XAXB input signal.
0x000C	5	R	SMBUS_TIMEOUT	1 if there is a timeout error.
0x000C	7:6	R	LOS_CMOS	01 is a LOS on IN3 10 is a LOS on IN4 11 is a LOS on IN3 and IN4

Bit 1 is the LOS status monitor for the XTAL at the XA/XB pins. Bit 3 is the XAXB problem status monitor and may indicate the XAXB input signal has excessive jitter, ringing, or low amplitude.

Table 14.13. Register 0x000D Loss-of Signal (LOS) Alarms

Reg Address	Bit Field	Type	Setting Name	Description
0x000D	3:0	R	LOS	1 if the clock input [Ref 2 1 0] is currently LOS.
0x000D	7:4	R	OOF	1 if the clock input [Ref, 2 1 0] is currently OOF.

Note that each bit corresponds to the input. The LOS bits are not sticky.

- Input 0 (IN0) corresponds to LOS 0x000D [0], OOF 0x000D[4]
- Input 1 (IN1) corresponds to LOS 0x000D [1], OOF 0x000D[5]
- Input 2 (IN2) corresponds to LOS 0x000D [2], OOF 0x000D[6]
- Reference Input (REF) corresponds to LOS 0x000D [3], OOF 0x000D[7]

Table 14.14. Register 0x000E Holdover and LOL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000E	3:0	R	LOL_PLL[D:A]	1 if the DSPLL is out of lock.
0x000E	7:4	R	HOLD_PLL[D:A]	1 if the DSPLL is in holdover (or free run).

DSPLL_A corresponds to bit 0,4.

DSPLL_B (Reference) corresponds to bit 1,5.

DSPLL_C corresponds to bit 2,6.

DSPLL_D corresponds to bit 3,7 in Standard Input mode.

Table 14.15. Register 0x000F INCAL Status

Reg Address	Bit Field	Type	Setting Name	Description
0x000F	7:4	R	CAL_PLL[D:A]	1 if the DSPLL internal calibration is busy.

DSPLL_A corresponds to bit 4.

DSPLL_B (Reference) corresponds to bit 5.

DSPLL_C corresponds to bit 6.

DSPLL_D corresponds to bit 7.

Table 14.16. Register 0x0011 Internal Error Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0011	0	R/W	SYSINCAL_FLG	Sticky version of SYSINCAL. Write a 0 to this bit to clear.
0x0011	1	R/W	LOSXAXB_FLG	Sticky version of LOSXAXB. Write a 0 to this bit to clear.
0x0011	3	R/W	XAXB_ERR_FLG	Sticky version of XAXB_ERR. Write a 0 to this bit to clear.
0x0011	5	R/W	SMBUS_TIME-OUT_FLG	Sticky version of SMBUS_TIME-OUT. Write a 0 to this bit to clear.
0x0011	7:6	R/W	LOS_CMOS_CK_FLG	01 LOS has been detected on IN3 in the past. 10 LOS has been detected on IN4 in the past.

These are sticky flag versions of 0x000C. They are cleared by writing zero to the bit that has been set.

Table 14.17. Register 0x0012 Sticky OOF and LOS Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0012	3:0	R/W	LOS_FLG	Sticky version of LOS. Write a 0 to this bit to clear.
0x0012	7:4	R/W	OOF_FLG	Sticky version of OOF. Write a 0 to this bit to clear.

These are sticky flag versions of 0x000D.

- Input 0 (IN0) corresponds to LOS_FLG 0x0012 [0], OOF_FLG 0x0012[4].
- Input 1 (IN1) corresponds to LOS_FLG 0x0012 [1], OOF_FLG 0x0012[5].
- Input 2 (IN2) corresponds to LOS_FLG 0x0012 [2], OOF_FLG 0x0012[6].
- Reference (REF) corresponds to LOS_FLG 0x0012 [3].

Table 14.18. Register 0x0013 Holdover and LOL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0013	3:0	R/W	LOL_FLG_PLL[D:A]	1 if the DSPLL was unlocked.
0x0013	7:4	R/W	HOLD_FLG_PLL[D:A]	1 if the DSPLL was in holdover (or freerun).

Sticky flag versions of address 0x000E.

- DSPLL_A corresponds to bit 0,4.
- DSPLL_B (Reference) corresponds to bit 1,5.
- DSPLL_C corresponds to bit 2,6.
- DSPLL_D corresponds to bit 3,7 when in Standard Input mode.

Table 14.19. Register 0x0014 INCAL Flags

Reg Address	Bit Field	Type	Setting Name	Description
0x0014	7:4	R/W	CAL_FLG_PLL[D:A]	1 if the DSPLL internal calibration was busy.

Table 14.20. Register 0x0016 LOL_ON_HOLD_PLLA/B/C/D

Reg Address	Bit Field	Type	Setting Name	Description
0x0016	0	R/W	LOL_ON_HOLD_PLLA	0: There is no LOL trigger on HO/FR or loop is not used. 1: Trigger a LOL when loop enters holdover/free-run.
0x0016	1	R/W	LOL_ON_HOLD_PLLB	
0x0016	2	R/W	LOL_ON_HOLD_PLLC	
0x0016	3	R/W	LOL_ON_HOLD_PLLD	

Note:

1. Trigger LOL when the PLLn enters holdover/free-run

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5383A-B12345-GM.

Applies to a factory pre-programmed OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.

Si5383A-B-GM.

Applies to a "base" or "blank" OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5383 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro.

These are sticky-flag versions of 0x000F.

DSPLL A corresponds to bit 4

DSPLL B (Reference) corresponds to bit 5

DSPLL C corresponds to bit 6

DSPLL D corresponds to bit 7

Table 14.21. Register 0x0017 Fault Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0017	0	R/W	SYSIN-CAL_INTR_MSK	1 to mask SYSINCAL_FLG from causing an interrupt.
0x0017	1	R/W	LOS-XAXB_INTR_MSK	1 to mask the LOSXAXB_FLG from causing an interrupt.
0x0017	5	R/W	SMB_TMOUT_INTR_MSK	1 to mask SMBUS_TIMOUT_FLG from causing an interrupt.
0x0017	7:6	R/W	INTR_LOS_CMOS_CK_MSK	1 to mask the INTR_LOS_CMOS_CK_MSK from causing an interrupt.

The interrupt mask bits for the fault flags in register 0x011. If the mask bit is set, the alarm will be blocked from causing an interrupt. The default for this trigger is 0x035.

Table 14.22. Register 0x0018 OOF and LOS Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0018	3:0	R/W	LOS_INTR_MSK	1: To mask the clock input LOS flag.
0x0018	7:4	R/W	OOF_INTR_MSK	1: For PPS inputs and to mask the OOF flag

- Input 0 (IN0) corresponds to LOS_IN_INTR_MSK 0x0018[0], OOF_IN_INTR_MSK 0x0018[4]
- Input 1 (IN1) corresponds to LOS_IN_INTR_MSK 0x0018[1], OOF_IN_INTR_MSK 0x0018[5]
- Input 2 (IN2) corresponds to LOS_IN_INTR_MSK 0x0018[2], OOF_IN_INTR_MSK 0x0018[6]
- Reference (REF) corresponds to LOS_IN_INTR_MSK 0x0018[3]

These are the interrupt mask bits for the OOF and LOS flags in register 0x0012. If a mask bit is set, the alarm will be blocked from causing an interrupt. The OOF is not supported on PPS inputs

Table 14.23. Register 0x0019 Holdover and LOL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	3:0	R/W	LOL_INTR_MSK_PLL[D:A]	1: To mask the clock input LOL flag.

Reg Address	Bit Field	Type	Setting Name	Description
0x0019	7:4	R/W	HOLD_INTR_MSK_PLL[D:A]	1: To mask the holdover flag.

- DSPLL A corresponds to LOL_INTR_MSK_PLL 0x0019[0], HOLD_INTR_MSK_PLL 0x0019[4]
- DSPLL B (Reference) corresponds to LOL_INTR_MSK_PLL 0x0019[1]
- DSPLL C corresponds to LOL_INTR_MSK_PLL 0x0019[2], HOLD_INTR_MSK_PLL 0x0019[6]
- DSPLL D corresponds to LOL_INTR_MSK_PLL 0x0019[3], HOLD_INTR_MSK_PLL 0x0019[7], Standard Input mode.

These are the interrupt mask bits for the LOL and HOLD flags in register 0x0013. If a mask bit is set, the alarm will be blocked from causing an interrupt.

Table 14.24. Register 0x001A INCAL Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x001A	7:4	R/W	CAL_INTR_MSK_DSPLL[D:A]	1: To mask the DSPLL internal calibration busy flag.

DSPLL A corresponds to bit 0

DSPLL B (Reference) corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3

Table 14.25. Register 0x001C Soft Reset and Calibration

Reg Address	Bit Field	Type	Setting Name	Description
0x001C	0	S	SOFT_RST_ALL	0: No effect. 1: Initialize and calibrate the entire device. This will also align the outputs from the four DSPLLs.
0x001C[1]	1	S	SOFT_RST_PLLA	1 initialize and calibrate DSPLLA.
0x001C	2	S	SOFT_RST_PLLB	1 initialize and calibrate DSPLLB (Reference).
0x001C[1]	3	S	SOFT_RST_PLLC	1 initialize and calibrate DSPLLC.
0x001C	4	S	SOFT_RST_PLLD	1 initialize and calibrate DSPLLD.

Note:
1. Si5383 only.

These bits are of type “S”, which means self-clearing. Unlike SOFT_RST_ALL, the SOFT_RST_PLLx bits do not update the loop BW values. If these have changed, the update can be done by writing to BW_UPDATE_PLLA, BW_UPDATE_PLLB, BW_UPDATE_PLLC, and BW_UPDATE_PLLD at addresses 0x0414, 0x514, 0x0614, and 0x0715. Note that unlike the other SOFT_RST_PLLx bits, a SOFT_RST_PLL_B will affect all of the DSPLLs.

Table 14.26. Register 0x001D FINC, FDEC

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	0	S	FINC	0: No effect 1: A rising edge will cause an frequency increment.

Reg Address	Bit Field	Type	Setting Name	Description
0x001D	1	S	FDEC	0: No effect 1: A rising edge will cause an frequency decrement.

FINC and FDEC will affect the M dividers depending on how their corresponding M_FSTEP_MSK_PLLx bits are programmed.

Table 14.27. Register 0x001E Sync

Reg Address	Bit Field	Type	Setting Name	Description
0x001E	2	S	SYNC	Resets all output R dividers to the same state.

Table 14.28. Register 0x002B RSVD

Reg Address	Bit Field	Type	Setting Name	Description
0x002B	3	R/W	RSVD	Write 0 and ignore on reads

Table 14.29. Register 0x002C LOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x002C	3:0	R/W	LOS_EN	0: For disable. 1: To enable LOS for a clock input.
0x002C	4	R/W	LOSXAXB_DIS	0: For disable. 1: To enable LOS for the XAXB input.

- Input 0 (IN0): LOS_EN[0]
- Input 1 (IN1): LOS_EN[1]
- Input 2 (IN2): LOS_EN[2]
- Reference (REF): LOS_EN[3]

Table 14.30. Register 0x002D Loss of Signal Re-Qualification Value

Reg Address	Bit Field	Type	Setting Name	Description
0x002D	1:0	R/W	LOS0_VAL_TIME	Clock Input 0 0: For 2 msec. 1: For 100 msec. 2: For 200 msec. 3: For one second.
0x002D	3:2	R/W	LOS1_VAL_TIME	Clock Input 1, same as above.
0x002D	5:4	R/W	LOS2_VAL_TIME	Clock Input 2, same as above.
0x002D	7:6	R/W	LOS3_VAL_TIME	Reference Clock, same as above.

When an input clock is gone (and therefore has an active LOS alarm), if the clock returns, there is a period of time that the clock must be within the acceptable range before the alarm is removed. This is the LOS_VAL_TIME.

Table 14.31. Register 0x002E-0x002F LOS0 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x002E	7:0	R/W	LOS0_TRG_THR	Calculated by CBPro.
0x002F	15:8	R/W	LOS0_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 0, given a particular frequency plan.

Table 14.32. Register 0x0030-0x0031 LOS1 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0030	7:0	R/W	LOS1_TRG_THR	Calculated by CBPro.
0x0031	15:8	R/W	LOS1_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 1, given a particular frequency plan.

Table 14.33. Register 0x0032-0x0033 LOS2 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0032	7:0	R/W	LOS2_TRG_THR	Calculated by CBPro
0x0033	15:8	R/W	LOS2_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for Input 2, given a particular frequency plan.

Table 14.34. Register 0x0034-0x0035 LOS3 Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0034	7:0	R/W	LOS3_TRG_THR	Calculated by CBPro.
0x0035	15:8	R/W	LOS3_TRG_THR	

ClockBuilder Pro calculates the correct LOS register threshold trigger value for the Reference given a particular frequency plan.

Table 14.35. Register 0x0036-0x0037 LOS0 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0036	7:0	R/W	LOS0_CLR_THR	Calculated by CBPro.
0x0037	15:8	R/W	LOS0_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 0, given a particular frequency plan.

Table 14.36. Register 0x0038-0x0039 LOS1 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0038	7:0	R/W	LOS1_CLR_THR	Calculated by CBPro.
0x0039	15:8	R/W	LOS1_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 1, given a particular frequency plan.

Table 14.37. Register 0x003A-0x003B LOS2 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003A	7:0	R/W	LOS2_CLR_THR	Calculated by CBPro.
0x003B	15:8	R/W	LOS2_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for Input 2, given a particular frequency plan.

Table 14.38. Register 0x003C-0x003D LOS3 Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x003C	7:0	R/W	LOS3_CLR_THR	Calculated by CBPro.
0x003D	15:8	R/W	LOS3_CLR_THR	

ClockBuilder Pro calculates the correct LOS register clear threshold value for the Reference, given a particular frequency plan.

Table 14.39. Register 0x0B47 Digital OOF, User Disable.

Reg Address	Bit Field	Type	Setting Name	Description
0x003E	3:0	R/W	LOS_EN_1HZ	Enables LOS detection for a 1PPS input. 0: Disabled 1: Enabled

Table 14.40. Register 0x003F OOF Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x003F	3:0	R/W	OOF_EN	0: To disable.
0x003F	6:4	R/W	FAST_OOF_EN	1: To enable.

Table 14.41. Register 0x0040 OOF Reference Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0040	2:0	R/W	OOF_REF_SEL	3: Reference

Table 14.42. 0x0041-0x0045 OOF Divider Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0041	4:0	R/W	OOF0_DIV_SEL	Sets a divider for the OOF circuitry for each input clock 0,1,2,3. The divider value is $2^{OOFx\_DIV\_SEL}$. CBPro sets these dividers.
0x0042	4:0	R/W	OOF1_DIV_SEL	
0x0043	4:0	R/W	OOF2_DIV_SEL	
0x0044	4:0	R/W	OOF3_DIV_SEL	
0x0045	4:0	R/W	OOFXO_DIV_SEL	

Table 14.43. Register 0x0046-0x0049 Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0046	7:0	R/W	OOF0_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0047	7:0	R/W	OOF1_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0048	7:0	R/W	OOF2_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x0049	7:0	R/W	OOF3_SET_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm set threshold for Reference, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm.

Table 14.44. Register0x004A-0x004D Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x004A	7:0	R/W	OOF0_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004B	7:0	R/W	OOF1_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

Reg Address	Bit Field	Type	Setting Name	Description
0x004C	7:0	R/W	OOF2_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm
0x004D	7:0	R/W	OOF3_CLR_THR	1 = 2 ppm 2 = 4 ppm 3 = 6 ppm ... 255 = 510 ppm

These registers determine the OOF alarm clear threshold for the reference, IN2, IN1 and IN0. The range is from ±2 ppm up to ±510 ppm in steps of 2 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 14.45. 0x004E-0x004F OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x004E	2:0	R/W	OOF0_DETWIN_SEL	Calculated by CBPro.
0x004E	6:4	R/W	OOF1_DETWIN_SEL	
0x004F	2:0	R/W	OOF2_DETWIN_SEL	
0x004F	6:4	R/W	OOF3_DETWIN_SEL	

Table 14.46. Register 0x0051-0x0054 Fast Out of Frequency Set Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0051	3:0	R/W	FAST_OOF0_SET_THR	(1+ value) x 1000 ppm
0x0052	3:0	R/W	FAST_OOF1_SET_THR	(1+ value) x 1000 ppm
0x0053	3:0	R/W	FAST_OOF2_SET_THR	(1+ value) x 1000 ppm
0x0054	3:0	R/W	FAST_OOF3_SET_THR	(1+ value) x 1000 ppm

These registers determine the OOF alarm set threshold for the reference, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

Table 14.47. Register 0x0055-0x0058 Fast Out of Frequency Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x0055	3:0	R/W	FAST_OOF0_CLR_THR	(1+ value) x 1000 ppm
0x0056	3:0	R/W	FAST_OOF1_CLR_THR	(1+ value) x 1000 ppm

Reg Address	Bit Field	Type	Setting Name	Description
0x0057	3:0	R/W	FAST_OOF2_CLR_THR	(1+ value) x 1000 ppm
0x0058	3:0	R/W	FAST_OOF2_CLR_THR	(1+value) x 1000 ppm

Table 14.48. 0x0059 Fast OOF Detection Windows

Reg Address	Bit Field	Type	Setting Name	Description
0x0059	2:0	R/W	FAST_OOF0_DET-WIN_SEL	Calcultated by CBPro.
0x0059	3:2	R/W	FAST_OOF1_DET-WIN_SEL	
0x0059	5:4	R/W	FAST_OOF2_DET-WIN_SEL	
0x0059	7:6	R/W	FAST_OOF3_DET-WIN_SEL	

Table 14.49. 0x005A-0x005D OOF0 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005A	7:0	R/W	OOF0_RATIO_REF	Calculated by CBPro.
0x005B	15:8	R/W	OOF0_RATIO_REF	
0x005C	23:16	R/W	OOF0_RATIO_REF	
0x005D	25:24	R/W	OOF0_RATIO_REF	

Table 14.50. 0x005E-0x0061 OOF1 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x005E	7:0	R/W	OOF1_RATIO_REF	Calculated by CBPro.
0x005F	15:8	R/W	OOF1_RATIO_REF	
0x0060	23:16	R/W	OOF1_RATIO_REF	
0x0061	25:24	R/W	OOF1_RATIO_REF	

Table 14.51. 0x0062-0x0065 OOF2 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0062	7:0	R/W	OOF2_RATIO_REF	Calculated by CBPro.
0x0063	15:8	R/W	OOF2_RATIO_REF	
0x0064	23:16	R/W	OOF2_RATIO_REF	
0x0065	25:24	R/W	OOF2_RATIO_REF	

Table 14.52. 0x0066-0x0069 OOF3 Ratio for Reference

Reg Address	Bit Field	Type	Setting Name	Description
0x0066	7:0	R/W	OOF3_RATIO_REF	Calculated by CBPro.
0x0067	15:8	R/W	OOF3_RATIO_REF	
0x0068	23:16	R/W	OOF3_RATIO_REF	
0x0069	25:24	R/W	OOF3_RATIO_REF	

Table 14.53. Register 0x0092 LOL_FST_EN_PLLA/B/C/D

Reg Address	Bit Field	Type	Setting Name	Description
0x0092	0	R/W	LOL_FST_EN_PLLA	0: Disable 1: Enable
0x0092	1	R/W	LOL_FST_EN_PLLB	
0x0092	2	R/W	LOL_FST_EN_PLLC	
0x0092	3	R/W	LOL_FST_EN_PLLD	

Note:

1. Enables fast LOL detect. A large input frequency error will quickly assert LOL when this is enabled.

Table 14.54. Register 0x0093-0x0094 Fast LOL Detection Window

Reg Address	Bit Field	Type	Setting Name	Description
0x0093	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLA	Calcuated by CBPro.
0x0093	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLB	
0x0094	3:0	R/W	LOL_FST_DET-WIN_SEL_PLLC	
0x0094	7:4	R/W	LOL_FST_DET-WIN_SEL_PLLD	

Note:

1. Selects the measurement time in a fast LOL detection window.

These registers determine the OOF alarm clear threshold for the reference, IN2, IN1 and IN0 when the fast control is enabled. The value in each of the register is (1+ value) x 1000 ppm. ClockBuilder Pro is used to determine the values for these registers.

OOF needs a frequency reference. ClockBuilder Pro provides the OOF register values for a particular frequency plan.

Table 14.55. Register 0x0095 Fast LOL Detectection Value Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0095[1]	1:0	R/W	LOL_FST_VAL-WIN_SELL_PLLA	Selection for number of detection windows in a fast LOLA validation window 0: 1 1: 16 2:128 3: 1024
0x0095	3:2	R/W	LOL_FST_VAL-WIN_SELL_PLLB	
0x0095[1]	5:4	R/W	LOL_FST_VAL-WIN_SELL_PLLC	
0x0095	7:6	R/W	LOL_FST_VAL-WIN_SELL_PLLD *(Standard Input mode)*	

Note:
1. Si5383 only.

Table 14.56. Register 0x0096-0x0097 Fast LOL Set Threshold Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0096[1]	3:0	R/W	LOL_FST_SET_THR_SEL (PLLA)	0: 0.2 ppm 1: 0.6 ppm 2: 2 ppm 3: 6 ppm 4: 20 ppm 5: 60 ppm 6: 200 ppm 7: 600 ppm 8: 2000 ppm 9: 6000 ppm 10: 20000 ppm
0x0096	7:4	R/W	LOL_FST_SET_THR_SEL (PLLB)	
0x0097[1]	3:0	R/W	LOL_FST_SET_THR_SEL (PLLC)	
0x0097	7:4	R/W	LOL_FST_SET_THR_SEL (PLLD) *(Standard Input mode)*	

Note:
1. Si5383 only.

Table 14.57. Register 0x0098-0x0099 Fast LOL Clear Threshold Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x0098[1]	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLA	0: 0.2 ppm 1: 0.6 ppm 2: 2 ppm 3: 6 ppm 4: 20 ppm 5: 60 ppm 6: 200 ppm 7: 600 ppm 8: 2000 ppm 9: 6000 ppm 10: 20000 ppm
0x0098	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLB	
0x0099[1]	3:0	R/W	LOL_FST_CLR_THR_SEL_PLLC	
0x0099	7:4	R/W	LOL_FST_CLR_THR_SEL_PLLD *(Standard Input mode)*	

Note:
1. Si5383

Table 14.58. Register 0x009A LOL Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x009A	3:0	R/W	LOL_SLW_EN_PLL[D:A]	0: To disable LOL. 1: To enable LOL.

Table 14.59. Register 0x009B-0x009C Slow LOL Detection Value

Reg Address	Bit Field	Type	Setting Name	Description
0x009B	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Calcuated by CBPro.
0x009B	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLB	
0x009C	3:0	R/W	LOL_SLW_DET-WIN_SEL_PLLC	
0x009C	7:4	R/W	LOL_SLW_DET-WIN_SEL_PLLD	

Note:
1. Selects the measurement time in a slow LOL detection window.

Table 14.60. Register 0x009D LOL_SLW_DETWIN_SEL_PLLA/B/C/D

Reg Address	Bit Field	Type	Setting Name	Description
0x009D	1:0	R/W	LOL_SLW_DET-WIN_SEL_PLLA	Selection for number of detection windows in a slow LOLA validation window 00: 1 01: 16 10: 128 11: 1024
0x009D	3:2	R/W	LOL_SLW_DET-WIN_SEL_PLLB	
0x009D	5:4	R/W	LOL_SLW_DET-WIN_SEL_PLLC	
0x009D	7:6	R/W	LOL_SLW_DET-WIN_SEL_PLLD	

Note:
1. Selection for number of detection windows in a slow LOL validation window.

DSPLL A corresponds to bit 0

DSPLL B (Reference) corresponds to bit 1

DSPLL C corresponds to bit 2

DSPLL D corresponds to bit 3 when operating in Standard Input mode

ClockBuilder Pro provides the LOL register values for a particular frequency plan.

Table 14.61. Register 0x009E LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009E[1]	3:0	R/W	LOL_SLW_SET_THR_PLLA	Configures the loss of lock set thresholds. Selectable as 1, 3, 10,30,100,300,1000,3000,10000. Values are in ppm.
0x009E	7:4	R/W	LOL_SLW_SET_THR_PLLB	Configures the loss of lock set thresholds. Selectable as 1, 3, 10,30,100,300,1000,3000,10000. Values are in ppm.

Note:
1. Si5383 only.

Table 14.62. Register 0x009F LOL Set Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x009F[1]	3:0	R/W	LOL_SLW_SET_THR_PLLC	Configures the loss of lock set thresholds. Selectable as 1, 3, 10,30,100,300,1000,3000,10000. Values are in ppm.
0x009F	7:4	R/W	LOL_SLW_SET_THR_PLLD *(Standard Input mode)*	Configures the loss of lock set thresholds. Selectable as 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values are in ppm.

Reg Address	Bit Field	Type	Setting Name	Description
Note: 1. Si5383 only.				

The following are the thresholds for the value that is placed in the four bits for DSPLLs.

- 0 = 0.1 ppm
- 1 = 0.3 ppm
- 2 = 1 ppm
- 3 = 3 ppm
- 4 = 10 ppm
- 5 = 30 ppm
- 6 = 100 ppm
- 7 = 300 ppm
- 8 = 1000 ppm
- 9 = 3000 ppm
- 10 = 10000 ppm

Table 14.63. Register 0x00A0 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A0[1]	3:0	R/W	LOL_SLW_CLR_THR_PLLA	Configures the loss of lock clear thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000. Values in ppm.
0x00A0	7:4	R/W	LOL_SLW_CLR_THR_PLLB	Configures the loss of lock clear thresholds for the reference. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000. Values in ppm.
Note: 1. Si5383 only.				

Table 14.64. Register 0x00A1 LOL Clear Thresholds

Reg Address	Bit Field	Type	Setting Name	Description
0x00A1[1]	3:0	R/W	LOL_SLW_CLR_THR_PLLC	Configures the loss of lock clear thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000, 3000, 10000. Values in ppm.
0x00A1	7:4	R/W	LOL_SLW_CLR_THR_PLLD *(Standard Input mode)*	Configures the loss of lock clear thresholds. Selectable as 0.1, 0.3, 1, 3, 10, 30, 100, 300, 1000. Values in ppm.
Note: 1. Si5383 only.				

The following are the thresholds for the value that is placed in the four bits for DSPLLs. ClockBuilder Pro sets these values.

- 0=0.1 ppm
- 1=0.3 ppm
- 2=1 ppm
- 3=3 ppm
- 4=10 ppm
- 5=30 ppm
- 6=100 ppm
- 7=300 ppm
- 8=1000 ppm
- 9=3000 ppm
- 10=10000 ppm

Table 14.65. Register 0x00A2 LOL Timer Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x00A2	3:0	R/W	LOL_TIMER_EN_PLL	0: To disable. 1: To enable.

LOL_TIMER extends the time after the LOL clear threshold has been met that LOL stays active.

DSPLL A bit 0

DSPLL B (Reference) bit 1

DSPLL C bit 2

DSPLL D bit 3 when operating in Standard Input mode

Table 14.66. Register 0x00A4-0x00A7 LOL Clear Delay DSPLL A[1]

Reg Address	Bit Field	Type	Setting Name	Description
0x00A4	7:0	R/W	LOL_CLR_DELAY_PLLA	Calculated by CBPro.
0x00A5	15:8	R/W	LOL_CLR_DELAY_PLLA	
0x00A6	23:16	R/W	LOL_CLR_DELAY_PLLA	
0x00A7	28:24	R/W	LOL_CLR_DELAY_PLLA	

Note:
1. Si5383 only.

Table 14.67. Register 0x00A9-0x00AC LOL Clear Delay DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x00A9	7:0	R/W	LOL_CLR_DE-LAY_PLLB	Calculated by CBPro..
0x00AA	15:8	R/W	LOL_CLR_DE-LAY_PLLB	
0x00AB	23:16	R/W	LOL_CLR_DE-LAY_PLLB	
0x00AC	28:24	R/W	LOL_CLR_DE-LAY_PLLB	

Table 14.68. Register 0x00AE-0x00B1 LOL Clear Delay DSPLL C[1]

Reg Address	Bit Field	Type	Setting Name	Description
0x00AE	7:0	R/W	LOL_CLR_DE-LAY_PLLC	Calcutated by CBPro.
0x00AF	13:8	R/W	LOL_CLR_DE-LAY_PLLC	
0x00B0	23:14	R/W	LOL_CLR_DE-LAY_PLLC	
0x00B1	28:24	R/W	LOL_CLR_DE-LAY_PLLC	

Note:
1. Si5383 only.

Table 14.69. Register 0x00B3-0x00B6 LOL Clear Delay DSPLL D[1]

Reg Address	Bit Field	Type	Setting Name	Description
0x00B3	7:0	R/W	LOL_CLR_DE-LAY_PLLD	Calculated by CBPro.
0x00B4	13:8	R/W	LOL_CLR_DE-LAY_PLLD	
0x00B5	23:14	R/W	LOL_CLR_DE-LAY_PLLD	
0x00B6	28:24	R/W	LOL_CLR_DE-LAY_PLLD	

Note:
1. Standard Input Mode Only

Table 14.70. Register 0x00E5 FASTLOCK_EXTEND_EN_PLLA/B/C/D

Reg Address	Bit Field	Type	Setting Name	Description
0x00E5	0	R/W	FASTLOCK_EXTEND_EN_PLLA	0: Do not extend Fastlock period 1: Extend Fastlock period
0x00E5	1	R/W	FASTLOCK_EXTEND_EN_PLLB	
0x00E5	2	R/W	FASTLOCK_EXTEND_EN_PLLC	
0x00E5	3	R/W	FASTLOCK_EXTEND_EN_PLLD	

Note:
1. Enables Fastlock extension past LOL clear period.

Table 14.71. Registers 0x00E6-0x00F5 FASTLOCK_EXTEND_PLLn

Reg Address	Bit Field	Type	Setting Name	Description
0x00E6	7:0	R/W	FASTLOCK_EXTEND_PLLA	Calcuated by CBPro.
x00E7	15:8			
0x00E8	23:16			
0x00E9	28:24			
0x00EA	7:0	R/W	FASTLOCK_EXTEND_PLLB	Calcuated by CBPro.
0x00EB	15:8			
0x00EC	23:16			
0x00ED	28:24			
0x00EE	7:0	R/W	FASTLOCK_EXTEND_PLLC	Calcuated by CBPro.
0x00EF	15:8			
0x00F0	23:16			
0x00F1	28:24			
0x00F2	7:0	R/W	FASTLOCK_EXTEND_PLLD	Calcuated by CBPro.
0x00F3	15:8			
0x00F4	23:16			
0x00F5	28:24			

Note:
1. Extension length added to fast-lock timer value.

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Table 14.72. Register 0x0102 Global OE Gating for all Clock Output Drivers

Reg Address	Bit Field	Type	Setting Name	Description
0x0102	0	R/W	OUTALL_DISABLE_LOW	0: Disables all output drivers. 1: Pass through the output enables.

Table 14.73. Register 0x0130 OUT6_CASCADE_EN

Reg Address	Bit Field	Type	Setting Name	Description
0x0130	4	R/W	OUT6_CASCADE_EN	0: Disabled 1: Enabled

Note:
1. Enables cascading OUT6 to OUT5, for 1PPS outputs.

Table 14.74. Register 0x0102, 0x0112, 0x0117, 0x011C, 0x0126, 0x012B, 0x0130

Reg Address	Bit Field	Type	Setting Name	Description
0x010D	0	R/W	OUT0_PDN	0: To power up the regulator. 1: To power down the regulator. Clock outputs will be weakly pulled-low.
0x0112			OUT1_PDN	
0x0117			OUT2_PDN	
0x011C			OUT3_PDN	
0x0126			OUT4_PDN	
0x012B			OUT5_PDN	
0x0130			OUT6_PDN	
0x010D	1	R/W	OUT0_OE	0: To disable the output. 1: To enable the output.
0x0112			OUT1_OE	
0x0117			OUT2_OE	
0x011C			OUT3_OE	
0x0126			OUT4_OE	
0x012B			OUT5_OE	
0x0130			OUT6_OE	

Reg Address	Bit Field	Type	Setting Name	Description
0x010D	2	R/W	OUT0_RDIV_FORCE	Force Rx output divider divide-by-2. 0: Rx_REG sets divide value (default) 1: Divide value forced to divide-by-2 ClockBuilder Pro sets this bit automatically when Rx = 2.
0x0112			OUT1_RDIV_FORCE	
0x0117			OUT2_RDIV_FORCE	
0x011C			OUT3_RDIV_FORCE	
0x0126			OUT4_RDIV_FORCE	
0x012B			OUT5_RDIV_FORCE	
0x0130			OUT6_RDIV_FORCE	

The output drivers are all identical. See Section 6.2 Performance Guidelines for Outputs.

Table 14.75. Register 0x010E, 0x0113, 0x0118, 0x011D, 0x0127, 0x012C, 0x0131 Output Format

Reg Address	Bit Field	Type	Setting Name	Description
0x010E	2:0	R/W	OUT0_FORMAT	0: Reserved. 1: Differential Normal mode. 2: Differential Low-Power mode. 3: Reserved. 4: LVCMOS single ended. 5-7: Reserved.
0x0113			OUT1_FORMAT	
0x0118			OUT2_FORMAT	
0x011D			OUT3_FORMAT	
0x0127			OUT4_FORMAT	
0x012C			OUT5_FORMAT	
0x0131			OUT6_FORMAT	
0x010E	3	R/W	OUT0_SYNC_EN	0: Disable. 1: Enable.
0x0113			OUT1_SYNC_EN	
0x0118			OUT2_SYNC_EN	
0x011D			OUT3_SYNC_EN	
0x0127			OUT4_SYNC_EN	
0x012C			OUT5_SYNC_EN	
0x0131			OUT6_SYNC_EN	
0x010E	5:4	R/W	OUT0_DIS_STATE	Determines the state of an output driver when disabled, selectable as: 0: Disable low. 1: Disable high.
0x0113			OUT1_DIS_STATE	
0x0118			OUT2_DIS_STATE	
0x011D			OUT3_DIS_STATE	
0x0127			OUT4_DIS_STATE	
0x012C			OUT5_DIS_STATE	
0x0131			OUT6_DIS_STATE	

Reg Address	Bit Field	Type	Setting Name	Description
0x010E	7:6	R/W	OUT0_CMOS_DRV	LVCMOS output impedance drive strength see the table titled LVCMOS Drive Strength Control Registers in Section 6.4.2 LVCMOS Output Impedance and Drive Strength Selection.
0x0113			OUT1_CMOS_DRV	
0x0118			OUT2_CMOS_DRV	
0x011D			OUT3_CMOS_DRV	
0x0127			OUT4_CMOS_DRV	
0x012C			OUT5_CMOS_DRV	
0x0131			OUT6_CMOS_DRV	

The output drivers are all identical.

Table 14.76. Register 0x0010F, 0x0114, 0x0119, 0x011E, 0x0128, 0x012D, 0x0132 Output

Reg Address	Bit Field	Type	Setting Name	Description
0x010F	3:0	R/W	OUT0_CM	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 48.
0x0114			OUT1_CM	
0x0119			OUT2_CM	
0x011E			OUT3_CM	
0x0128			OUT4_CM	
0x012D			OUT5_CM	
0x0132			OUT6_CM	
0x010F	6:4	R/W	OUT0_AMPL	OUTx common-mode voltage selection. This field only applies when OUTx_FORMAT = 1 or 2. See Table 6.6 Recommended Settings for Differential LVDS, LVPECL, HCSL, and CML on page 48.
0x0114			OUT1_AMPL	
0x0119			OUT2_AMPL	
0x011E			OUT3_AMPL	
0x0128			OUT4_AMPL	
0x012D			OUT5_AMPL	
0x0131			OUT6_AMPL	

ClockBuilder Pro is used to select the correct settings for this register. The output drivers are all identical.

Table 14.77. Register 0x0110, 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133 R-Divider Mux

Reg Address	Bit Field	Type	Setting Name	Description
0x0110	2:0	R/W	OUT0_MUX_SEL	Output driver 0 input mux select.This selects the source of the output clock. 0: DSPLL A 1: Reserved 2: DSPLL C 3: DSPLL D
0x0115			OUT1_MUX_SEL	
0x011A			OUT2_MUX_SEL	
0x011F			OUT3_MUX_SEL	
0x0129			OUT4_MUX_SEL	
0x012E			OUT5_MUX_SEL	
0x0133			OUT6_MUX_SEL	

Reg Address	Bit Field	Type	Setting Name	Description
0x0110 0x0115 0x011A 0x011F 0x0129 0x012E 0x0133	7:6	R/W	OUT0_INV OUT1_INV OUT2_INV OUT3_INV OUT4_INV OUT5_INV OUT6_INV	0: neither CLK nor CLKb are inverted 1: CLK is inverted 2: CLK and CLKb are inverted 3: CLK inverted These bits have no effect on differential outputs.

Table 14.78. Register 0x0111-0x013F OUTn_DISC_SRC

Reg Address	Bit Field	Type	Setting Name	Description
0x0111	2:0	R/W	OUT0_DIS_SRC	Squelch during reset selection 000: Not associated with any DSPLL 001: DSPLLA 010: DSPLLB 011: DSPLLC 100: DSPLLD
0x0116	2:0	R/W	OUT1_DIS_SRC	
0x011B	2:0	R/W	OUT2_DIS_SRC	
0x0120	2:0	R/W	OUT3_DIS_SRC	
0x012A	2:0	R/W	OUT4_DIS_SRC	
0x012F	2:0	R/W	OUT5_DIS_SRC	
0x013F	2:0	R/W	OUT6_DIS_SRC	

Note:
1. Used to squelch outputs according DSPLLA/B/C/D association.

Each output can be connected to any of the four DSPLLs using the OUTx_MUX_SEL. The output drivers are all identical.

Table 14.79. Register 0x0110, 0x0115, 0x011A, 0x011F, 0x0129, 0x012E, 0x0133 OUTx VDD Selection and Voltage Setting

Reg Address	Bit Field	Type	Setting Name	Descrption
0x0110	3	R/W	OUT0_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT0_VDD_SEL
0x0110	5:4	R/W	OUT0_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved
0x011A	3	R/W	OUT1_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT1_VDD_SEL
0x011A	5:4	R/W	OUT1_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved

Reg Address	Bit Field	Type	Setting Name	Descrption
0x011F	3	R/W	OUT2_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT2_VDD_SEL
0x011F	5:4	R/W	OUT2_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved
0x0124	3	R/W	OUT3_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT3_VDD_SEL
0x0124	5:4	R/W	OUT3_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved
0x0129	3	R/W	OUT4_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT4_VDD_SEL
0x0129	5:4	R/W	OUT4_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved
0x012E	3	R/W	OUT5_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT5_VDD_SEL
0x012E	5:4	R/W	OUT5_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11:Reserved
0x0133	3	R/W	OUT6_VDD_SEL_EN	0: Do not set to 0 1: Set to value in OUT6_VDD_SEL
0x0133	5:4	R/W	OUT6_VDD_SEL	00: 3.3V 01: 1.8V 10: 2.5V 11: Reserved

Table 14.80. Register 0x0141 Output Disable Mask for LOS XAXB

Reg Address	Bit Field	Type	Setting Name	Description
0x0141	6	R/W	OUT_DIS_MSK_LOS-XAXB	Determines if outputs are disabled during an LOSXAXB condition. 0: All outputs disabled on LOS-XAXB. 1: All outputs remain enabled during LOSXAXB condition.
0x0141	7	R/W	OUT_DIS_MSK_LOS_PFD	0: Not masked 1: Masked

Table 14.81. Register 0x0142 Output Disable Loss of Lock PLL

Reg Address	Bit Field	Type	Setting Name	Description
0x0142	3:0	R/W	OUT_DIS_MASK_LOL_PLL[D:A]	0: LOL will disable all connected outputs. 1: LOL does not disable any outputs.

- Bit 0 LOL_DSPLL_A mask
- Bit 2 LOL_DSPLL_C mask
- Bit 3 LOL_DSPLL_D mask

Table 14.82. Register 0x0145 Power Down All Outputs

Reg Address	Bit Field	Type	Setting Name	Description
0x0145	0	R/W	OUT_PDN_ALL	0: No effect. 1: All drivers powered down.

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Table 14.83. 0x0206 Pre-scale Reference Divide Ratio

Reg Address	Bit Field	Type	Name	Description
0x0206	1:0	R/W	PXAXB	Sets the prescale divider for the input clock on XAXB.

- 0 = pre-scale value 1
- 1 = pre-scale value 2
- 2 = pre-scale value 4
- 4 = pre-scale value 8

NOTES: This can only be used with external clock sources, not crystals. A reset must be implemented when modifying PXAPB.

Table 14.84. Register 0x0208-0x020D P0 Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0208	7:0	R/W	P0_NUM	Calculated by CBPro.
0x0209	15:8	R/W	P0_NUM	
0x020A	23:16	R/W	P0_NUM	
0x020B	31:24	R/W	P0_NUM	
0x020C	39:32	R/W	P0_NUM	
0x020D	47:40	R/W	P0_NUM	

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Changing Registers while Device in Operation are followed.

Table 14.85. Register 0x020E-0x0211 P0 Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x020E	7:0	R/W	P0_DEN	Calculated by CBPro.
0x020F	15:8	R/W	P0_DEN	
0x0210	23:16	R/W	P0_DEN	
0x0211	31:24	R/W	P0_DEN	

The P1, P2 and P3 divider numerator and denominator follow the same format as P0 described above. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Changing Registers while Device in Operation are followed.

Table 14.86. P1-P3 Divider Registers that Follow P0 Definitions

Register Address	Description	Size	Same as Address
0x0212-0x0217	P1_NUM	48-bit Integer Number	0x0208-0x020D
0x0218-0x021B	P1_DEN	32-bit Integer Number	0x020E-0x0211
0x021C-0x0221	P2_NUM	48-bit Integer Number	0x0208-0x020D
0x0222-0x0225	P2_DEN	32-bit Integer Number	0x020E-0x0211

Register Address	Description	Size	Same as Address
0x0226-0x022B	P3_NUM (Reference)	48-bit Integer Number	0x0208-0x020D
0x022C-0x022F	P3_DEN (Reference)	32-bit Integer Number	0x020E-0x0211

The following set of registers configure the P-dividers corresponding to each of the four input clocks seen in Figure 1. ClockBuilder Pro calculates the correct values for the P-dividers. Note that changing these registers during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Changing Registers while Device in Operation are followed. Note that P3 corresponds to the Reference divider value.

Table 14.87. Register 0x0230 Px_UPDATE

Reg Address	Bit Field	Type	Setting Name	Description
0x0230	0	S	P0_UPDATE	0: No update for P-divider value. 1: Update P-divider value.
0x0230	1	S	P1_UPDATE	
0x0230	2	S	P2_UPDATE	
0x0230	3	S	P3_UPDATE	

Table 14.88. 0x053A Hitless Switching Mode for PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0231	3:0	R/W	P0_FRACN_MODE	Managed by CBPro
0x0231	4	R/W	P0_FRACN_EN	
0x0232	3:0	R/W	P1_FRACN_MODE	
0x0232	4	R/W	P0_FRACN_EN	
0x0233	3:0	R/W	P2_FRACN_MODE	
0x0233	4	R/W	P0_FRACN_EN	
0x0234	3:0	R/W	P3_FRACN_MODE	
0x0234	4	R/W	P0_FRACN_EN	

Note that these controls are not needed when following the guidelines in Section 4.2 Changing Registers while Device in Operation. Specifically, they are not needed when using the global soft reset “SOFT_RST_ALL”. However, these are required when using the individual DSPLL soft reset controls, SOFT_RST_PLLA, SOFT_RST_PLLB, etc., as these do not update the Px_NUM or Px_DEN values. Note that P3 corresponds to the Reference.

Table 14.89. Register 0x0235-0x023A MXAXB Divider Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0235	7:0	R/W	MXAXB_NUM	Calculated CBPro.
0x0236	15:8	R/W	MXAXB_NUM	
0x0237	23:16	R/W	MXAXB_NUM	
0x0238	31:24	R/W	MXAXB_NUM	
0x0239	39:32	R/W	MXAXB_NUM	
0x023A	43:40	R/W	MXAXB_NUM	

Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Changing Registers while Device in Operation are followed.

Table 14.90. Register 0x023B-0x023E MXAXB Divider Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x023B	7:0	R/W	MXAXB_DEN	Calculated by CBPro
0x023C	15:8	R/W	MXAXB_DEN	
0x023D	23:16	R/W	MXAXB_DEN	
0x023E	31:24	R/W	MXAXB_DEN	

The M-divider numerator and denominator are set by ClockBuilder Pro for a given frequency plan. Note that changing this register during operation may cause indefinite loss of lock unless the guidelines in Section 4.2 Changing Registers while Device in Operation are followed.

Table 14.91. Register 0x0240 MXAXB_FSTEP_x

Reg Address	Bit Field	Type	Setting Name	Description
0x0240	0	R/W	MXAXB_FSTEP_MSK	0: FINC/FDEC function Enabled 1: FINC/FDEC function Disabled
0x0240	1	R/W	MXAXB_FSTEP_DEN	0: Modify Numerator 1: Modify Denominator

Note:
1. Enables the FINC and FDEC function and assigns FTEP value to Numerator or Denominator.

Table 14.92. Register 0x0241 MXAXB_FSTEPW

Reg Address	Bit Field	Type	Setting Name	Description
0x0241	7:0	R/W	MXAXB_FSTEPW	Calcuated by CBPro.
0x0241	15:8			
0x0241	23:16			
0x0241	31:24			
0x0241	39:24			
0x0241	43:40			

Note:
1. FINC or FDEC step size value.

Table 14.93. Register 0x024D-0x024F R0 Divider

Reg Address	Bit Field	Type	Setting Name	Description
0x024D	7:0	R/W	R0_REG	Calculated by CBPro. Divide value = (R0_REG+1) x 2 To set R0 = 2, set OUT0_RDIV_FORCE2 = 1 and then the R0_REG value is irrelevant.
0x024E	15:8	R/W	R0_REG	
0x024F	23:16	R/W	R0_REG	

The R dividers are at the output clocks and are purely integer division. The R1-.R6 dividers follow the same format as the R0 divider described above.

Table 14.94. Si5383/84 R1-R6 Divider Registers that Follow R0 Definitions

Register Address	Description	Size	Same as Address
0x0250-0x0252	R1_REG	24-bit Integer Number	0x024A-0x024C
0x0253-0x0255	R2_REG	24-bit Integer Number	0x024A-0x024C
0x0256-0x0258	R3_REG	24-bit Integer Number	0x024A-0x024C
0x025C-0x025E	R4_REG	24-bit Integer Number	0x024A-0x024C
0x025F-0x0261	R5_REG	24-bit Integer Number	0x024A-0x024C
0x0262-0x0264	R6_REG	24-bit Integer Number	0x024A-0x024C

Table 14.95. Register 0x026B-0x0272 Design Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x026B	7:0	R/W	DESIGN_ID0	ASCII encoded string defined by ClockBuilder Pro user, with user defined space or null padding of unused characters. A user will normally include a configuration ID + revision ID. For example, ULT.1A with null character padding sets: DESIGN_ID0: 0x55 DESIGN_ID1: 0x4C DESIGN_ID2: 0x54 DESIGN_ID3: 0x2E DESIGN_ID4: 0x31 DESIGN_ID5: 0x41 DESIGN_ID6:0x 00 DESIGN_ID7: 0x00
0x026C	15:8	R/W	DESIGN_ID1	
0x026D	23:16	R/W	DESIGN_ID2	
0x026E	31:24	R/W	DESIGN_ID3	
0x026F	39:32	R/W	DESIGN_ID4	
0x0270	47:40	R/W	DESIGN_ID5	
0x0271	55:48	R/W	DESIGN_ID6	
0x0272	63:56	R/W	DESIGN_ID7	

Table 14.96. Register 0x0278-0x027C OPN Identifier

Reg Address	Bit Field	Type	Setting Name	Description
0x0278	7:0	R/W	OPN_ID0	OPN unique identifier. ASCII encoded. For example, with OPN: 5348B-A12345-GM, 12345 is the OPN unique identifier: OPN_ID0: 0x31 OPN_ID1: 0x32 OPN_ID2: 0x33 OPN_ID3: 0x34 OPN_ID4: 0x35
0x0279	15:8	R/W	OPN_ID1	
0x027A	23:16	R/W	OPN_ID2	
0x027B	31:24	R/W	OPN_ID3	
0x027C	39:32	R/W	OPN_ID4	

Part numbers are of the form:

Si<Part Num Base><Grade>-<Device Revision><OPN ID>-<Temp Grade><Package ID>

Examples:

Si5383B-D12345-GM

Applies to a "custom": OPN (Ordering Part Number) device. These devices are factory pre-programmed with the frequency plan and all other operating characteristics defined by the user's ClockBuilder Pro project file.

Si5383B-D-GM

Applies to a "base" or "non-custom" OPN device. Base devices are factory pre-programmed to a specific base part type (e.g., Si5383 but **exclude** any user-defined frequency plan or other user-defined operating characteristics selected in ClockBuilder Pro).

Table 14.97. Register 0x0294 -0x0295 FASTLOCK EXTEND SCL

Reg Address	Bit Field	Type	Setting Name	Description
0x0294[1]	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLA	Calculated by .CBPro.
0x0294	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLB	Calculated by CBPro.
x0295[1]	3:0	R/W	FASTLOCK_EXTEND_SCL_PLLC	Calculated by CBPro.
x0295	7:4	R/W	FASTLOCK_EXTEND_SCL_PLLD	Calculated by CBPro.

Note:
1. Si5383 only.

Table 14.98. Register 0x0297 -0x02A7 FASTLOCK DLY ONSW_EN

Reg Address	Bit Field	Type	Setting Name	Description
0x297[1]	3	R/W	FAST-LOCK_DLY_ONSW_EN_PLLA	0: Disables FAST-LOCK_DLY_ONSW_EN PLLA 1: Enables FAST-LOCK_DLY_ONSW_EN PLLA
0x297	2	R/W	FAST-LOCK_DLY_ONSW_EN_PLLB	0: Disables FAST-LOCK_DLY_ONSW_EN PLLB 1: Enables FAST-LOCK_DLY_ONSW_EN PLLB
0x297[1]	1	R/W	FAST-LOCK_DLY_ONSW_EN_PLLC	0: Disables FAST-LOCK_DLY_ONSW_EN PLLC 1: Enables FAST-LOCK_DLY_ONSW_EN PLLC
0x297	0	R/W	FAST-LOCK_DLY_ONSW_EN_PLLD	0: Disables FAST-LOCK_DLY_ONSW_EN PLLD 1: Enables FAST-LOCK_DLY_ONSW_EN PLLD
0x2A6[1]	19:0	R/W	FAST-LOCK_DLY_ONSW_PLL A	Value calculated in CBPro based on Frequency Plan.
0x02A9, 0x02AA, 0x02AB	19:0	R/W	FAST-LOCK_DLY_ONSW_PLL B	Value calculated in CBPro based on Frequency Plan.
x02AC, 0x02AD, 0x02AE[1]	19:0	R/W	FAST-LOCK_DLY_ONSW_PLL C	Value calculated in CBPro based on Frequency Plan.
0x02AF, 0x02B0, 0x02B1	19:0	R/W	FAST-LOCK_DLY_ONSW_PLL D	Value calculated in CBPro based on Frequency Plan.

Note:
1. Si5383 only.

Table 14.99. Register 0x0299 -0x02A3 FASTLOCK DLY ONLOL_EN

Reg Address	Bit Field	Type	Setting Name	Description
0x299[1]	3	R/W	FASTLOCK_DLY_ONLOL_EN_PLLA	0: Disables FASTLOCK_DLY_ONSW_PLLA 1: Enables FASTLOCK_DLY_ONSW_PLLA
0x299	2	R/W	FASTLOCK_DLY_ONLOL_EN_PLLB	0: Disables FASTLOCK_DLY_ONSW_PLLA 1: Enables FASTLOCK_DLY_ONSW_PLLA
0x299[1]	1	R/W	FASTLOCK_DLY_ONLOL_EN_PLLC	0: Disables FASTLOCK_DLY_ONSW_PLLA 1: Enables FASTLOCK_DLY_ONSW_PLLA
0x299	0	R/W	FASTLOCK_DLY_ONLOL_EN_PLLD	0: Disables FASTLOCK_DLY_ONSW_PLLA 1: Enables FASTLOCK_DLY_ONSW_PLLA
0x29A[1]	19:0	R/W	FASTLOCK_DLY_ONLOL_PLLA	Value calculated in CBPro based on value selected.
0x29D	19:0	R/W	FASTLOCK_DLY_ONLOL_PLLB	Value calculated in CBPro based on value selected.
0x2A0[1]	19:0	R/W	FASTLOCK_DLY_ONLOL_PLLC	Value calculated in CBPro based on value selected.
0x2A3	19:0	R/W	FASTLOCK_DLY_ONLOL_PLLD	Value calculated in CBPro based on value selected.

Note:
1. Si5383 only.

Table 14.100. Register 0x02B7 LOL_NOSIG_TIME_PLLA, B,C,D

Reg Address	Bit Field	Type	Setting Name	Description
0x02B7[1]	1:0	R/W	LOL_NO-SIG_TIME_PLLA	0: 1.7 sec 1: 107 ms 2: 67 ms 3: 417 µs
0x02B7	3:2	R/W	LOL_NO-SIG_TIME_PLLB	
0x02B7[1]	5:4	R/W	LOL_NO-SIG_TIME_PLLC	
0x02B7	7:6	R/W	LOL_NO-SIG_TIME_PLLD *(Standard Input mode)*	

Note:
1. Si5383 only.

Table 14.101. Register 0x02B8 LOL_LOS_REFCLK_PLLA, B,C,D

Reg Address	Bit Field	Type	Setting Name	Description
0x02B8[1]	0	R	LOL__LOS_REFCLK_PLLA	0: No alarm 1: Alarm
0x02B8	1	R	LOL__LOS_REFCLK_PLLB	0: No alarm 1: Alarm
0x02B8[1]	2	R	LOL__LOS_REFCLK_PLLC	0: No alarm 1: Alarm
0x02B8	3	R	LOL__LOS_REFCLK_PLLD *(Standard Input mode)*	0: No alarm 1: Alarm

Note:
1. Si5383 only.

Table 14.102. Register 0x02B9 LOL_LOS_REFCLK_PLLA, B,C,D_FLG

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9[1]	0	R/W	LOL__LOS_REFCLK_PLLA _FLG	0: No alarm 1: Alarm
0x02B9	1	R/W	LOL__LOS_REFCLK_PLLB_FLG	0: No alarm 1: Alarm
0x02B9[1]	2	R/W	LOL__LOS_REFCLK_PLLC_FLG	0: No alarm 1: Alarm

Reg Address	Bit Field	Type	Setting Name	Description
0x02B9	3	R/W	LOL__LOS_REFCLK_PLLD_FLG *(Standard Input mode)*	0: No alarm 1: Alarm

Note:
1. Si5383 only.

Table 14.103. Register 0x02BC LOS CMOS Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x02BC	1:0	R/W	LOS_CMOS_EN	0: Disable LOS 1: Enable LOS for a clock input
0x02BC	5:4	R/W	LOS_CMOS_EN_1HZ	0: Disable LOS for 1 Hz inputs 1: Enable LOS for 1 Hz inputs

Note:
1. Bit Field [0] = IN3 and Bit Field [1] = IN4

Table 14.104. Register 0x02BD LOS CMOS VAL TIME

Reg Address	Bit Field	Type	Setting Name	Description
0x02BD	1:0	R/W	LOS_CMOS0_VAL_TIME(IN3)	Caclulated by CBPro.
0x02BD	3:2	R/W	LOS_CMOS1_VAL_TIME(IN4)	Caclulated by CBPro.

Table 14.105. Register 0x02BE - 0x02C0 LOS CMOS TRG_THR

Reg Address	Bit Field	Type	Setting Name	Description
0x02BE, 0x02BF	15:0	R/W	LOS_CMOS0_TRG_THR (IN3)	Caclulated by CBPro.
0x02C0, 0x02C1	15:0	R/W	LOS_CMOS1_TRG_THR (IN4)	Calculated by CBPro..

Table 14.106. Register 0x02C2 - 0x02C4 LOS CMOS CLR_THR

Reg Address	Bit Field	Type	Setting Name	by Description
0x02C2, 0x02C3	15:0	R/W	LOS_CMOS0_CLR_THR (IN3)	Calculated by CBPro.
0x02C4, 0x02C5	15:0	R/W	LOS_CMOS1_CLR_THR (IN4)	Calculated by CBPro.

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Table 14.107. Register 0x0302-0305, 0x030D-0x0310, 0x0318-0x031B, 0x0323-0x0326 N0x Numerator

Reg Address	Bit Field	Type	Setting Name	Description
0x0302	7:0	R/W	N0_NUM	Cacluated by CBPro.
0x0303	15:8			
0x0304	23:16			
0x0305	31:24			
0x030D	7:0	R/W	N1_NUM	Cacluated by CBPro.
0x030E	15:8			
0x030F	23:16			
0x0310	31:24			
0x0318	7:0	R/W	N2_NUM	Calculated CBPro.
0x0319	15:8			
0x031A	23:16			
0x031B	31:24			
0x0323	7:0	R/W	N3_NUM	Cacluated by CBPro.
0x0324	15:8			
0x0325	23:16			
0x0326	31:24			

Table 14.108. Register 0x0308-0x030B, 0x0313-0x0316, 0x031E-0x0321, 0x0329-0x032C Nx Denominator

Reg Address	Bit Field	Type	Setting Name	Description
0x0308	7:0	R/W	N0_DEN	Calculated by CBPro..
0x0309	15:8			
0x030A	23:16			
0x030B	31:24			
0x0313	7:0	R/W	N1_DEN	Calculated by CBPro.
0x0314	15:8			
0x0315	23:16			
0x0316	31:24			
0x031E	7:0	R/W	N2_DEN	Calculated by CBPro.
0x031F	15:8			
0x0320	23:16			
0x0321	31:24			

Reg Address	Bit Field	Type	Setting Name	Description
0x0329	7:0	R/W	N3_DEN	Calculated by CBPro.
0x032A	15:8			
0x032B	23:16			
0x032C	31:24			

Table 14.109. DSPLL Internal Divider Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x030C	0	S	N0_UPDATE	Write 1 to update all N0 values
0x0317	0	S	N1_UPDATE	Write 1 to update all N1 values
0x0322	0	S	N2_UPDATE	Write 1 to update all N2 values
0x032D	0	S	N3_UPDATE	Write 1 to update all N3 values

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.110. Registers 0x0338 All DSPLL Internal Dividers Update Bit

Reg Address	Bit Field	Type	Setting Name	Description
0x0338	1	S	N_UPDATE_ALL	Writing a 1 to this bit will update all DSPLL internal divider values. When this bit is written, all other bits in this register must be written as zeros.

ClockBuilder Pro handles these updates when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.111. Register 0x0339 FINC/FDEC Masks

Reg Address	Bit Field	Type	Name	Description
0x0339	4:0	R/W	N_FSTEP_MSK	0 to enable FINC/FDEC updates 1 to disable FINC/FDEC updates

- Bit 0 corresponds to MultiSynth N0 N_FSTEP_MSK 0x0339[0]
- Bit 1 corresponds to MultiSynth N1 N_FSTEP_MSK 0x0339[1]
- Bit 2 corresponds to MultiSynth N2 N_FSTEP_MSK 0x0339[2]
- Bit 3 corresponds to MultiSynth N3 N_FSTEP_MSK 0x0339[3]
- Bit 4 corresponds to MultiSynth N4 N_FSTEP_MSK 0x0339[4]

There is one mask bit for each of the five N dividers. Figure 55, “Logic Diagram of the FINC/FDEC Masks,” on page 113 shows the logic diagram of the FINC/FDEC masks.

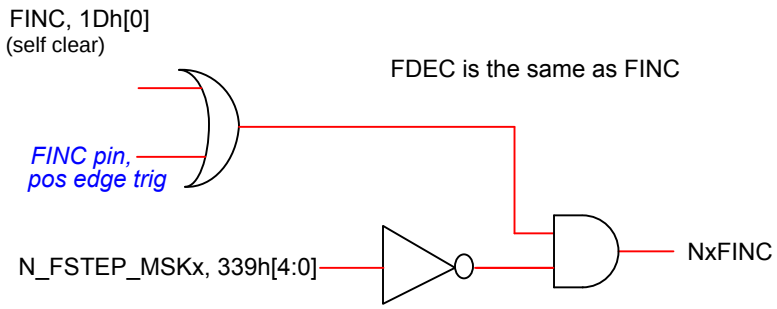

Figure 14.1. Logic Diagram of the FINC/FDEC Masks

Table 14.112. 0x033B-0x0340 N0 Frequency Step Word

Reg Address	Bit Field	Type	Name	Description
0x033B	7:0	R/W	N0_FSTEPW	Calculated by CBPro
0x033C	15:8	R/W	N0_FSTEPW	
0x033D	23:16	R/W	N0_FSTEPW	
0x033E	31:24	R/W	N0_ FSTEPW	
0x033F	39:32	R/W	N0_ FSTEPW	
0x0340	43:40	R/W	N0_ FSTEPW	

Table 14.113. Registers that Follow the N0_FSTEPW Definitions

Register Address	Description	Size	Same as Address
0x0341-0x0346	N1 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x0347-0x034C	N2 Frequency Step Word	44-bit Integer Number	0x033B-0x0340
0x034D-0x0352	N3 Frequency Step Word	44-bit Integer Number	0x033B-0x0340

14.3.5 Page 4 Registers Si5383

Page 4 Registers apply to the Si5383 only.

Table 14.114. Register 0x0402 PLLA PFD settings

Reg Address	Bit Field	Type	Setting Name	Description
0x0402	0	R/W	PFD_PDNB_PLLA	0: Powered Down 1: Powered On
0x0402	1	R/W	PFD_RST_PLLA	0: Normal Operation 1: Reset PFD
0x0402	2	R/W	M_RST_PLLA	0: Normal Operation 1: Reset N2 divider
0x0402	3	R/W	PFD_CLKM_STOP_PLLA	0: Normal Operation 1: Stop Clock
0x0402	4	R/W	ADD_DIV256_PLLA	0: Disabled 1: Enabled

Table 14.115. Register 0x0407 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0407	7:6	R	IN_PLLA_ACTV	Current input clock

These bits indicate which input clock DSPLL A is currently selected. 0 for IN0; 1 for IN1; etc.

Table 14.116. Register 0x0408-0x040D DSPLL A Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0408	5:0	R/W	BW0_PLLA	Calculated by CBPro.
0x0409	5:0	R/W	BW1_PLLA	
0x040A	5:0	R/W	BW2_PLLA	
0x040B	5:0	R/W	BW3_PLLA	
0x040C	5:0	R/W	BW4_PLLA	
0x040D	5:0	R/W	BW5_PLLA	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 14.117. Register 0x040E-0x0414 DSPLL A Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x040E	5:0	R/W	FAST_BW0_PLLA	Calculated by CBPro.
0x040F	5:0	R/W	FAST_BW1_PLLA	
0x0410	5:0	R/W	FAST_BW2_PLLA	
0x0411	5:0	R/W	FAST_BW3_PLLA	
0x0412	5:0	R/W	FAST_BW4_PLLA	
0x0413	5:0	R/W	FAST_BW5_PLLA	
0x0414	0	S	BW_UPDATE_PLLA	0: No effect. 1: Update the Normal, Fastlock and Exit from Holdover BWs for PLL A.

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLA to update the BW parameters for this DSPLL. Soft Reset does nnot update the DSPLL bandwidth parameters.

Table 14.118. Register 0x0415-0x041B MA Divider Numerator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0415	7:0	R/W	M_NUM_PLLA	Calculated by CBPro..
0x0416	15:8	R/W	M_NUM_PLLA	
0x0417	23:16	R/W	M_NUM_PLLA	
0x0418	31:24	R/W	M_NUM_PLLA	
0x0419	39:32	R/W	M_NUM_PLLA	
0x041A	47:40	R/W	M_NUM_PLLA	
0x041B	55:48	R/W	M_NUM_PLLA	

The MA divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.119. Register 0x041C-0x041F MA Divider Denominator for DSPLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x041C	7:0	R/W	M_DEN_PLLA	Cacluated by CBPro.
0x041D	15:8	R/W	M_DEN_PLLA	
0x041E	23:16	R/W	M_DEN_PLLA	
0x041F	31:24	R/W	M_DEN_PLLA	

The loop MA divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan annd are written into these registers.

Table 14.120. Register 0x0420 M Divider Update Bit for PLL A

Reg Address	Bit Field	Type	Setting Name	Description
0x0420	0	S	M_UPDATE_PLLA	Must write a 1 to this bit to cause PLL A M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.121. Register 0x0421 M Divider Fractional Control and Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0421	3:0	R/W	M_FRAC_MODE_PLLA	Managed by CBPro
0x0421	4	R/W	M_FRAC_EN_PLLA	M divider fractional enable 0: Interger mode 1: Enable fractional modulator Will be enabled when in DCO mode.

Table 14.122. Register 0x0422 DSPLL A FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0422	0	R/W	M_FSTEP_MSK_PLLA	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.
0x0422	1	R/W	M_FSTEP_DEN_PLLA	0: Modify Numerator 1: Modify Denominator

Table 14.123. Register 0x0423-0x0429 DSPLLA MA Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0423	7:0	R/W	M_FSTEPW_PLLA	Calculated by CBPro.
0x0424	15:8	R/W	M_FSTEPW_PLLA	
0x0425	23:16	R/W	M_FSTEPW_PLLA	
0x0426	31:24	R/W	M_FSTEPW_PLLA	
0x0427	39:32	R/W	M_FSTEPW_PLLA	
0x0428	47:40	R/W	M_FSTEPW_PLLA	
0x0429	55:48	R/W	M_FSTEPW_PLLA	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL A is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also registers 0x0415–0x041F.

Table 14.124. Register 0x042A DSPLL A Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x042A	2:0	R/W	IN_SEL_PLLA	0: For IN0 1: For IN1 2: For IN2 3-7: Reserved

This is the input clock selection for manual register-based clock selection.

Table 14.125. Register 0x042B DSPLL A Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x042B	0	R/W	FASTLOCK_AUTO_EN_PLLA	Applies when FASTLOCK_MAN_PLLA=0. 0: To disable auto fast lock when PLLA is out of lock 1: To enable auto fast lock
0x042B	1	R/W	FASTLOCK_MAN_PLLA	0: For normal operation 1: For force fast lock

Table 14.126. DSPLLA Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Descrption
0x042C	0	R/W	HOLD_EN_PLLA	0: Holdover Disabled 1: Holdover Enabled. Standard setting.
0x042C	3	R/W	HOLD_RAMP_BYP_PLLA	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover
0x042C	4	R/W	HOLD_EXITBW_SEL1_PLLA	This bit with HOLDEXIT_BW_SEL0_PLLA are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit.
0x042C	7:5	R/W	HOLD_RAMP_RATE_PLLA	The ramp rate is selected when using CBPro.

Table 14.127. Register 0x042D HOLD_RAMPBYP_NOHIST_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x042D	1	R/W	HOLD_RAMP-BYP_NOHIST_PLLA	0: Bypass is disabled 1: Bypasss is enabled

Note:
1. Bypass digital hold exit ramping when there is no valid history.

Table 14.128. Register 0x042E DSPLL A Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x042E	4:0	R/W	HOLD_HIST_LEN_PLLA	Calculated by CBPro.

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See Section 4.4.4 Holdover Mode to calculate the window length from the register value.

Table 14.129. Register 0x042F DSPLLA Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x042F	4:0	R/W	HOLD_HIST_DE-LAY_PLLA	Calculated by CBpro.

Table 14.130. Register 0x0431 HOLD_REF_COUNT_FRC_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0431	4:0	R/W	HOLD_REF_COUNT_FRC_PLLA	Calculated by CBPro.

Note:
1. Holdover exit ramp optimzation.

Table 14.131. Register 0x0432 HOLD_15M_CYC_COUNT_PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0432	7:0	R/W	HOLD_15M_CYC_COUNT_PLLA	Calcuated by CBPro.
0x0432	15:8			
0x0432	23:16			

Note:
1. Sets up a time to wait before starting to measure the digital hold history.

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See Section 4.4.4 Holdover Mode to calculate the window length from the register value.

Table 14.132. Register 0x0435 DSPLL A Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0435	0	R/W	FORCE_HOLD_PLLA	0: For normal operation. 1: To force holdover.

Table 14.133. Register 0x0436 DSPLLA Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0436	1:0	R/W	CLK_SWITCH_MODE_PLLA	Clock Selection Mode 0: Manual. 1: Automatic, non-revertive. 2: Automatic, revertive. 3: Reserved.
0x0436	2	R/W	HSW_EN_PLLA	0: Glitchless switching mode (phase buildout turned off). 1: Hitless switching mode (phase buildout turned on).

Table 14.134. Register 0x0437 DSPLLA Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0437	3:0	R/W	IN_LOS_MSK_PLLA	For each clock input LOS alarm 0: To use LOS in the clock selection logic. 1: To mask LOS from the clock selection logic.
0x0437	7:4	R/W	IN_OOF_MSK_PLLA	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0437[0], OOF alarm 0x0437[4]

IN1 Input 1 applies to LOS alarm 0x0437[1], OOF alarm 0x0437[5]

IN2 Input 2 applies to LOS alarm 0x0437[2], OOF alarm 0x0437[6]

Table 14.135. Register 0x0438 DSPLL A Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0438	2:0	R/W	IN0_PRIORITY_PLLA	The priority for clock input 0 is: 0: Clock input not selected. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4-7: Reserved.
0x0438	6:4	R/W	IN1_PRIORITY_PLLA	The priority for clock input 1 is: 0: Clock input not selected. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4-7: Reserved.

Table 14.136. Register 0x0439 DSPLL A Clock Inputs 2 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0439	2:0	R/W	IN2_PRIORITY_PLLA	The priority for clock input 2 is: 0: Clock input not selected. 1: For priority 1. 2: For priority 2. 3: For priority 3. 4-7: Reserved.

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.137. Register 0x043A Hitless Switching mode for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	1:0	R/W	HSW_MODE_PLLA	0: OL Logic decides whether to use only course or course plus fine phase measurement. Coarse plus fine is used only when switching in manual mode and inputs clock are valid. 1: Force coarse plus fine phas adjustment whether or not input clocks are valid. Input clock must be valid. 2: Use coarse measurement and adjustment only. 3: Same as 0

Reg Address	Bit Field	Type	Setting Name	Description
0x043A	3:2	R/W	HSW_PHMEAS_CTRL_PLLA	0: Use HSW_PHMEAS_THR_PLLA to decide wether or not to apply a new phase measurement 1: Apply a new phase measurement for every hitless switch 2: Undo the phase adjustment that was applied on the switch from CLK1 to CLK2 3: Same as 0.

Table 14.138. Register 0x043B and 0x043C Hitless Switching Phase Threshold for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043B	7:0	R/W	HSW_PHMEAS_THR_PLLA	Calculated by CBPro.
0x043C	9:8	R/W	HSW_PHMEAS_THR_PLLA	

Table 14.139. Register 0x043D Hitless Switching Length for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043D	4:0	R/W	HSW_COARSE_PM_LEN_PLLA	Calculated by CBPro.

Table 14.140. Register 0x043E Hitless Switching Delay for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x043E	4:0	R/W	HSW_COARSE_PM_DLY_PLLA	Calculated by CBPro.

Table 14.141. Register 0x043F DSPLL A Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x043F	1	R	HOLD_HIST_VALID_PLLA	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid. 1: Valid.
0x043F	2	R	FASTLOCK_STATUS_PLLA	0: Not in Fastlock. 1: Fastlock active.

Table 14.142. Register 0x0488 Hitless Switching Length, Fine Adjust, for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0488	3:0	R/W	HSW_FINE_PM_LEN_PLLA	Calculated by CBPro.

Table 14.143. Register 0x0489 and 0x048A PFD Enable Delay for PLLA

Reg Address	Bit Field	Type	Setting Name	Description
0x0489	7:0	R/W	PFD_EN_DLY_PLLA	Calculated by CBPro.
0x048A	12:8	R/W	PFD_EN_DLY_PLLA	

Table 14.144. Registers 0x049B, Exit from Holdover BW Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x049B	6	R/W	HOLDEX-IT_BW_SEL0_PLLA	Managed by CBPro. See HOLDEX-IT_BW_SEL1_PLLA
0x049B	7	R/W	HOLDEX-IT_STD_BO_PLLA	0: Normal fine phase adjustment 1: Skip fine phase adjustment

Table 14.145. Registers 0x049D- 0x004A2, Exit from Holdover BW Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x049D	5:0	R/W	BW0_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x049E	5:0	R/W	BW1_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x049F	5:0	R/W	BW2_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x04A0	5:0	R/W	BW3_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x04A1	5:0	R/W	BW4_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Reg Address	Bit Field	Type	Setting Name	Description
0x04A2	5:0	R/W	BW5_HO_PLLA	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Table 14.146. DSPLLA Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x04A6	3	R/W	Ramp_Switch_EN_PLLA	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x04A6	2:0	R/W	RAMP_STEP_SIZE_PLLA	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

14.3.6 Page 5 Registers Si5383/84

The page 5 registers are associated with DSPLLB, which is the Reference DSPLL and is responsible for supplying the VCO frequency to the other DSPLLs. Because of this, changes to DSPLLB will have an effect onn all the DSPLLs. This warning applies to all the page 5 registers.

Table 14.147. Register 0x0508-0x050D DSPLL B (Reference) Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0508	5:0	R/W	BW0_PLLB	Calculated by CBPro.
0x0509	5:0	R/W	BW1_PLLB	
0x050A	5:0	R/W	BW2_PLLB	
0x050B	5:0	R/W	BW3_PLLB	
0x050C	5:0	R/W	BW4_PLLB	
0x050D	5:0	R/W	BW5_PLLB	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers. The BW_UPDATE bit (register 0x0514[0] must be set to cause the normal and fast bandwidth parameters to be active.

Table 14.148. Register 0x050E-0x0514 DSPLL B (Reference) Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x050E	5:0	R/W	FAST_BW0_PLLB	Calculated by CBPro.
0x050F	5:0	R/W	FAST_BW1_PLLB	
0x0510	5:0	R/W	FAST_BW2_PLLB	
0x0511	5:0	R/W	FAST_BW3_PLLB	
0x0512	5:0	R/W	FAST_BW4_PLLB	
0x0513	5:0	R/W	FAST_BW5_PLLB	
0x0514	0	S	BW_UPDATE_PLLB	0: No effect 1: Update both the Normal and Fastlock BWs for PLL B (Reference).

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLB to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.

Table 14.149. Register 0x0515-0x051B MB Divider Numerator for DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x0515	7:0	R/W	M_NUM_PLLB	Calculated by CBPro..
0x0516	15:8	R/W	M_NUM_PLLB	
0x0517	23:16	R/W	M_NUM_PLLB	
0x0518	31:24	R/W	M_NUM_PLLB	
0x0519	39:32	R/W	M_NUM_PLLB	
0x051A	47:40	R/W	M_NUM_PLLB	
0x051B	55:48	R/W	M_NUM_PLLB	

The MB divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.150. Register 0x051C-0x051F MB Divider Denominator for DSPLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x051C	7:0	R/W	M_DEN_PLLB	Calculated by CBPro.
0x051D	15:8	R/W	M_DEN_PLLB	
0x051E	23:16	R/W	M_DEN_PLLB	
0x051F	31:24	R/W	M_DEN_PLLB	

The loop MB divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.151. Register 0x0520 M Divider Update Bit for PLL B (Reference)

Reg Address	Bit Field	Type	Setting Name	Description
0x0520	0	S	M_UPDATE_PLLB	Must write a 1 to this bit to cause PLL B M divider changes to take effect.

Table 14.152. 0x0521 M Divider Fractional Control and Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0521	3:0	R/W	M_FRAC_MODE_PLLB	Managed by CBPro
0x0521	4	R/W	M_FRAC_EN_PLLB	M divider fractional enable 0: Interger Mode 1: Enable fractional modulator Will be enabled when in DCO mode.

Table 14.153. 0x0521 Hitless Switching Phase Threshold for PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x053B	7:0	R/W	HSW_PHMEAS_THR_PLLB	Calculated by CBPro.
0x053C	2:0	R/W	HSW_PHMEAS_THR_PLLB	

Table 14.154. Register 0x053A Hitless Switching Mode for PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x053A	1:0	R/W	HSW_MODE_PLLB	Managed by CBPro

Table 14.155. Register 0x053D Hitless Switching Length for PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x053D	1:0	R/W	HSW_Course_PM_LEN_PLLB	Managed by CBPro.

Table 14.156. Register 0x053A Hitless Switching Delay for PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x053E	4:0	R/W	HSW_COARSE_PM_PLLB	Managed by CBPro.

Table 14.157. Register 0x0B89-0x058A PFD Enabled Delay PLLB

Reg Address	Bit Field	Type	Setting Name	Description
0x0589	7:0	R/W	PFD_EN_DELAY_PLLB	Managed by CBPro
0x058A	4:0	R/W	PFD_EN_DELAY_PLLB	

Table 14.158. Register 0x059B Exit from Holdover BW Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x059B	6	R/W	HOLD_EXIT_BW_SEL0_PLLB	Managed by CBPro
0x059B	7	R/W	HOLD_EXIT_STD_BO_PLLB	0: Normal fine phase adjustment 1: Skip fine phase adjustment

Table 14.159. Registers 0x059D-0x05A2 Exit from Holdover BW Select

Reg Address	Bit Field	Type	Setting Name	Description
0x059D	5:0	R/W	HOLDEXIT_BW0_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x059E	5:0	R/W	HOLDEXIT_BW1_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x059F	5:0	R/W	HOLDEXIT_BW2_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x05A0	5:0	R/W	HOLDEXIT_BW3_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x05A1	5:0	R/W	HOLDEXIT_BW4_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x05A2	5:0	R/W	HOLDEXIT_BW5_PLLB	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.160. Register 0x05A6 DSPLLB Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x05A6	2:0	R/W	RAMP_STEP_SIZE_PLLB	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x05A6	3	R/W	RAMP_STEP_SIZE_PLLB	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

14.3.7 Page 6 Registers Si5383

Page 6 Registers apply to the Si5383 only.

Table 14.161. Register 0x0602 Add an additional 256 Divide-by

Reg Address	Bit Field	Type	Setting Name	Description
0x0602	4	R/W	ADD_DIV256_PLLC	0: Disabled 1: Enabled

Table 14.162. Register 0x0607 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0607	7:6	R	IN_PLLC_ACTV	Current input clock

These bits indicate which input clock DSPLL C is currently selected. 0 for IN0; 1 for IN1; etc.

Table 14.163. Register 0x0608-0x060D DSPLL C Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0608	5:0	R/W	BW0_PLLC	The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.
0x0609	5:0	R/W	BW1_PLLC	
0x060A	5:0	R/W	BW2_PLLC	
0x060B	5:0	R/W	BW3_PLLC	
0x060C	5:0	R/W	BW4_PLLC	
0x060D	5:0	R/W	BW5_PLLC	

Table 14.164. Register 0x060E-0x0614 DSPLL C Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x060E	5:0	R/W	FAST_BW0_PLLC	The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers. Note that a 1 must be written to BW_UPDATE_PLLC to update the BW parameters for this DSPLL. Soft Reset does not update the DSPLL bandwidth parameters.
0x060F	5:0	R/W	FAST_BW1_PLLC	
0x0610	5:0	R/W	FAST_BW2_PLLC	
0x0611	5:0	R/W	FAST_BW3_PLLC	
0x0612	5:0	R/W	FAST_BW4_PLLC	
0x0613	5:0	R/W	FAST_BW5_PLLC	
0x0614	0	S	BW_UPDATE_PLLC	0: No effect. 1: Update both the Normal and Fastback BWs for PLL C.

Table 14.165. Register 0x0615-0x061B MC Divider Numerator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0615	7:0	R/W	M_NUM_PLLC	Calculated by CBPro
0x0616	15:8	R/W	M_NUM_PLLC	
0x0617	23:16	R/W	M_NUM_PLLC	
0x0618	31:24	R/W	M_NUM_PLLC	
0x0619	39:32	R/W	M_NUM_PLLC	
0x061A	47:40	R/W	M_NUM_PLLC	
0x061B	55:48	R/W	M_NUM_PLLC	

Table 14.166. Register 0x061C-0x061F MC Divider Denominator for DSPLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x061C	7:0	R/W	M_DEN_PLLC	Calculated by CBPro
0x061D	15:8	R/W	M_DEN_PLLC	
0x061E	23:16	R/W	M_DEN_PLLC	
0x061F	31:24	R/W	M_DEN_PLLC	

Table 14.167. Register 0x0620 M Divider Update Bit for PLL C

Reg Address	Bit Field	Type	Setting Name	Description
0x0620	0	S	M_UP-DATE_PLLC	Must write a 1 to this bit to cause PLL C M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.168. Register 0x0621 M Divider Fractional Control Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0621	3:0	R/W	M_FRAC_MODE_PLLC	Managed by CBPro
0x0621	4	R/W	M_FRAC_EN_PLLC	M divider fractional enable 0: Interger Mode 1: Enable fractional modulator Will be enabled when in DCO mdoe.

Table 14.169. Register 0x0622 DSPLL C FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	0	R/W	M_FSTEP_MSK_PLLC	0: To enable FINC/FDEC updates. 1: To disable FINC/FDEC updates.

Reg Address	Bit Field	Type	Setting Name	Description
0x0622	1	R/W	MFSTEP_DEN_PLLC	0: Modify Numerator 1: Modify Denominator

Table 14.170. Register 0x0623-0x0629 DSPLLC MC Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0623	7:0	R/W	M_FSTEPW_PLLC	The frequency step word (FSTEPW) for the feedback M divider of DSPLL C is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0615–0x061F. Calculated by CBPro.
0x0624	15:8	R/W	M_FSTEPW_PLLC	
0x0625	23:16	R/W	M_FSTEPW_PLLC	
0x0626	31:24	R/W	M_FSTEPW_PLLC	
0x0627	39:32	R/W	M_FSTEPW_PLLC	
0x0628	47:40	R/W	M_FSTEPW_PLLC	
0x0629	55:48	R/W	M_FSTEPW_PLLC	

Table 14.171. Register 0x062A DSPLL C Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x062A	2:0	R/W	IN_SEL_PLLC	This is the input clock selection for manual register based clock selection. 0: For IN0 1: For IN1 2: For IN2 3-7: Reserved

Table 14.172. Register 0x062B DSPLL C Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x062B	0	R/W	FASTLOCK_AUTO_EN_PLLC	Applies when FASTLOCK_MAN_PLLC=0. 0: To disbale auto fast lock when PLLB is out of lock 1: To enable auto fast lock
0x062B	1	R/W	FASTLOCK_MAN_PLLC	0: For normal operation 1: For force fast lock

Table 14.173. Register 0x062C DSPLL C Holdover Control

Reg Address	Bit Field	Type	Setting Name	Descrption
0x062C	0	R/W	HOLD_EN_PLLC	0: Holdover Disabled 1: Holdover Enabled. Standard setting.

Reg Address	Bit Field	Type	Setting Name	Descrption
0x062C	3	R/W	HOLD_RAMP_BYP_PLLC	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover
0x062C	4	R/W	HOLD_EXITBW_SEL1_PLLC	This bit with HOLDEXIT_BW_SEL0_PLLB are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit.
0x062C	7:5	R/W	HOLD_RAMP_RATE_PLLC	The ramp rate is selected when using CBPro.

Table 14.174. Register 0x062D HOLD_RAMPBYP_NOHIST_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x062D	1	R/W	HOLD_RAMPBYP_NOHIST_PLLC	0: Disabled 1: Enabled

Note:
1. Bypass digital hold exit ramping when there is no valid history.

Table 14.175. Register 0x062E DSPLL C Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x062E	4:0	R/W	HOLD_HIST_LEN_PLLC	Calculated by CBPro

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See Section 4.4.4 Holdover Mode to calculate the window length from the register value.

Table 14.176. Register 0x062F DSPLLC Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x062F	4:0	R/W	HOLD_HIST_DELAY_PLLC	Calculated by CBPro

Table 14.177. Register 0x0631 HOLD_REF_COUNT_FRC_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0631	4:0	R/W	HOLD_REF_COUNT_FRC_PLLC	Calculated by CBPro

Note:
1. Holdover exit ramp optimzation.

Table 14.178. Register 0x0632 HOLD_15M_CYC_COUNT_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0632	7:0	R/W	HOLD_15M_CYC_COUNT_PLLC	Calcuated by CBPro.
0x0632	15:8			
0x0632	23:16			

Note:
1. Sets up a time to wait before starting to measure the digital hold history.

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushed back into the past. The amount the average window is delayed is the holdover history delay. See Section 4.4.4 Holdover Mode to calculate the ignore delay time from the register value.

Table 14.179. Register 0x0635 DSPLL C Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0635	0	R/W	FORCE_HOLD_PLLC	0: For normal operation 1: To force holdover

Table 14.180. Register 0x0636 DSPLLC Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0636	1:0	R/W	CLK_SWITCH_MODE_PLLC	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0636	2	R/W	HSW_EN_PLLC	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

Table 14.181. Register 0x0637 DSPLLC Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	3:0	R/W	IN_LOS_MSK_PLLC	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic

Reg Address	Bit Field	Type	Setting Name	Description
0x0637	7:4	R/W	IN_OOF_MSK_PLLC	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applies to LOS alarm 0x0637[0], OOF alarm 0x0637[4]

IN1 Input 1 applies to LOS alarm 0x0637[1], OOF alarm 0x0637[5]

IN0 Input 2 applies to LOS alarm 0x0637[2], OOF alarm 0x0637[6]

Table 14.182. Register 0x0638 DSPLL C Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0638	2:0	R/W	IN0_PRIORITY_PLLC	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7: Reserved
0x0638	6:4	R/W	IN1_PRIORITY_PLLC	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7: Reserved

Table 14.183. Register 0x0639 DSPLL C Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	2:0	R/W	IN2_PRIORITY_PLLC	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x0639	6:4	R/W	IN3_PRIORTY_PLLC	The priority for clock input 3 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7 : Reserved

Table 14.184. Register 0x063A HOLD_REF_COUNT_FRC_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063A	1:0	R/W	HSW_MODE_PLLC	0: OL Logic decides whether to use only course or course plus fine phase measurement. Coarse plus fine is used only when switching in manual mode and inputs clock are valid. 1: Force coarse plus fine phas adjustment whether or not input clocks are valid. Input clock must be valid. 2: Use coarse measurement and adjustment only. 3: Same as 0

Note:
1. Optimizes the exit ramp when exiting Holdover.

Table 14.185. Register 0x063A-0x063B HSW_MODE_PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063A	7:0	R/W	HSW_MODE_PLLC	Calcuated by CBPro.
0x063B	9:8	R/W		

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.186. Register 0x063D Hitless Switching Length for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063D	4:0	R/W	HSW_COARSE_PM_LEN_PLLC	Calculated by CBPro.

Table 14.187. Register 0x063E Hitless Switching Delay for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x063E	4:0	R/W	HSW_COARSE_PM_DLY_PLLC	Caclulated in CBPro

Table 14.188. Register 0x063F DSPLL C Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x063F	1	R	HOLD_HIST_VALID_PLLC	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid

Table 14.189. Register 0x0689 and 0x068A PFD Enable Delay for PLLC

Reg Address	Bit Field	Type	Setting Name	Description
0x0689	7:0	R/W	PFD_EN_DLY_PLLC	Calculated by CBPro.
0x068A	12:8	R/W	PFD_EN_DLY_PLLC	

Table 14.190. Registers 0x069B, Exit from Holdover BW Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x069B	6	R/W	HOLDEXIT_BW_EN_PLLC	Set by CBPro. See HOLDEXIT_BW_SEL1_PLLA
0x069B	7	R/W	HOLDEXIT_STD_BO_PLLC	0: Normal fine phase adjustment 1: Skip fine phase adjustment

Table 14.191. Registers 0x069D- 0x006A2, Exit from Holdover BW Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x069D	5:0	R/W	BW0_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x069E	5:0	R/W	BW1_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x069F	5:0	R/W	BW2_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Reg Address	Bit Field	Type	Setting Name	Description
0x06A0	5:0	R/W	BW3_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x06A1	5:0	R/W	BW4_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.
0x06A2	5:0	R/W	BW5_HO_PLLC	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made.

Table 14.192. DSPLLC Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x06A6	3	R/W	Ramp_Switch_EN_PLLC	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover
0x06A6	2:0	R/W	RAMP_STEP_SIZE_PLLC	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made.

14.3.8 Page 7 Registers Si5383/84

Note that register addresses for Page 7 DSPLL D Registers 0x0709-0x074D are incremented relative to similar DSPLL A and C addresses on Pages 4 and 6. For example, Register 0x0709 has the equivalent function to Registers 0x0408/0x0608.

Table 14.193. Register 0x0702 ADD_DIV256_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0702	4	R/W	ADD_DIV256_PLLD	0: Standard Mode 1: 1PPS output mode

Note:
1. Additional divide-by required for a 1PPS outout.

Table 14.194. Register 0x0708 Active Input Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0708	2:0	R	IN_PLLD_ACTV	Current input clock

These bits indicate which input clock DSPLL D is currently selected. 0 for IN0; 1 for IN1, 2 for IN2, 3 Reserved, 4 for IN4, annd 5 for IN5.

Table 14.195. Register 0x0709-0x070E DSPLL D Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x0709	5:0	R/W	BW0_PLLD	Calculated by CBPro. *(Standard Input mode)*
0x070A	5:0	R/W	BW1_PLLD	
0x070B	5:0	R/W	BW2_PLLD	
0x070C	5:0	R/W	BW3_PLLD	
0x070D	5:0	R/W	BW4_PLLD	
0x070E	5:0	R/W	BW5_PLLD	

The loop Bandwidth values are calculated by ClockBuilder Pro and written into these registers.

Table 14.196. Register 0x070F-0x0715 DSPLL D Fast Lock Loop Bandwidth

Reg Address	Bit Field	Type	Setting Name	Description
0x070F	5:0	R/W	FAST_BW0_PLLD	Calculated by CBPro. *(Standard Input mode)*
0x0710	5:0	R/W	FAST_BW_1PLLD	
0x0711	5:0	R/W	FAST_BW2_PLLD	
0x0712	5:0	R/W	FAST_BW3_PLLD	
0x0713	5:0	R/W	FAST_BW_4PLLD	
0x0714	5:0	R/W	FAST_BW5_PLLD	
0x0715	0	S	BW_UPDATE_PLLD	0: No effect 1: Update both the Normal and Fastlock BWs for PLL D. *(Standard Input mode)*

The fast lock loop bandwidth values are calculated by ClockBuilder Pro and are written into these registers.

Table 14.197. Register 0x0716-0x071C MD Divider Numerator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x0716	7:0	R/W	M_NUM_PLLD	Calculated by CBPro
0x0717	15:8	R/W	M_NUM_PLLD	
0x0718	23:16	R/W	M_NUM_PLLD	
0x0719	31:24	R/W	M_NUM_PLLD	
0x071A	39:32	R/W	M_NUM_PLLD	
0x071B	47:40	R/W	M_NUM_PLLD	
0x071C	55:48	R/W	M_NUM_PLLD	

The MD divider numerator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.198. Register 0x071D-0x0720 MD Divider Denominator for DSPLL D

Reg Address	Bit Field	Type	Setting Name	Description
0x071D	7:0	R/W	M_DEN_PLLD	Calculated by CBPro.
0x071E	15:8	R/W	M_DEN_PLLD	
0x071F	23:16	R/W	M_DEN_PLLD	
0x0720	31:24	R/W	M_DEN_PLLD	

The loop MD divider denominator values are calculated by ClockBuilder Pro for a particular frequency plan and are written into these registers.

Table 14.199. Register 0x0721 M Divider Update Bit for PLL B

Reg Address	Bit Field	Type	Setting Name	Description
0x0721	0	S	M_UPDATE_PLLD	Must write a 1 to this bit to cause PLL D M divider changes to take effect.

Bits 7:1 of this register have no function and can be written to any value.

Table 14.200. Register 0x0722 M_FRAC_EN_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	4	R/W	M_FRAC_EN_PLLD	0: Interger mode 1: Enable fracn modulator

Note:

1. Bypass digital hold exit ramping when there is no valid history.

Table 14.201. Register 0x0722 M Divider Fractional Control and Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x0722	3:0	R/W	M_FRAC_MODE_PLLD	Managed by CBPro
0x0722	4	R/W	M_FRAC_EN_PLLD	M divider fractional Enable 0: Interger Mode 1: Enable Fractional modulator Will be enabled when in DCO mode

Table 14.202. Register 0x0723 DSPLL D FINC/FDEC Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0723	0	R/W	M_FSTEP_MSK_PLLD	0: To enable FINC/FDEC updates 1: To disable FINC/FDEC updates *(Standard Input mode)*
0x0723	1	R/W	M_FSTEP_DEN_PLLD	0: Modify Numerator 1: Modify Denominator

Table 14.203. Register 0x0724-0x072A DSPLLD MD Divider Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x0724	7:0	R/W	M_FSTEPW_PLLD	Calculated by CBPro *(Standard Input mode)*
0x0725	15:8	R/W	M_FSTEPW_PLLD	
0x0726	23:16	R/W	M_FSTEPW_PLLD	
0x0727	31:24	R/W	M_FSTEPW_PLLD	
0x0728	39:32	R/W	M_FSTEPW_PLLD	
0x0729	47:40	R/W	M_FSTEPW_PLLD	
0x072A	55:48	R/W	M_FSTEPW_PLLD	

The frequency step word (FSTEPW) for the feedback M divider of DSPLL D is always a positive integer. The FSTEPW value is either added to or subtracted from the feedback M divider Numerator such that an FINC will increase the output frequency and an FDEC will decrease the output frequency. See also Registers 0x0716-0x0720.

Table 14.204. Register 0x072B DSPLL D Input Clock Select

Reg Address	Bit Field	Type	Setting Name	Description
0x072B	2:0	R/W	IN_SEL_PLLD	0: For IN0 1: For IN1 2: For IN2 3: Reserved 4: For IN3 5: For IN4 6-7: Reserved

This is the input clock selection for manual register based clock selection. IN3 and IN4 are selected in manual mode only..

Table 14.205. Register 0x072C DSPLL D Fast Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072C	0	R/W	FASTLOCK_AUTO_EN_PLLD	Applies when FASTLOCK_MAN_PLLD=0. 0: To disable auto fast lock when PLLD is out of lock 1: To enable auto fast lock
0x072C	1	R/W	FASTLOCK_MAN_PLLD	0: For normal operation 1: For force fast lock

Table 14.206. Register 0x072E HOLD_RAMPBYP_NOHIST_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x072E	4	R/W	HOLD_RAMPBYP_NOHIST_PLLD	0: Disabled 1: Enabled

Note:
1. Bypass digital hold exit ramping when there is no valid history.

Table 14.207. Register 0x072D DSPLL D Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	0	R/W	HOLD_EN_PLLD	0: Holdover Disabled 1: Holdover Enabled. Standard setting. *(Standard Input mode)*

Reg Address	Bit Field	Type	Setting Name	Description
0x072D	3	R/W	HOLD_RAMP_BYP_PLLD	0: Use Ramp Rate when exiting from Holdover 1: Standard PLL configuration when exiting from Holdover *(Standard Input mode)*
0x072D	4	R/W	HOLD_EXITBW_SEL1_PLLD	This bit with HOLDEXIT_BW_SEL0_PLLA are set by CBPro to allow the bandwidth when exiting holdover to be set independent of the PLL bandwidth during other times of operation. CBPro sets this bit. *(Standard Input mode)*
0x072D	7:5	R/W	HOLD_RAMP_RATE_PLLD	The ramp rate is selected when using CBPro. *(Standard Input mode)*

Table 14.208. Register 0x072F DSPLL D Holdover History Average Length

Reg Address	Bit Field	Type	Setting Name	Description
0x072F	4:0	R/W	HOLD_HIST_LEN_PLLD	Calculated by CBPro. *(Standard Input mode)*

The holdover logic averages the input frequency over a period of time whose duration is determined by the history average length. The average frequency is then used as the holdover frequency. See Section 4.4.4 Holdover Mode to calculate the window length from the register value.

Table 14.209. Register 0x0730 DSPLLD Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x0730	4:0	R/W	HOLD_HIST_DELAY_PLLD	Calculated by CBPro. *(Standard Input mode)*

The most recent input frequency perturbations can be ignored during entry into holdover. The holdover logic pushes back into the past. The amount the average window is delayed is the holdover history delay. See Section 4.4.4 Holdover Mode to calculate the ignore delay time from the register value.

Table 14.210. Register 0x0732 HOLD_REF_COUNT_FRC_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0732	4:0	R/W	HOLD_REF_COUNT_FRC_PLLD	Calculated by CBPro

Note:
1. Holdover exit ramp optimzation.

Table 14.211. Register 0x0733 HOLD_15M_CYC_COUNT_PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0733	7:0	R/W	HOLD_15M_CYC_COUNT_PLLD	Calculated by CBPro
0x0733	15:8			
0x0733	23:16			

Note:
1. Sets up a time to wait before starting to measure the digital hold history.

Table 14.212. Register 0x0736 DSPLL D Force Holdover

Reg Address	Bit Field	Type	Setting Name	Description
0x0736	0	R/W	FORCE_HOLD_PLLD	0: For normal operation 1: To force holdover *(Standard Input mode)*

Table 14.213. Register 0x0737 DSPLLD Input Clock Switching Control

Reg Address	Bit Field	Type	Setting Name	Description
0x0737	1:0	R/W	CLK_SWITCH_MODE_PLLD	Clock Selection Mode 0: Manual 1: Automatic, non-revertive 2: Automatic, revertive 3: Reserved
0x0737	2	R/W	HSW_EN_PLLD	0: Glitchless switching mode (phase buildout turned off) 1: Hitless switching mode (phase buildout turned on)

The only way to use IN3 and IN4 is with manual register based clock selection.

Table 14.214. Register 0x0738 DSPLLD Input Alarm Masks

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	3:0	R/W	IN_LOS_MSK_PLLD	For each clock input LOS alarm 0: To use LOS in the clock selection logic 1: To mask LOS from the clock selection logic

Reg Address	Bit Field	Type	Setting Name	Description
0x0738	7:4	R/W	IN_OOF_MSK_PLLD	For each clock input OOF alarm 0: To use OOF in the clock selection logic 1: To mask OOF from the clock selection logic

For each of the four clock inputs the OOF and/or the LOS alarms can be used for the clock selection logic or they can be masked from it. Note that the clock selection logic can affect entry into holdover.

IN0 Input 0 applied to LOS alarm 0x0738[0], OOF alarm 0x0738[4]

IN1 Input 1 applied to LOS alarm 0x0738[1], OOF alarm 0x0738[5]

IN2 Input 2 applies to LOS alarm 0x0738[2], OOF alarm 0x0738[6]

Table 14.215. Register 0x0739 DSPLL D Clock Inputs 0 and 1 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x0739	2:0	R/W	IN0_PRIORITY_PLLD	The priority for clock input 0 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7: Reserved
0x0739	6:4	R/W	IN1_PRIORITY_PLLD	The priority for clock input 1 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4-7: Reserved

Clock input priorities are used only when the clock switch mode is automatic.

Table 14.216. Register 0x073A DSPLL D Clock Inputs 2 and 3 Priority

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	2:0	R/W	IN2_PRIORITY_PLLD	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Reg Address	Bit Field	Type	Setting Name	Description
0x073A	6:4	R/W	IN3_PRIORITY_PLLD	The priority for clock input 2 is: 0: Clock input not selected 1: For priority 1 2: For priority 2 3: For priority 3 4: For priority 4 5-7: Reserved

Table 14.217. Register 0x073B and 0x073C Hitless Switching Phase Threshold for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x073B	7:0	R/W	HSW_PHMEAS_THR_PLLD	Calculated by CBPro.

Table 14.218. Register 0x073D Hitless Switching Length for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x073D	4:0	R/W	HSW_COARSE_PM_LEN_PLLD	Calculated by CBPro.

Table 14.219. Register 0x073E Hitless Switching Delay for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x073E	4:0	R/W	HSW_COARSE_PM_DLY_PLLD	Calculated by CBPro.

Table 14.220. Register 0x0740 DSPLL D Hold Valid History and Fastlock Status

Reg Address	Bit Field	Type	Setting Name	Description
0x0740	1	R	HOLD_HIST_VALID_PLLD	Holdover historical frequency data is valid and indicates if there is enough historical history data collected for a valid holdover value. 0: Not valid 1: Valid
0x0740	2	R	FASTLOCK_STATUS_PLLD	0: Not in Fastlock 1: Fastlock active

Table 14.221. Register 0x0788 Hitless Switching Length, Fine Adjust, for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0788	3:0	R/W	HSW_FINE_PM_LEN_PLLD	Calculated by CBPro.

Table 14.222. Register 0x0789 and 0x078A PFD Enable Delay for PLLD

Reg Address	Bit Field	Type	Setting Name	Description
0x0789	7:0	R/W	PFD_EN_DLY_PLLD	Caclulated in CBPro.
0x078A	3:0	R/W	PFD_EN_DLY_PLLD	

Table 14.223. Registers 0x079B, Exit from Holdover BW Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x079B	6	R/W	HOLDEX-IT_BW_EN_PLLD	Managed by CBPro. See HOLDEX-IT_BW_SEL1_PLLA

Table 14.224. Registers 0x079D- 0x07A2, Exit from Holdover BW Selection

Reg Address	Bit Field	Type	Setting Name	Description
0x079D	5:0	R/W	BW0_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*
0x079E	5:0	R/W	BW1_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*
0x079F	5:0	R/W	BW2_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*
0x07A0	5:0	R/W	BW3_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*
0x07A1	5:0	R/W	BW4_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*
0x07A2	5:0	R/W	BW5_HO_PLLD	The exit from holdover bandwidth is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*

Table 14.225. DSPLLD Exit from Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x07A6	3	R/W	Ramp_Switch_EN_PLLD	0: Disables a ramp upon exit from Holdover 1: Enables a ramp upon exit from Holdover *(Standard Input mode*)

Reg Address	Bit Field	Type	Setting Name	Description
0x07A6	2:0	R/W	RAMP_STEP_SIZE_PLLD	The ramp rate is selected when using CBPro, these register values are calculated based on the selections made. *(Standard Input mode)*

Table 14.226. Register 0x07AA PLLD Clock Input Control

Reg Address	Bit Field	Type	Setting Name	Description
0x07AA	0	R/W	CONFIG3_CMOS_PLLD	0:Normal Selection 1: Replace input selection with CONFIG2_CMOS_PLLD
0x07AA	1	R/W	CONFIG2_CMOS_PLLD	0: IN3 1: IN4
0x07AA	2	R/W	CONFIG1_CMOS_PLLD	0: standard IN0, IN1, IN3 1: Override with value selected in CONFIG2_CMOS_PLLD
0x07AA	5:4	R/W	CONFIG0_CMOS_PLLD	00: Replace IN0 with IN3/IN4 not selected by CONFIG2_CMOS_PLLD 01: Replace IN1 with IN3/IN4 not selected by CONFIG2_CMOS_PLLD 10:Replace IN2 with IN3/IN4 not selected by ONFIG2_CMOS_PLLD 11: Reserved

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Table 14.227. Register 0x090E XAXB Configuration

Reg Address	Bit Field	Type	Name	Description
0x090E	0	R/W	XAXB_EXTCLK_EN	This bit selects between the Crystal or External reference clock on the XAXB pins. 0: Crystal on XAXB, enable internal XO (default) 1: External XAXB signal, internal XO disabled
0x090E	1	R/W	XAXB_XO_EN	Powerdown the built-in low noise crystal oscillator when using an external reference input. 0: Powerdown Internal Oscillator 1: Internal Oscillator Powered (default) - required when using a crystal with the XAXB input.

Table 14.228. Register 0x0943 Control I/O Voltage Select

Reg Address	Bit Field	Type	Setting Name	Description
0x0943	0	R/W	IO_VDD_SEL	0: For 1.8 V external connections 1: For 3.3 V external connections

Table 14.229. Register 0x0949 Clock Input Control and Configuration

Reg Address	Bit Field	Type	Setting Name	Description
0x0949	3:0	R/W	IN_EN	0: Disable and Powerdown Input Buffer 1: Enable Input Buffer for Ref, IN2, IN1 and IN0.
0x0949	7:4	R/W	IN_PULSED_CMOS_EN	0: Standard Input Format 1: Pulsed CMOS Input Format for IN2, IN1 and IN0.

When a clock is disabled, it is powered down.

- Input 0 corresponds to IN_EN 0x0949 [0], IN_PULSED_CMOS_EN 0x0949 [4]
- Input 1 corresponds to IN_EN 0x0949[1], IN_PULSED_CMOS_EN 0x0949[5]
- Input 2 corresponds to IN_EN 0x0949[2], IN_PULSED_CMOS_EN 0x0949[6]
- Input 3 (Reference) corresponds to IN_EN 0x0949[3]

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Table 14.230. Register 0x0A03 Enable DSPLL Internal Divider Clocks

Reg Address	Bit Field	Type	Setting Name	Description
0x0A03	3:0	R/W	N_CLK_TO_OUTX_EN	Enable the internal dividers for PLLs (D C B A). Must be set to 1 to enable the dividers. See related registers 0x0A05 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.231. Register 0x0A04 DSPLL Internal Divider Integer Force

Reg Address	Bit Field	Type	Setting Name	Description
0x0A04	3:0	R/W	N_PIBYP	Bypass the fractional part of the internal divider for PLLs (D C B A). Set to a 1 when the value is integer, as this may give slightly lower phase noise. May be set to 0 when the value is either fractional or integer. Will be set by CBPro when in fractional/DCO mode.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.232. Register 0x0A05 DSPLL Internal Divider Power Down

Reg Address	Bit Field	Type	Setting Name	Description
0x0A05	3:0	R/W	N_PDNB	Powers down the internal dividers for PLLs (D C B A). Set to 0 to power down unused PLLs. Must be set to 1 for all active PLLs. See related registers 0x0A03 and 0x0B4A[4:0].

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Table 14.233. Register 0x0B24 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B24	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See Section 4.2 Changing Registers while Device in Operation for more information.

Table 14.234. Register 0x0B25 Reserved Control

Reg Address	Bit Field	Type	Name	Description
0x0B25	7:0	R/W	RESERVED	Reserved

This register is used when making certain changes to the device. See Section 4.2 Changing Registers while Device in Operation for more information.

Table 14.235. Register 0x0B2E Global OD Timeout

Reg Address	Bit Field	Type	Setting Name	Description
0x0B2E	6:0	R/W	GLOBAL_OD_TIME-OUT	Calcuated by CBPro.

Table 14.236. Register 0x0B44 IN0/1/2 Input P divider fractional clock disable

Reg Address	Bit Field	Type	Setting Name	Description
0x0B44	3:0	R/W	PDIV_FRACn_CLK_DIS	0: Enabled 1: Disabled
Note: 1. Enables/Disables fractional mode on IN0/1/2.				

Table 14.237. Register 0x0B45 Clock Disable PLLA/B/C/D

Reg Address	Bit Field	Type	Setting Name	Description
0x0B45	0	R/W	CLK_DIS_PLLA	Calculated set by CBPro.
0x0B45	1	R/W	CLK_DIS_PLLB	
0x0B45	2	R/W	CLK_DIS_PLLC	
0x0B45	3	R/W	CLK_DIS_PLLD	

Table 14.238. Register 0x0B44 M Divider Fractional Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B44	7:4	R/W	M_FRACN_CLK_DIS_PLLx	M divider fractional clock disable

When a DSPLL is in DCO mode, its corresponding clock disable bit should be cleared.

If DSPLLA is in DCO mode, 0x0B44[4] should be zero.

If DSPLLC is in DCO mode, 0x0B44[6] should be zero.

If DSPLLD is in DCO mode, 0x0B44[7] should be zero.

Table 14.239. Register 0x0B46 Loss of Signal Clock Disable

Reg Address	Bit Field	Type	Name	Description
0x0B46	3:0	R/W	LOS_CLK_DIS	Disables LOS for (REF, IN2, IN1, IN0). Must be set to 0 to enable the LOS function of the respective inputs.
0x0B46	5:4	R/W	LOS_CMOS_CLK_DIS	Disables LOS for IN3 and IN4. Must be set to 0 to enable the LOS function of the respective inputs.

Table 14.240. 0x0B47 Digital OOF, User Disable.

Reg Address	Bit Field	Type	Setting Name	Description
0x0B47	4:0	R/W	OOF_CLK_DIS	Calculated by CBPro

Table 14.241. 0x0B48 Digital OOF, Divided, User Disable.

Reg Address	Bit Field	Type	Setting Name	Description
0x0B48	4:0	R/W	OOF_DIV_CLK_DIS	Calculated by CBPro

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed whhen changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.242. Register 0x0B49 Calibration Bits

Reg Address	Bit Field	Type	Name	Description
0x0B49	1:0	R/W	CAL_DIS	Must be 0 for normal operation.
0x0B49	3:2	R/W	CAL_FORCE	Must be 0 for normal operation.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

Table 14.243. Register 0x0B4A Divider Clock Disables

Reg Address	Bit Field	Type	Name	Description
0x0B4A	4:0	R/W	N_CLK_DIS	Disable internal dividers for PLLs. Must be set to 0 to use the DSPLL. See related registers 0x0A03 and 0x0A05.
0x0B4A	5	R/W	M_CLK_DIS	Disable M dividers. Must be set to 0 to enable the M divider.
0x0B4A	6	R/W	M_DIV_CAL_DIS	Disable M divider calibration. Must be set to 0 to allow calibration.

ClockBuilder Pro handles these bits when changing settings for all portions of the device. This control bit is only needed when changing the settings for only a portion of the device while the remaining portion of the device operates undisturbed.

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Table 14.244. Registers 0x0D11-0x0D20

Reg Address	Bit Field	Type	Setting Name	Description
0x0D11	7:0	R/W	PFD_TRM_PLLA	Calcuated by CBPro.
0x0D12	15:8			
0x0D13	23:16			
0x0D14	24			
0x0D15	7:0	R/W	PFD_TRM_PLLB	Calcuated by CBPro.
0x0D16	15:8			
0x0D17	23:16			
0x0D18	24			
0x0D19	7:0	R/W	PFD_TRM_PLLC	Calcuated by CBPro.
0x0D1A	15:8			
0x0D1B	23:16			
0x0D1C	24			
0x0D1D	7:0	R/W	PFD_TRM_PLLD	Calcuated by CBPro.
0x0D1E	15:8			
0x0D1F	23:16			
0x0D20	24			

14.3.13 Page 53 Registers Si5383/84, 1 PPS Mode

Table 14.245. Register 0x5300 and 0x5301 Firmware Revision

Reg Address	Bit Field	Type	Setting Name	Description
0x5300	7:4	R	FIRMWARE_TYPE	Firmware Type 0 = Production
0x5300	3:0	R	FIRMWARE_MAJOR_REV	Major Firmware Revision
0x5301	7:0	R	FIRMWARE_MINOR_REV	Minor Firmware Revision

Table 14.246. Register 0x5302 I^2C Address

Reg Address	Bit Field	Type	Setting Name	Description
0x5302	6:0	R/W	I2C_ADDR	7-bit I^2C Address

Table 14.247. Register 0x5303 Hard Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x5303	0	R/W	HARD_RST	1 = Reset Asserted 0 = Reset Negated This bit returns to 0 during recovery from reset.

Table 14.248. Register 0x5304 Hard Reset Flag

Reg Address	Bit Field	Type	Setting Name	Description
0x5304	0	R/W	HARD_RST_FLG	Sticky version of HARD_RST Write 0 to clear this bit

Table 14.249. Register 0x5305 Bootloader Reset

Reg Address	Bit Field	Type	Setting Name	Description
0x5305	7:0	R/W	BOOT_RST	Writing 0x57 followed by 0xBA to this register triggers a reset into bootloader mode.

Other regsiters may be accessed between the two writes without impacting operation. Any value written other than the expected value returns the state machine back to the initial state.

Table 14.250. 0x5306-0x5307 Firmware Build Number

Reg Address	Bit Field	Type	Setting Name	Description
0x5306	15:8	R	Firmware Build	Firmware Build Number
0x5307	7:0	R	Firmware Build	

Table 14.251. Registers 0x5308-0x530F Scratch Pad

Reg Address	Bit Field	Type	Setting Name	Description
0x5308	7:0	R/W	Scratch Pad	Read/Write location that can be used to verify operation of the I2C interface.
0x5309	7:0	R/W		
0x530A	7:0	R/W		
0x530B	7:0	R/W		
0x530C	7:0	R/W		
0x530D	7:0	R/W		
0x530E	7:0	R/W		
0x530F	7:0	R/W		

14.3.14 Page 53 PPS Loop Registers Si5383/84

Note: These registers apply to PPS Mode only.

Table 14.252. Register 0x5320 PPS Loop Initial Acquisition Type and PPS Mode Enable

Reg Address	Bit Field	Type	Setting Name	Description
0x5320	6	R/W	INIT_LCKB_DIS	0: When cleared, PPS acquisituion waits for the reference loop to lock before proceeding.
0x5320	4	R/W	INIT_ACQ_TYPE	Initial acquisition type. Determines the acquisition mode when PPS is first enabled. 0: Smart Lock Mode A 1: Smart Lock Mode B
0x5320	0	R/W	PPS_EN	0: PPS Mode Disabled 1: PPS Mode Enabled

Table 14.253. Register 0x5321 PPS Holdover Valid

Reg Address	Bit Field	Type	Setting Name	Description
0x5321	0	R	HOLD_HIST_VALID	0 = Holdover logic has not acquired adequate data for calculation. 1 = Holdover logic has aquired adequete data for calculation.

Table 14.254. Register 0x5322 PPS Event

Reg Address	Bit Field	Type	Setting Name	Description
0x5322	7	R/W	DCO_OF_FLG	Sticky indication that a DCO accumulator overflow has occurred. 0: Normal Operation. 1: Overflow occurred. Write 0 to this bit to clear.
0x5322	6	R/W	DCO_UF_FLG	Sticky indication that a DCO accumulator underflow has occurred. 0: Normal Operation. 1: Underflow Occurred. Write 0 to this bit to clear.

Reg Address	Bit Field	Type	Setting Name	Description
0x5322	4	R/W	RL_ERR_FLG	Sticky indication that phase error exceeded threshold on RapidLock exit. 0: Normal Operation. 1: Phase Error Exceeded Threshold. Write 0 to this bit to clear.
0x5322	3	R/W	PP_ERR_FLG	Sticky indication that phase error exceeded threshold following phase pull. 0: Normal Operation. 1: Phase Error Exceeded Threshold. Write 0 to this bit to clear.
0x5322	2	R/W	PP_OOR_FLG	Sticky indication that initial PPS phase error was out-of-range. 0: Normal Operation. 1: PPS Input is Out of Range. Write 0 to this bit to clear.
0x5322	1	R/W	FP_ERR_FLG	Sticky indication that frequency error exceeded threshold following frequency pull. 0: Normal Operation. 1: Frequency Error Exceeded Thershold. Write 0 to this bit to clear.
0x5322	0	R/W	FP_OOR_FLG	Sticky indication that initial PPS frequency error was out-of-range. 0: Normal Operation. 1: PPS Input is Out of Range. Write 0 to this bit to clear.

Table 14.255. Register 0x5323 PPS LOS Status

Reg Address	Bit Field	Type	Setting Name	Description
0x5323	4	R/W	LOS_PPS_FLG	Sticky version of LOS_PPS Write a 0 to this bit to clear

Reg Address	Bit Field	Type	Setting Name	Description
0x5323	0	R	LOS_PPS	0: Normal Operation 1: LOS on the selected PPS Input

Table 14.256. Register 0x5324 Holdover, LOL and LOT

Reg Address	Bit Field	Type	Setting Name	Description
0x5324	7	R/W	HOLD_FLG	Sticky version of Hold Write 0 to this bit to clear
0x5324	5	R/W	LOL_FLG	Sticky version of LOL Write 0 to clear this bit
0x5324	4	R/W	LOT_FLG	Sticky version of LOT Write 0 to clear this bit
0x5324	3	R	HOLD	Holdover State - Indicates holdover status 0 = Normal Operation 1 = Holdover
0x5324	1	R	LOL	0 = PLL Locked 1 = PLL Unlocked
0x5324	0	R	LOT	0 = PLL Tracking 1 = PLL Not Tracking

Table 14.257. Register 0x5330 LOS Control

Reg Address	Bit Field	Type	Setting Name	Description
0x5330	3	R/W	LOS_EN	Loss-of-Signal Enable - Enables the Si5383 LOS detector. 0 = Si5383/84 LOS Disabled 1 = Si5383/84 LOS Enabled
0x5330	1	R/W	LOS_EXT_EN	External Loss-of-Signal Enable - Enables an external device to control the LOS status via the I^2C I/F 0 = External LOS Disabled 1 = External LOS Enabled
0x5330	0	R/W	LOS_EXT	External Loss-of-Signal Control 0 = External LOS Negated 1 = External LOS Asserted

Table 14.258. Register LOS trigger count

Reg Address	Bit Field	Type	Setting Name	Description
0x5331	7:0	R/W	LOS_TRG_CNT	Calculated by CBPro.

Note:

1. Loss-of-Signal Trigger Count - The number of consecutive polls the input signal must be seen invalid before the LOS alarm is raised. Must be set before PPS_EN.

Table 14.259. Register LOS clear count

Reg Address	Bit Field	Type	Setting Name	Description
0x5332	7:0	R/W	LOS_CLR_CNT	Calculated by CBPro.

Note:

1. The number of consecutive polls the input signal must be seen valid before the LOS alarm is cleared. Must be set before PPS_EN.

Table 14.260. Register 0x5340 Loss of Lock Control

Reg Address	Bit Field	Type	Setting Name	Description
0x5340	5:4	R/W	LOL_ACQ_TYPE	LOL acquisition type. Determines the acquisition mode when LOL occurs. 00 = SmartLock Mode A 01 = SmartLock Mode B 1x = Normal Lock

Table 14.261. 0x5341 Loss of Tracking Holdoff Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5341	7:0	R/W	LOT_HO_CNT	The number of polls after LOT is asserted before reacquistion occurs 00h = 1 poll 01h = 2 polls FFh= 256 polls

Table 14.262. Register 0x5342-0x5343 LOL Trigger Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5342	15:8	R/W	LOL_TRG_CNT	The number of consecutive polls the trigger threshold is exceeded before the LOl alarm is raised. 16h'0000 = 1 poll 16h'0001 = 2 polls …. 16h'FFFF= 65536 Polls
0x5343	7:0	R/W	LOL_TRG_CNT	

Table 14.263. Register 0x5344-0x5345 LOL Clear Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5344	15:8	R/W	LOL_CLR_CNT	The number of consecutive polls the clear threshold is not exceeded before LOL alarm is cleared. 16h'0000 = 1 poll 16h'0001 = 2 polls …. 16h'FFFF= 65536 Polls
0x5345	7:0	R/W	LOL_CLR_CNT	

Table 14.264. Register 0x5348-0x534B Loss of Lock Trigger Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x5348	29:24	R/W	LOL_TRG_THR	LOL Trigger Threshold. Calculated by CBPro.
0x5349	23:16	R/W	LOL_TRG_THR	
0x534A	15:8	R/W	LOL_TRG_THR	
0x534B	7:0	R/W	LOL_TRG_THR	

Table 14.265. Register 0x534C-0x534F Loss of Lock Clear Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x534C	29:24	R/W	LOL_CLR_THR	LOL Clear Threshold. Calculated by CBPro.
0x534D	23:16	R/W	LOL_CLR_THR	
0x534E	15:8	R/W	LOL_CLR_THR	
0x534F	7:0	R/W	LOL_CLR_THR	

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Table 14.266. Register 0x5350-0x5353 DCO Frequency Step Word

Reg Address	Bit Field	Type	Setting Name	Description
0x5350	30:24	R/W	DCO_FSTEPW	DCO Frequency Step Word. Calculated by CBPro.
0x5351	23:16	R/W	DCO_FSTEPW	
0x5352	15:8	R/W	DCO_FSTEPW	
0x5353	7:0	R/W	DCO_FSTEPW	

Table 14.267. 0x5354 DCO Frequency Step Command, 1PPS Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x5354	1:0	R/W	DCO_FSTEPW_CMD	DCO Frequency Step Command: 00 = Idle 01 = Increment 10 = Decrement 11 = Reset FSW Accumulator

Table 14.268. 0x5358 DCO Scale

Reg Address	Bit Field	Type	Setting Name	Description
0x5358	2:0	R/W	DCO_SCALE	Calculated by CBPro.

Table 14.269. 0x535C-0x535F Phase Pull Control Word Limit

Reg Address	Bit Field	Type	Setting Name	Description
0x535C	31:24	R/W	PP_CW_LMT	Calculated by CBPro.
0x535D	23:16	R/W	PP_CW_LMT	
0x535E	15:8	R/W	PP_CW_LMT	
0x535F	7:0	R/W	PP_CW_LMT	

Table 14.270. Register 0x5360-0x5363 Phase Detector Adjustment

Reg Address	Bit Field	Type	Setting Name	Description
0x5360	31:24	R/W	PD_ADJ	Phase Detector Adjustment. Calculated by CBPro
0x5361	23:16	R/W	PD_ADJ	
0x5362	15:8	R/W	PD_ADJ	
0x5363	7:0	R/W	PD_ADJ	

Table 14.271. Register 0x5364-0x5367 Phase Detector Control Word to Adjustment Conversion

Reg Address	Bit Field	Type	Setting Name	Description
0x5364	31:24	R/W	PD_CW_2_ADJ	Calculated by CBPro.
0x5365	23:16	R/W	PD_CW_2_ADJ	
0x5366	15:8	R/W	PD_CW_2_ADJ	
0x5367	7:0	R/W	PD_CW_2_ADJ	

Table 14.272. Register 0x5368-0x536B SmartLock Period to Adjustment Conversion

Reg Address	Bit Field	Type	Setting Name	Description
0x5368	31:24	R/W	SL_PER_2_ADJ	Calculated by CBPro.
0x5369	23:16	R/W	SL_PER_2_ADJ	
0x536A	15:8	R/W	SL_PER_2_ADJ	
0x536B	7:0	R/W	SL_PER_2_ADJ	

Table 14.273. Register 0x536C-0x536F SmartLock Phase Error to Adjustment Conversion

Reg Address	Bit Field	Type	Setting Name	Description
0x536C	31:24	R/W	SL_PE_2_ADJ	Calculated by CBPro.
0x536D	23:16	R/W	SL_PE_2_ADJ	
0x536E	15:8	R/W	SL_PE_2_ADJ	
0x536F	7:0	R/W	SL_PE_2_ADJ	

Table 14.274. 0x5371 Smart Lock Frequency Average Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5371	7:0	R/W	SLA_FA_CNT	Calculated by CBPro.

Table 14.275. 0x5372 SmartLock Frequency Pull Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x5372	2:0	R/W	SLA_FP_NCYC	Calculated by CBPro.

Table 14.276. 0x5373 SmartLock Frequency Pull Validation Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5373	7:0	R/W	SLA_FP_VAL_CNT	Calculated by CBPro.

Table 14.277. Register 0x5374-0x5377 SmartLock Frequency Error Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x5374	30:24	R/W	SLA_FE_THR	Calculated by CBPro.
0x5375	23:16	R/W	SLA_FE_THR	
0x5376	15:8	R/W	SLA_FE_THR	
0x5377	7:0	R/W	SLA_FE_THR	

Table 14.278. 0x5378 SmartLock Phase Pull 1 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x5378	4:0	R/W	SLA_PP1_NCYC	Calculated by CBPro.

Table 14.279. 0x5379 SmartLock_A Phase Pull 2 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x5379	4:0	R/W	SLA_PP2_NCYC	Calculated by CBPro..

Table 14.280. 0x537A SmartLock_A Phase Pull 3 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537A	4:0	R/W	SLA_PP3_NCYC	Calculated by CBPro.

Table 14.281. 0x537B SmartLock_A Phase Pull 4 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537B	4:0	R/W	SLA_PP4_NCYC	Calculated by CBPro.

Table 14.282. 0x537C SmartLock_A Phase Pull 5 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537C	4:0	R/W	SLA_PP5_NCYC	Calculated by CBPro.

Table 14.283. 0x537D SmartLock_A Phase Pull 6 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537D	4:0	R/W	SLA_PP6_NCYC	Calculated by CBPro.

Table 14.284. 0x537E SmartLock_A Phase Pull 7 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537E	4:0	R/W	SLA_PP7_NCYC	Calculated by CBPro.

Table 14.285. 0x537F SmartLock_A Phase Pull 8 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x537F	4:0	R/W	SLA_PP8_NCYC	Calculated by CBPro.

Table 14.286. Register 0x5380-0x5383 SmartLock_A Phase Error Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x5380	29:24	R/W	SLA_PE_THR	Calculated by CBPro.
0x5381	23:16	R/W	SLA_PE_THR	
0x5382	15:8	R/W	SLA_PE_THR	
0x5383	7:0	R/W	SLA_PE_THR	

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Table 14.287. 0x5384 SmartLock_A RapidLock1 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x5384	4:0	R/W	SLA_RL1_NF	Calculated by CBPro.

Table 14.288. 0x5385 SmartLock_A RapidLock1 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x5385	4:0	R/W	SLA_RL1_NI	Calculated by CBPro.

Table 14.289. 0x5386-0x5387 SmartLockA_RapidLock1_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5386	15:8	R/W	SLA_RL1_CNT	Calculated by CBPro.
0x5387	7:0	R/W	SLA_RL1_CNT	

Table 14.290. 0x5388 SmartLock_A RapidLock2 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x5388	3:0	R/W	SLA_RL2_NF	Calculated by CBPro.

Table 14.291. 0x5389 SmartLock_A RapidLock2 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x5389	4:0	R/W	SLA_RL2_NI	Calculated by CBPro.

Table 14.292. 0x538A-0x538B SmartLockA_RapidLock2_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x538A	15:8	R/W	SLA_RL2_CNT	Calculated by CBPro.
0x538B	7:0	R/W	SLA_RL2_CNT	

Table 14.293. 0x538C SmartLock_A RapidLock3 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x538C	3:0	R/W	SLA_RL3_NF	Calculated by CBPro.

Table 14.294. 0x538D SmartLock_A RapidLock3 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x538D	4:0	R/W	SLA_RL3_NI	Calculated by CBPro.

Table 14.295. 0x538E-0x538F SmartLockA_RapidLock3_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x538E	15:8	R/W	SLA_RL3_CNT	Calculated by CBPro.
0x538F	7:0	R/W	SLA_RL3_CNT	

Table 14.296. 0x5390 Smart Lock Rapid Lock NF, 1PPS Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x5390	3:0	R/W	SLA_RL4_NF	Calculated by CBPro.

Table 14.297. 0x5391 Smart Lock Rapid Lock NI, 1PPS Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x5391	4:0	R/W	SLA_RL4_NI	Calculated by CBPro.

Table 14.298. 0x5392-0x5393 SmartLockA_RapidLock4_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x5392	15:8	R/W	SLA_RL4_CNT	Calculated by CBPro
0x5393	7:0	R/W	SLA_RL4_CNT	

Table 14.299. 0x53A1 SmartLock B Frequency Average Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53A1	7:0	R/W	SLB_FA_CNT	Calculated by CBPro

Table 14.300. 0x53A2 SmartLock B Frequency Pull Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53A2	2:0	R/W	SLB_FP_NCYC	Calculated by CBPro

Table 14.301. 0x53A3 SmartLock_B Frequency Pull Validation Count

Reg Address	Bit Field	Type	Setting Name	Description
0x53A3	7:0	R/W	SLB_FP_VAL_CNT	Calculated by CBPro

Table 14.302. Register 0x53A4-0x53A7 SmartLock_B Frequency Error Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x53A4	30:24	R/W	SLB_FE_THR	Calculated by CBPro
0x53A5	23:16	R/W	SLB_FE_THR	
0x53A6	15:8	R/W	SLB_FE_THR	
0x53A7	7:0	R/W	SLB_FE_THR	

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Table 14.303. 0x53A8 SmartLock_B Phase Pull 1 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53A8	4:0	R/W	SLB_PP1_NCYC	Calculated by CBPro

Table 14.304. 0x53A9 SmartLock_B Phase Pull 2 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53A9	4:0	R/W	SLB_PP2_NCYC	Calculated by CBPro

Table 14.305. 0x53AA SmartLock_B Phase Pull 3 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AA	4:0	R/W	SLB_PP3_NCYC	Calculated by CBPro

Table 14.306. 0x53AB SmartLock_B Phase Pull 4 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AB	4:0	R/W	SLB_PP4_NCYC	Calculated by CBPro

Table 14.307. 0x53AC SmartLock_B Phase Pull 5 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AC	4:0	R/W	SLB_PP5_NCYC	Calculated by CBPro

Table 14.308. 0x53AD SmartLock_B Phase Pull 6 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AD	4:0	R/W	SLB_PP6_NCYC	Calculated by CBPro

Table 14.309. 0x53AE SmartLock_B Phase Pull 7 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AE	4:0	R/W	SLB_PP7_NCYC	Calculated by CBPro

Table 14.310. 0x53AF SmartLock_B Phase Pull 8 Cycles

Reg Address	Bit Field	Type	Setting Name	Description
0x53AF	4:0	R/W	SLB_PP8_NCYC	Calculated by CBPro

Table 14.311. Register 0x53B0-0x53B3 SmartLock_B Phase Error Threshold

Reg Address	Bit Field	Type	Setting Name	Description
0x53B0	29:24	R/W	SLB_PE_THR	Calculated by CBPro
0x53B1	23:16	R/W	SLB_PE_THR	
0x53B2	15:8	R/W	SLB_PE_THR	
0x53B3	7:0	R/W	SLB_PE_THR	

Table 14.312. 0x53B4 SmartLock_B RapidLock1 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x53B4	3:0	R/W	SLB_RL1_NF	Calculated by CBPro

Table 14.313. 0x53B5 SmartLock_B RapidLock1 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x53B5	4:0	R/W	SLB_RL1_NI	Calculated by CBPro

Table 14.314. 0x53B6-0x53B7 Smartlock_B_RapidLock1_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x53B6	15:8	R/W	SLB_RL1_CNT	Calculated by CBPro
0x53B7	7:0	R/W	SLB_RL1_CNT	

Table 14.315. 0x53B8 SmartLock_B RapidLock2 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x53B8	3:0	R/W	SLB_RL2_NF	Calculated by CBPro

Table 14.316. 0x53B9 SmartLock_B RapidLock2 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x53B9	4:0	R/W	SLB_RL2_NI	Calculated by CBPro

Table 14.317. 0x53BA-0x53BB SmartLock_B_RapidLock2_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x53BA	15:8	R/W	SLB_RL2_CNT	Calculated by CBPro
0x53BB	7:0	R/W	SLB_RL2_CNT	

Table 14.318. 0x53BC SmartLock_B RapidLock3 NF

Reg Address	Bit Field	Type	Setting Name	Description
0x53BC	3:0	R/W	SLB_RL3_NF	Calculated by CBPro

Table 14.319. 0x53BD SmartLock_B RapidLock3 NI

Reg Address	Bit Field	Type	Setting Name	Description
0x53BD	4:0	R/W	SLB_RL3_NI	Calculated by CBPro

Table 14.320. 0x53BE-0x53BF SmartLock_B_RapdiLock3_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x53BE	15:8	R/W	SLB_RL3_CNT	Calculated by CBPro
0x53BF	7:0	R/W	SLB_RL3_CNT	

Table 14.321. 0x53C0 Smart Lock Rapid Lock NF

Reg Address	Bit Field	Type	Setting Name	Description
0x53C0	3:0	R/W	SLB_RL4_NF	Calculated by CBPro

Table 14.322. 0x53C1 Smart Lock NI

Reg Address	Bit Field	Type	Setting Name	Description
0x53C1	3:0	R/W	SLB_RL4_NI	Calculated by CBPro

Table 14.323. 0x53C2-0x53C3 SmartLock_B_RapidLock4_Count

Reg Address	Bit Field	Type	Setting Name	Description
0x53C2	15:8	R/W	SLB_RL4_CNT	Calculated by CBPro
0x53C3	7:0	R/W	SLB_RL4_CNT	

Table 14.324. 0x53D1 NormalLock NF

Reg Address	Bit Field	Type	Setting Name	Description
0x53D1	3:0	R/W	NL_NF	Calculated by CBPro

Table 14.325. 0x53D2 NormalLock NI

Reg Address	Bit Field	Type	Setting Name	Description
0x53D2	4:0	R/W	NL_NI	Calculated by CBPro

Table 14.326. 0x53E0 Holdover Control

Reg Address	Bit Field	Type	Setting Name	Description
0x53E0	5:4	R/W	HO_ACQ_TYPE	Holdover acquisition type. Determines the acquisition mode when holdover is exited. 0 = SmartLock Mode A 1 = SmartLock Mode B 10 and 11: Normal Mode

Reg Address	Bit Field	Type	Setting Name	Description
0x53E0	1	R/W	FORCE_HOLD	When asserted, the PPS loop will transition from FREERUN or LOCKED status into the HOLD-OVER state. It will remain in this state until the force is removed. 0 = Normal Operation 1 = Force Holdover
0x53E0	0	R/W	HO_EXIT_EN	When enabled, HOLDOVER will automatically exit and attempt reacquisition when a valid input is detected. When disabled, FORCE_HOLD will be set on entry into HOLDOVER and must be manually cleared to exit the HOLD-OVER state. 0 = Holdover Exit Disabled 1 = Holdover Exit Enabled

Table 14.327. 0x53E1 Holdover History Length

Reg Address	Bit Field	Type	Setting Name	Description
0x53E1	2:0	R/W	HOLD_HIST_LEN	000 = 1 samples 001 = 2 samples 010 = 4 samples 011 = 8 samples 1xx = 16 samples Value calculated by CBPro based on value of selected.

Table 14.328. 0x53E2 Holdover History Delay

Reg Address	Bit Field	Type	Setting Name	Description
0x53E2	4:0	R/W	HOLD_HIST_DELAY	00000 = 0 samples 00001 = 1 sample 01111 = 15 samples 10000 = 16 samples Calculated by CBPro based on value of selected.

14.3.15 Page 54 Phase Readout Registers Si5383/84, 1PPS Mode

Table 14.329. Register 0x5402 Phase Read Control

Reg Address	Bit Field	Type	Setting Name	Description
0x5402	4	S	PHRD_EXE-CUTE_READ	Set to 1 to request a phase readout for the PLL as specified in PHRD_PLL_SEL
0x5402	1:0	R/W	PHRD_PLL_SEL	Selects the PLL to read when a phase read is requested. 00: PLLA 01: PLLB 10: PLLC 11: PLLD

Note:

1. After enabling PPS mode, users should wait for a PPS edge (PHRD_HALFCYC_FLG) before performing a DSPLLD phase readout. The data associated with this first read should be discarded to ensure both phase data and status have been initialized to a valid state.

Table 14.330. Register 0x5403 Selected Clocks for Phase Read Out

Reg Address	Bit Field	Type	Setting Name	Description
0x5403	7	R/W	PHRD_SELEC-TED_REFCLK	1: Loop is open due to register setting
0x5403	6	R/W	PHRD_SELEC-TED_REFCLK	1: Loop is open due to holdover/free run.
0x5403	5:4	R/W	PHRD_SELEC-TED_REFCLK	00: IN3 and IN4 not selected 01: IN3 10: IN4 11: IN3 and IN4 selected

Reg Address	Bit Field	Type	Setting Name	Description
0x5403	3:0	R/W	PHRD_SELEC-TED_REFCLK	Determines the selected reference clock since the last read. 0000: IN0, IN1, IN2 and RefIn not selected. 0001: IN0 0010: IN1 0100: IN2 1000: RefIn 1001:RefIn and IN0 1010:RefIn and IN1 1011:RefIn, IN0 and IN1 1100:RefIn and IN2 1101:RefIn, IN0 and IN2 1111:RefIn, IN0, IN1, IN2

Note:

1. Only valid after phase read control is executed. Indicates the selected reference clock since the last read.
2. Reads of DSPLLD when PPS mode is enabled may return all zeros in this register. This is an indication that not enough time passed between reads to collect data.

Table 14.331. Register 0x5404-0x5407 Phase Read

Reg Address	Bit Field	Type	Setting Name	Description
0x5404	31:24	R/W	PHRD_PHASE_READ_R	Only valid after phase read control is executed. Returns current phase in units of 25/Fvco.
0x5405	23:16	R/W	PHRD_PHASE_READ_R	
0x5406	15:8	R/W	PHRD_PHASE_READ_R	
0x5407	7:0	R/W	PHRD_PHASE_READ_R	

Note:

1. Bit 31 is set when the value was previously read (indicates "stale" information being returned).

Table 14.332. Register 0x5408-0x540B Reference Time Read

Reg Address	Bit Field	Type	Setting Name	Description
0x5408	31:24	R/W	PHRD_REF_TIME_READ_R	Only valid after phase read is executed. Returns current reference clock period in units of 25/Fvco.
0x5409	23:16	R/W	PHRD_REF_TIME_READ_R	
0x540A	15:8	R/W	PHRD_REF_TIME_READ_R	
0x540B	7:0	R/W	PHRD_REF_TIME_READ_R	

Note:
1. Bit 31 is set when the value was previously read (indicates "stale" information being returned).

Table 14.333. Register 0x540C-0x540F Feedback Time Read

Reg Address	Bit Field	Type	Setting Name	Description
0x540C	31:24	R/W	PHRD_FB_TIME_READ_R	Only valid after phase read control is executed. Returns current feedback clock period in units of 25/Fvco.
0x540D	23:16	R/W	PHRD_FB_TIME_READ_R	
0x540E	15:8	R/W	PHRD_FB_TIME_READ_R	
0x540F	7:0	R/W	PHRD_FB_TIME_READ_R	

Note:
1. Bit 31 is set when the value was previously read (indicates "stale" information being returned).

Table 14.334. 0x5410 Phase Read Status

Reg Address	Bit Field	Type	Setting Name	Description
0x5410	7:5	R/W	PHRD_NET_REFCLKS	2's complement of excess(+)/missing(-) reference clocks since read was last executed on this PLL.
0x5410	4	S	PHRD_NET_REFCLKS_Z	1: Every feedback clock cycle the phase readout saw exactly 1 reference clock cycle (e.g. net refclks was always 0)
0x5410	3	R/W	PHRD_REFCLKIN_DEAD	1: Selected reference-clock for this PLL went 2 sequential feedback clock cycles with no reference clock edges.

Reg Address	Bit Field	Type	Setting Name	Description
0x5410	2	R/W	PHRD_LOL_STS	0: No loss of lock 1: Loss of lock detected
0x5410	1	R/W	PHRD_LOS_STS	0: No loss of signal 1: Loss of signal detected
0x5410	0	R/W	PHRD_OOF_STS	0: OOF not set 1: OOF detected

Note:
1. Only valid after a phase read control is executed.

Table 14.335. 0x5421 Half Cycle Event

Reg Address	Bit Field	Type	Setting Name	Description
0x5421	3	R/W	PHRD_HALFCYC_FLG	Write 0 to clear 1 is set when a new half-cycle of feedback clock is done and new phase measurement is avaliable.

15. Custom Differential Amplitude Controls

In some applications, it may be desirable to drive larger or smaller differential amplitudes than those produced by the standard LVPECL and LVDS settings generated by ClockBuilder Pro. For example, "CML" format is sometimes desired for an application, but CML is not a defined standard, and hence, the input amplitude of CML signals may differ between receivers. In these cases, the following information describes how to implement non-standard differential amplitudes.

The differential output driver has two basic modes of operation as well as variable output amplitude capability. The Normal mode has an internal impedance of ~100 ohms differential, while the Low Power mode has an internal impedance of >500 ohms differential. In both cases, when properly terminated with 100 ohms differential externally, the amplitudes listed in the table below result.

Table 15.1. Differential Output Amplitude Typical Values

OUTx_AMPL	Normal Mode OUTx_FORMAT = 1 (Vpp-SE mV - Typical)	Low Power Mode OUTx_FORMAT = 2 (Vpp SE mV - Typical)
0	130	200
1	230	400
2	350	620
3	450	820
4	575	1010
5	700	1200
6	810	1350[1]
7	920	1600[1]

Note:

1. In low power mode with VDDOx = 1.8 V, OUTx_AMPL may not be set to 6 or 7.
2. These amplitudes are based upon 100 Ω differential termination

For applications using a custom differential output amplitude the common mode voltage should be selected as shown in the table below. These settings, along iwth the settings given in Table 21, have been verified to give good signal integrity. Some extreme combinations of amplitude and common mode may have impaired signal integrity.

Also, in cases where the receiver is dc-biased either internally or through an external network, the outputs of this device must be ac-coupled. Output driver performance is not guaranteed when dc-coupled to a biased-input receiver.

Table 15.2. Differential Output Common Mode Voltage Settings

VDDOx (V)	Differential Format	OUTx_FORMAT (dec)	Common Mode Voltage (V)	OUTx_CM (dec)
3.3	Normal	1	2.05	11
3.3	Low Power	2	1.65	7
2.5	Normal	1	1.35	12
2.5	Low Power	2	1.15	10
1.8	Normal	1	0.80	13
1.8	Low Power	2	0.80	13

See also (xref) for additional information on the OUTx_FORMAT, OUTx_AMPL, and OUTx_CM controls.

16. Accessing Design and Support Collateral

The Si5383/84 is currently available to restricted customers only. To access the support documentation, contact Skyworks Support.

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