



# 2105181043 Si828x Version 2 Silicon Revision

**PRCN Issue Date:** May 18, 2021

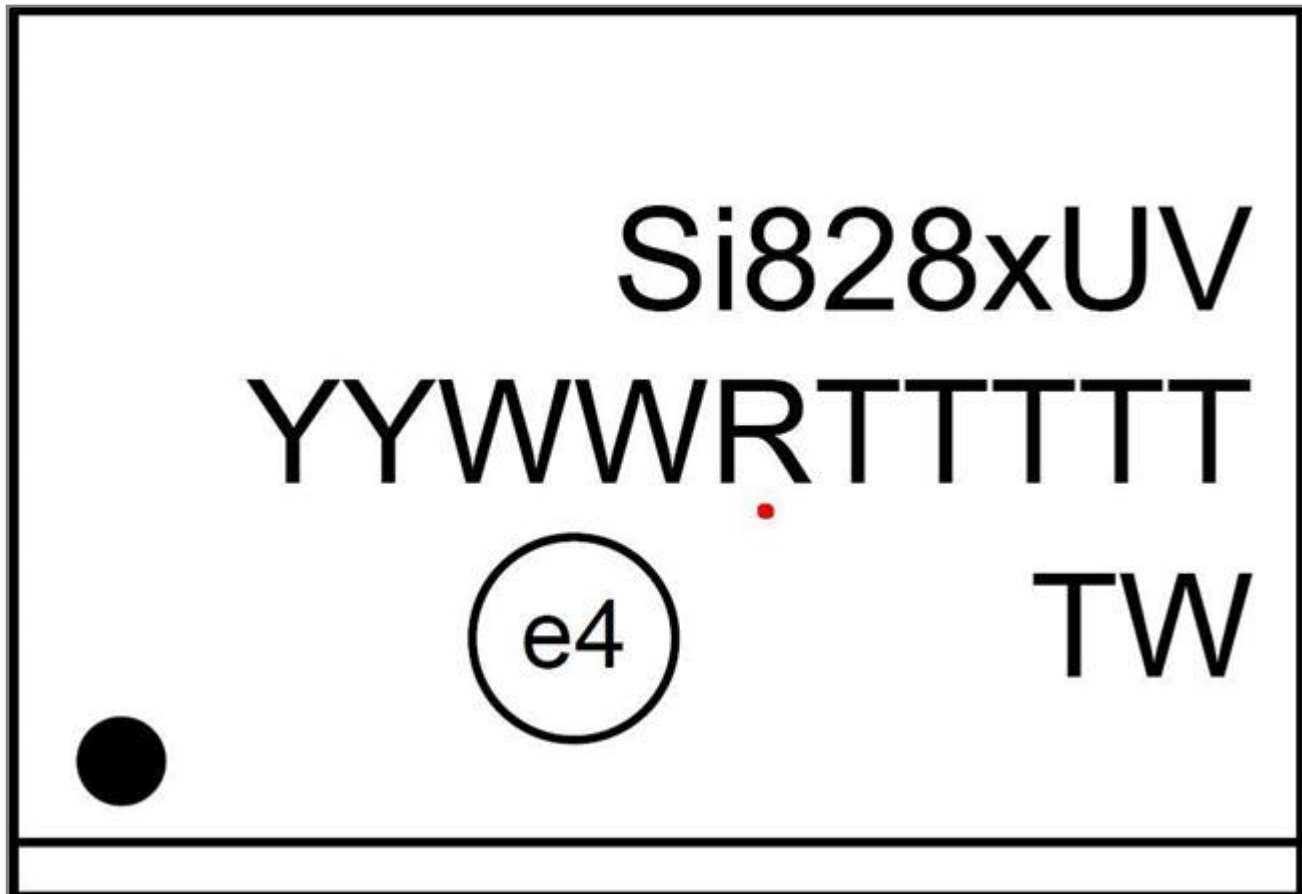
**Effective Date:** Aug 24, 2021

**PCN Type:** Product Revision

## Description of Change

Silicon Labs is pleased to announce hardware version 2 of the Si828x SiC FET-Ready ISODrivers and revision 2.0 of the corresponding datasheet for these products.

Please note the identification of the revised devices. In the device topside marking, the first character ("R") in the "RTTTTT" field is "D" for Industrial Grade and "Q" for Automotive Grade of the new revision.



Note: After the effective date of the PRCN, Silicon Labs reserves the right not to accept orders for the old revision.

## Reason for Change

The Si828x version 2 provides improvements that make it more relevant for SiC FET gate drive applications, including improved common mode transient immunity (CMTI) and additional undervoltage lockout (UVLO) voltages, in addition to being fully backwards compatible for IGBTs.

Several datasheet parameters have been updated and are documented in the new v2.0 datasheet. Please review the datasheet thoroughly when assessing the impact of this Product Revision on your design.

Refer to the Revision History section of the v2.0 datasheet for additional summaries of document changes. Among the parameters adjusted are the following:

Parameter Name	Symbol	Previous		New		Change Type	Reason
		Minimum	Maximum	Minimum	Maximum		
Common Mode Transient Immunity	CMTI	35kV/μs		125kV/μs		Improvement	Better noise immunity for fast-switching SiC FETs
High Drive Peak Output Current	IOH	2.5A		2.0A		Recharacterization	Improved peak current test methodology demonstrated lower IOH
Low Drive Peak Output Current	IOL	3.0A		4.1A		Recharacterization	Improved peak current test methodology demonstrated higher IOL
VDESAT Threshold	VDESAT	6.5V	7.3V	6.25V	7.4V	Recharacterization	More correctly specify VDESAT
VDESAT Sense to 90% VIH Delay	tDESAT(90%)	---	300ns	---	350ns	Recharacterization	Test conditions clarified and spec revised
VDESAT Sense to 10% VIH Delay	tDESAT(10%)	0.77μs	2.7μs	---	2.3μs	Recharacterization	Test conditions clarified and spec revised
Reset to FLT High Delay	tRST to FLT	---	45ns	---	350ns	Improvement	Debounce filter added to RST pin to improve noise immunity; impacts FLT indication time
Safety Temperature	TS	---	150°C	---	140°C	Respecification	Process parameters clarified
IC Junction-to-Air Thermal Resistance	θJA	---	60 °C/W	---	74 °C/W	Recharacterization	Packaging model updated

## Impact on Form, Fit, Function, Quality, Reliability

The version 2 is a pin compatible, drop-in replacement for the version 1 devices with improved CMTI with no adverse impact on form, fit, function, or reliability of the devices.

The Si828x Industrial Grade does not fully comply to AEC-Q100 qualification requirements. However, Automotive grade components are available which support AEC-Q100 qualification requirements--please contact Silicon Labs for details.

## Product Identification

Existing Part #	Replacement Part #	DropInCompInd.
Si8281BC-IS	Si8281BC-IS	YES
Si8281BD-IS	Si8281BD-IS	YES
Si8281CC-IS	Si8281CC-IS	YES
Si8281CD-IS	Si8281CD-IS	YES
Si8282BC-IS	Si8282BC-IS	YES
Si8282BD-IS	Si8282BD-IS	YES
Si8282CC-IS	Si8282CC-IS	YES
Si8282CD-IS	Si8282CD-IS	YES
Si8283BC-IS	Si8283BC-IS	YES
Si8283BD-IS	Si8283BD-IS	YES
Si8283CC-IS	Si8283CC-IS	YES
Si8283CD-IS	Si8283CD-IS	YES
Si8284BC-IS	Si8284BC-IS	YES
Si8284BD-IS	Si8284BD-IS	YES
Si8284CC-IS	Si8284CC-IS	YES
Si8284CD-IS	Si8284CD-IS	YES
Si8285BC-IS	Si8285BC-IS	YES
Si8285BD-IS	Si8285BD-IS	YES
Si8285CC-IS	Si8285CC-IS	YES
Si8285CD-IS	Si8285CD-IS	YES
Si8286BC-IS	Si8286BC-IS	YES
Si8286BD-IS	Si8286BD-IS	YES
Si8286CC-IS	Si8286CC-IS	YES
Si8286CD-IS	Si8286CD-IS	YES

## Kit Identification

Kits impacted by the above product are listed below. Orders for the following obsolete kits will no longer be accepted.

Existing Kit #	Replacement Kit #
SI8284-KIT	SI8284V2-KIT

**Last Date of Unchanged Product:** Aug 24, 2021

### **Qualification Samples**

All OPNs available

### **Customer Response**

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at <http://www.silabs.com>.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to [PCNEarlyAcceptance@silabs.com](mailto:PCNEarlyAcceptance@silabs.com)

### **User Registration**

Register today to create your account on Silabs.com. Your personalized profile allows you to receive technical document updates, new product announcements, "how-to" and design documents, product change notices (PCN) and other valuable content available only to registered users. <http://www.silabs.com/profile>

### **Qualification Data**

See attached Qualification Report.



### Si828x AEC-Q100 Qualification Report

The information contained in this document is CONFIDENTIAL and PROPRIETARY to Silicon Labs and is intended only for the internal use of Silicon Labs. Any other use or reproduction of any part of this document is prohibited without Silicon Labs' written consent. Any use of this document outside of Silicon Labs is solely at the risk of the user. Silicon Labs disclaims all warranties concerning the accuracy of the information contained in this document. This document is version controlled; printed or electronically saved versions of this documents may be obsolete. Any misuse of this document should be reported to DL.QualitySystems@silabs.com

Part Rev D, Vanguard Fabrication, ASECL Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
<b>Test Group A – Accelerated Environment Stress Tests - 24-Pin WB SOIC</b>							
HAST	JA110 130°C, 85%RH Vcc=5.5V, 96 hours	3 lots, N=>77	Q040569	0/80	1		Pass
			Q040871	0/80	1	3 lots	
			Q040872	0/80	1	0/240	
UHAST	JA110 130°C, 85%RH 96 hours	3 lots, N=>77	Q040629	0/80	1		Pass
			Q040873	0/80	1	3 lots	
			Q040874	0/80	1	0/240	
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q040875	0/80	1		Pass
			Q040630	0/80	1	3 lots	
			Q040876	0/80	1	0/240	
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q038795	0/46	1		Pass
			Q040877	0/46	1	3 lots	
			Q040878	0/46	1	0/138	
<b>Test Group A – Accelerated Environment Stress Tests - 20-Pin WB SOIC</b>							
HAST	JA110 130°C, 85%RH Vcc=5.5V, 96 hours	3 lots, N=>77	Q037147	0/78	1, 2		Pass
			Q040787	0/80	1, 2	3 lots	
			Q040785	0/80	1, 2	0/238	
UHAST	JA110 130°C, 85%RH 96 hours	3 lots, N=>77	Q037148	0/78	1, 2		Pass
			Q040786	0/80	1, 2	3 lots	
			Q040784	0/80	1, 2	0/238	
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q046039	0/80	1		Pass
			Q040730	0/80	1, 2	3 lots	
			Q040731	0/80	1, 2	0/240	
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q036594	0/80	1, 2		Pass
			Q040877	0/46	1, 2	3 lots	
			Q040878	0/46	1, 2	0/172	



### Si828x AEC-Q100 Qualification Report

The information contained in this document is CONFIDENTIAL and PROPRIETARY to Silicon Labs and is intended only for the internal use of Silicon Labs. Any other use or reproduction of any part of this document is prohibited without Silicon Labs' written consent. Any use of this document outside of Silicon Labs is solely at the risk of the user. Silicon Labs disclaims all warranties concerning the accuracy of the information contained in this document. This document is version controlled; printed or electronically saved versions of this documents may be obsolete. Any misuse of this document should be reported to DL.QualitySystems@silabs.com

Part Rev D, Vanguard Fabrication, ASECL Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
<b>Test Group A – Accelerated Environment Stress Tests - 16-Pin WB SOIC</b>							
HAST	JA110 130°C, 85%RH Vcc=5.5V, 96 hours	3 lots, N=>77	Q037147	0/78	1, 2	3 lots 0/238	Pass
			Q040787	0/80	1, 2		
			Q040785	0/80	1, 2		
UHAST	JA110 130°C, 85%RH 96 hours	3 lots, N=>77	Q037148	0/78	1, 2	3 lots 0/238	Pass
			Q040786	0/80	1, 2		
			Q040784	0/80	1, 2		
Temp Cycle	JA104 Cond C: -65°C to 150°C 500 cycles	3 lots, N=>77	Q040730	0/80	1, 2	3 lots 0/240	Pass
			Q040730	0/80	1, 2		
			Q040731	0/80	1, 2		
HTSL	JA103 150°C, 1000hr	1 lot, N=>45	Q036594	0/80	1, 2	3 lots 0/172	Pass
			Q040877	0/46	1, 2		
			Q040878	0/46	1, 2		
<b>Test Group B – Accelerated Lifetime Simulation Tests</b>							
HTOL	JA108 T <sub>j</sub> ≥ 125°C, Dynamic Vcc=5.5V, 1000 hours	3 lots, N=>77	Q038379	0/80	3	3 lots 0/250	Pass
			Q041697	0/90			
			Q042614	0/80			
LTOL	JA108 -10°C, Dynamic Vcc=5.5V, 1000 hours	1 lot, N=>77	Q027145	0/80	3	1 lots 0/80	Pass
ELFR	AEC-Q100-008 T <sub>j</sub> ≥ 125°C, Dynamic Vcc=5.5V, 48 hours	3 lots, N=>800	Q047260	0/810	4	4 lots 0/3237	Pass
			Q042775	0/808			
			Q042836	0/810			
			Q029753	0/809			



### Si828x AEC-Q100 Qualification Report

The information contained in this document is CONFIDENTIAL and PROPRIETARY to Silicon Labs and is intended only for the internal use of Silicon Labs. Any other use or reproduction of any part of this document is prohibited without Silicon Labs' written consent. Any use of this document outside of Silicon Labs is solely at the risk of the user. Silicon Labs disclaims all warranties concerning the accuracy of the information contained in this document. This document is version controlled; printed or electronically saved versions of this documents may be obsolete. Any misuse of this document should be reported to DL.QualitySystems@silabs.com

Part Rev D, Vanguard Fabrication, ASECL Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
<b>Test Group C – Package Assembly Integrity Tests - 16-Pin NB SOIC</b>							
Wire Bond Shear	AEC-Q100-001	5 units, N=>30	723163	0/5		3 lots	Pass
			721178	0/5			
			388268	0/5			
Wire Bond Pull	M-STD-883 Performed post-TC	5 units, N=>30	798488	0/5		3 lots	Pass
			798489	0/5			
			798490	0/5			
Physical Dimensions	JB100 24-Pin WB (300mil)	3 lots, N=>10	798488	0/30		3 lots	Pass
			798489	0/30			
			798490	0/30			
Physical Dimensions	JB100 20-Pin WB (300mil)	3 lots, N=>10	725151	0/30		3 lots	Pass
			725150	0/30			
			709393	0/30			
Physical Dimensions	JB100 16-Pin WB (300mil)	3 lots, N=>10	723163	0/30		3 lots	Pass
			721178	0/30			
			388268	0/30			
Solderability	JB102	1 lot, N=>15	798488	0/10		3 lots	Pass
			798489	0/10			
			798490	0/10			
<b>Test Group E – Electrical Verification</b>							
ESD-HBM	AEC-Q100-002	1 lot, N=>3	Q047220			0.5 kV	Class H1B
ESD-CDM	AEC-Q100-011 16-Pin NB SOIC	1 lot, N=>3	Q047221			750 V	Class C5
Latch Up	AEC-Q100-004 ±100mA Overvoltage = 36V	1 lot, N=>6	Q047170	85 °C			Pass
Electromagnetic Compatibility	SAE J1752	1 lot, N=>1	Q045675				Pass

Notes:

1. Parts are Pre-conditioned at MSL3/260°C
2. Leveraged package family qualification data
3. Leveraged die family qualification data

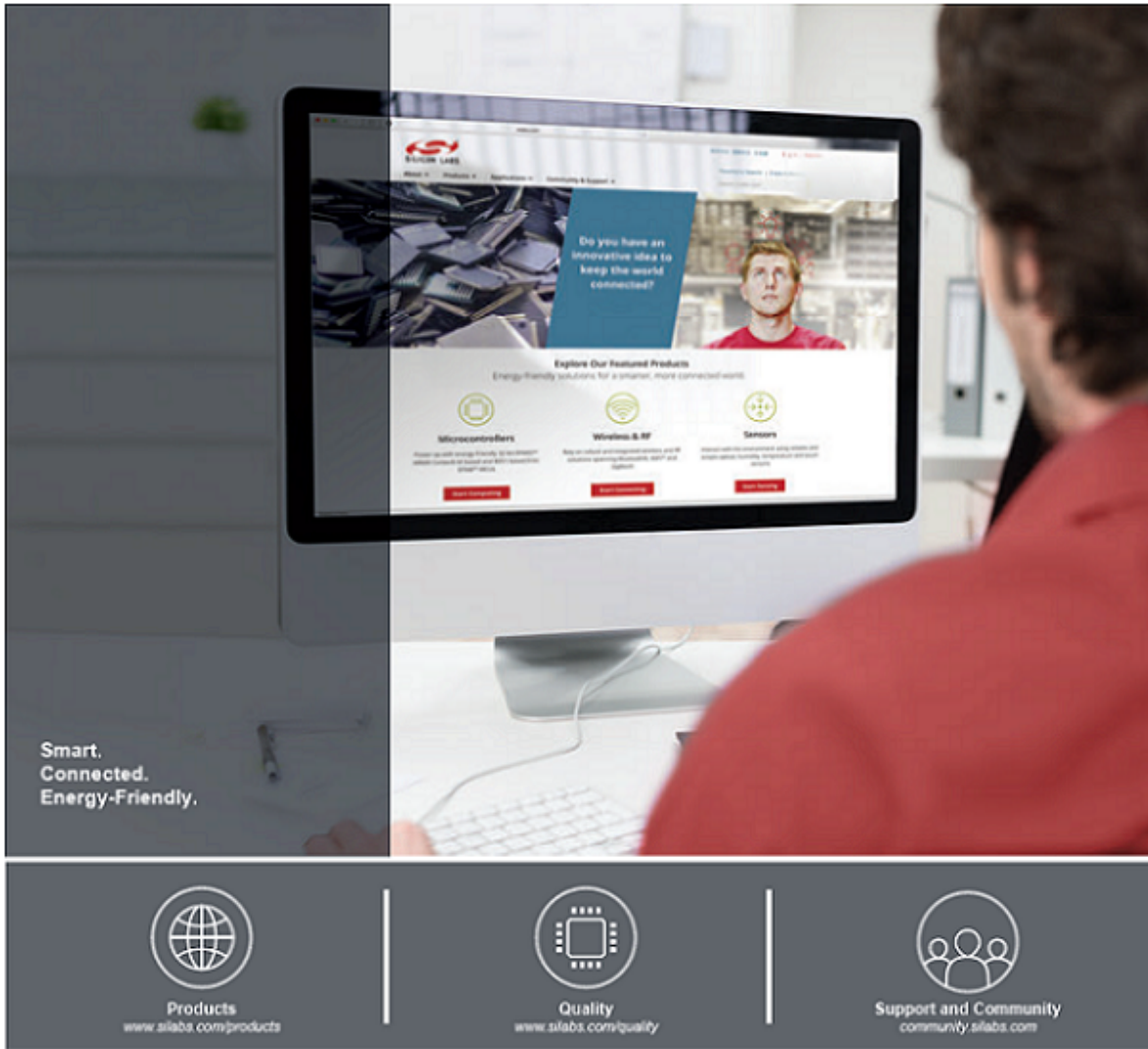
This report applies to the following part numbers:				
Si8281BC-IS/R	Si8281BD-IS/R	Si8281CC-IS/R	Si8281CD-IS/R	Si8281DC-IS/R



### Si828x AEC-Q100 Qualification Report

The information contained in this document is CONFIDENTIAL and PROPRIETARY to Silicon Labs and is intended only for the internal use of Silicon Labs. Any other use or reproduction of any part of this document is prohibited without Silicon Labs' written consent. Any use of this document outside of Silicon Labs is solely at the risk of the user. Silicon Labs disclaims all warranties concerning the accuracy of the information contained in this document. This document is version controlled; printed or electronically saved versions of this documents may be obsolete. Any misuse of this document should be reported to DL.QualitySystems@silabs.com

Part Rev D, Vanguard Fabrication, ASECL Assembly except as noted							
Test Name	Test Condition	Qualification	Lot ID or Start	Fail/Pass or End	Notes	Summary	Status
Si8281DD-IS/R	Si8281EC-IS/R	Si8281ED-IS/R		Si8282BC-IS/R		Si8282BD-IS/R	
Si8282CC-IS/R	Si8282CD-IS/R	Si8282DC-IS/R		Si8282DD-IS/R		Si8282EC-IS/R	
Si8282ED-IS/R	Si8283BC-IS/R	Si8283BD-IS/R		Si8283CC-IS/R		Si8283CD-IS/R	
Si8283DC-IS/R	Si8283DD-IS/R	Si8283EC-IS/R		Si8283ED-IS/R		Si8284BC-IS/R	
Si8284BD-IS/R	Si8284CC-IS/R	Si8284CD-IS/R		Si8284DC-IS/R		Si8284DD-IS/R	
Si8284EC-IS/R	Si8284ED-IS/R	Si8285BC-IS/R		Si8285BD-IS/R		Si8285CC-IS/R	
Si8285CD-IS/R	Si8285DC-IS/R	Si8285DD-IS/R		Si8285EC-IS/R		Si8285ED-IS/R	
Si8286BC-IS/R	Si8286BD-IS/R	Si8286CC-IS/R		Si8286CD-IS/R		Si8286DC-IS/R	
Si8286DD-IS/R	Si8286EC-IS/R	Si8286ED-IS/R					
Si8281BC-AS/R	Si8281BD-AS/R	Si8281CC-AS/R		Si8281CD-AS/R		Si8281DC-AS/R	
Si8281DD-AS/R	Si8281EC-AS/R	Si8281ED-AS/R		Si8282BC-AS/R		Si8282BD-AS/R	
Si8282CC-AS/R	Si8282CD-AS/R	Si8282DC-AS/R		Si8282DD-AS/R		Si8282EC-AS/R	
Si8282ED-AS/R	Si8283BC-AS/R	Si8283BD-AS/R		Si8283CC-AS/R		Si8283CD-AS/R	
Si8283DC-AS/R	Si8283DD-AS/R	Si8283EC-AS/R		Si8283ED-AS/R		Si8284BC-AS/R	
Si8284BD-AS/R	Si8284CC-AS/R	Si8284CD-AS/R		Si8284DC-AS/R		Si8284DD-AS/R	
Si8284EC-AS/R	Si8284ED-AS/R	Si8285BC-AS/R		Si8285BD-AS/R		Si8285CC-AS/R	
Si8285CD-AS/R	Si8285DC-AS/R	Si8285DD-AS/R		Si8285EC-AS/R		Si8285ED-AS/R	
Si8286BC-AS/R	Si8286BD-AS/R	Si8286CC-AS/R		Si8286CD-AS/R		Si8286DC-AS/R	
Si8286DD-AS/R	Si8286EC-AS/R	Si8286ED-AS/R					



#### Disclaimer

Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Labs shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any Life Support System without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

#### Trademark Information

Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, Clockbuilder®, CMEMS®, DSPLL®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Ember®, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, ISModem®, Micrium, Precision32®, ProSLIC®, Simplicity Studio®, SiPHY®, Telegesis, the Telegesis Logo®, USBXpress®, Zentri and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.



**Silicon Laboratories Inc.**  
**400 West Cesar Chavez**  
**Austin, TX 78701**

<http://www.silabs.com>