LMH6518 900 MHz, Digitally Controlled, Variable Gain Amplifier

1 Features

- Gain Range: 40 dB
- Gain Step Size: 2 dB
- Combined Gain Resolution With Gsps ADCs: 8.5 mdB
- Minimum Gain: −1.16 dB
- Maximum Gain: 38.8 dB
- −3 dB BW: 900 MHz
- Rise and Fall Time: <500 ps
- Recovery Time: <5 ns
- Propagation Delay Variation: 100 ps
- HD2 at 100 MHz: −50 dBc
- HD3 at 100 MHz: −53 dBc
- Input-Referred Noise (Maximum Gain): 0.98 nV/√Hz
- Overvoltage Clamps for Fast Recovery
- Power Consumption: Auxiliary Turned Off 1.1 W to 0.75 W

2 Applications

- Oscilloscope Programmable Gain Amplifiers
- Differential ADC Drivers
- High-Frequency Single-Ended Input to Differential Conversion
- Precision Gain Control Applications
- Medical Applications
- RF/IF Applications

3 Description

The LMH6518 device is a digitally controlled variable gain amplifier whose total gain is varied from −1.16 dB to 38.8 dB for a 40 dB range in 2-dB steps. The −3-dB bandwidth is 900 MHz at all gains. Gain accuracy at each setting is typically 0.1 dB. When used in conjunction with TI's Gsample/second (Gsps) ADC with adjustable full-scale (FS) range, the LMH6518 gain adjustment accommodates full scale input signals from 6.8 mV_{PP} to 920 mV_{PP} to get 700 mV_{PP} nominal at the ADC input. The auxiliary output (+OUT AUX and −OUT AUX) follows the main output and is intended for use in oscilloscope trigger function circuitry but may have other uses in other applications.

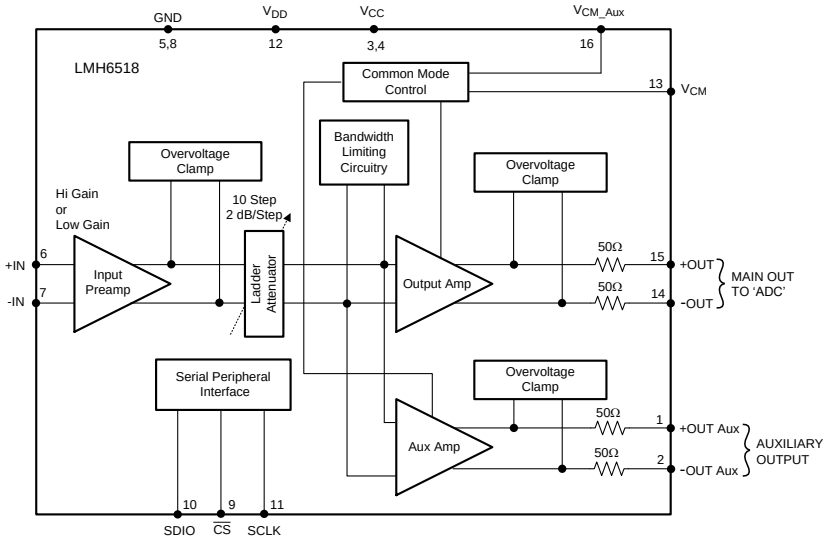
The LMH6518 gain is programmed through a SPI-1 compatible serial bus. A signal path combined gain resolution of 8.5 mdB is achieved when the device's gain and the Gsps ADC's FS input are both manipulated. Inputs and outputs are DC-coupled. The outputs are differential with individual common mode (CM) voltage control (for main and auxiliary outputs), and have a selectable bandwidth limiting circuitry (common to both main and auxiliary) of 20, 100, 200, 350, 650, 750 MHz or full bandwidth.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMH6518	WQFN (16)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2013) to Revision D **Page**

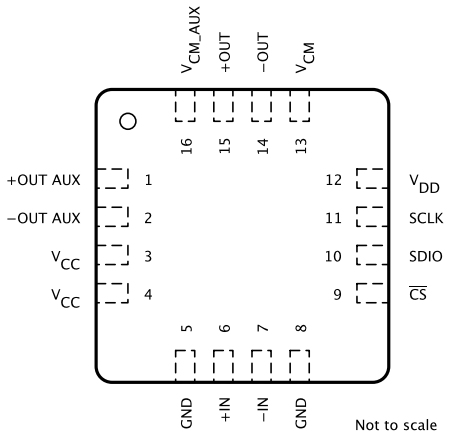
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added *Thermal Information* table ... 5
- Changed Y-axis unit on Output vs Input *Typical Characteristics* graphs From: (V) To: (mV) ... 17
- Changed Y-axis unit on V_{OUT} vs V_{IN} *Application Curves* graph From: (V) To: (mV) ... 34

Changes from Revision A (March 2013) to Revision B **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 1

5 Pin Configuration and Functions

RGH Package
16-Pin WQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	+OUT AUX	O	Auxiliary positive output
2	−OUT AUX	O	Auxiliary negative output

(1) G = Ground, I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
3, 4	V_{CC}	P	Analog power supply
5, 8	GND	G	Ground, electrically connected to the WQFN heat sink
6	+IN	I	Positive input
7	–IN	I	Negative input
9	$\overline{CS}$	I	Serial chip select (SPI interface, active low): While this signal is asserted SCLK is used to accept serial data present on SDIO and to source serial data on SDIO. When this signal is de-asserted, SDIO is ignored and SDIO is in TRI-STATE mode.
10	SDIO	I/O	Serial data-in or data-out (SPI interface): Serial data are shifted into the device (8 bit command and 16 bit data) on this pin while $\overline{CS}$ signal is asserted during Write operation. Serial data are shifted out of the device on this pin during a read operation while $\overline{CS}$ signal is asserted. At other times, and after one complete Access Cycle (24 bits, see Figure 54 and Figure 55), this input is ignored. This output is in TRI-STATE mode when $\overline{CS}$ is de-asserted. This pin is bi-directional.
11	SCLK	I	Serial clock (SPI interface): Serial data are shifted into and out of the device synchronous with this clock signal. SCLK transitions with $\overline{CS}$ de-asserted are ignored. SCLK must be stopped when not required to minimize digital crosstalk.
12	V_{DD}	P	Digital power supply
13	V_{CM}	I	Input from ADC to control main output CM
14	−OUT	O	Main negative output
15	+OUT	O	Main positive output
16	V_{CM_AUX}	I	Input to control auxiliary output CM

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{CC} (5 V nominal)		5.5	V
	V_{DD} (3.3 V nominal)		3.6	
Differential input			±1	V
Input common mode voltage		1	4	V
V_{CM} and V_{CM_Aux}			2	V
SPI inputs			3.6	V
Soldering temperature	Infrared or convention (20 s)		235	°C
	Wave (10 s)		260	
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Analog supply voltage		5 ±5%		V
V_{DD}	Digital supply voltage		3.3 ±5%		V
T_A	Temperature range	–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		LMH6518 RGH (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, all limits are ensured for T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on) (see Table 8 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
DYNAMIC PERFORMANCE						
LSBW	–3-dB bandwidth	All gains		900		MHz
	Peaking	All gains		1		dB
GF_0.1 dB	±0.1-dB gain flatness	All gains		150		MHz
GF_1 dB	±1-dB gain flatness	All gains		400		MHz
TRS	Rise time			460		ps
TRL	Fall time			450		
OS	Overshoot	Main output		9%		
t_{s_1}	Settling time	Main output, ±0.5%		10		ns
t_{s_2}	Settling time	Main output, ±0.05%		14		
t_recover	Recovery time(4)	All gains		<5		ns
P_D	Propagation delay	V_{OUT} = 0.7 V_{PP}, all gains		1.2		ns
P_{D_VAR}	Propagation delay variation	Gain varied		100		ps
NOISE, DISTORTION, AND RF SPECIFICATIONS						
e_{n_1}	Input noise spectral density	Max gain, 10 MHz		0.98		nV/√Hz
e_{n_2}	Input noise spectral density	Preamp LG and 0-dB ladder, 10 MHz		4.1		nV/√Hz
e_{no_1}	RMS output noise	Max gain, 100 Hz to 400 MHz		1.7		mV
e_{no_2}	RMS output noise	Preamp LG, 0-dB ladder, 100 Hz to 400 MHz		940		µV
NF_1	Noise figure	Max gain, R_S = 50 Ω each input, 10 MHz		3.8		dB
NF_2	Noise figure	Preamp LG, 0-dB ladder, R_S = 50 Ω each input, 10 MHz		13.5		dB
HD2_1	2nd harmonic distortion(5)	Main output, 100 MHz, all gains		–50		dBc
HD3_1	3rd harmonic distortion(5)	Main output, 100 MHz, all gains		–53		dBc
HD2_2	2nd harmonic distortion(5)	Auxiliary output, 100 MHz, all gains		–48		dBc
HD3_2	3rd harmonic distortion(5)	Auxiliary output, 100 MHz, all gains		–50		dBc
HD2_3	2nd harmonic distortion(5)	Main output, 250 MHz, all gains		–44		dBc
HD3_3	3rd harmonic distortion(5)	Main output, 250 MHz, all gains		–50		dBc
HD2/HD3_4	2nd/ 3rd harmonic distortion(5)	Auxiliary output, 250 MHz, all gains		–42		dBc
IMD3	Intermodulation distortion(5)	f = 250 MHz, main output		–65		dBc
OIP3_1	Intermodulation intercept(5)	Main output, 250 MHz		26		dBm
P_1dB_main	–1-dB compression	Main output, 250 MHz, 0-dB ladder		1.8		V_{PP}
		Main output, 250 MHz, 20-dB ladder		1		

(1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$.
(2) Limits are 100% production tested at 25°C unless otherwise specified. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and also depends on the application and configuration. The typical values are not tested and are not ensured on shipped production material.
(4) Recovery time is the slower of the main and auxiliary outputs. Output swing of 700 mV_{PP} shifted up or down by 50% (0.35 V) by introducing an offset. Measured values correspond to the time it takes to return to within ±1% of 0.7 V_{PP} (±7 mV).
(5) Distortion data taken under single ended input condition.

Electrical Characteristics (continued)

Unless otherwise noted, all limits are ensured for T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on) (see Table 8 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP(3)	MAX(2)	UNIT
P_1dB_aux	–1-dB compression	Auxiliary output, 250 MHz, 0-dB ladder		1.65		V_{PP}
		Auxiliary output, 250 MHz, 20-dB ladder		1		
GAIN PARAMETERS						
$A_{V\_DIFF\_MAX}$	Maximum gain		38.1	38.8	39.5	dB
$A_{V\_DIFF\_MIN}$	Minimum gain		–1.91	–1.16	–0.4	dB
Gain_Step	Gain step size	All gains including preamp step	1.8	2	2.2	dB
	Gain step size with ADC (see *Application and Implementation*)	ADC FS adjusted		8.5		mdB
Gain_Range	Gain range		39	40	41	dB
$TC\_A_{V\_DIFF}$	Gain temp coefficient(6)	All gains		–0.8		mdB/°C
$Gain\_A_{CC}$	Absolute gain accuracy	Compared to theoretical from max gain in 2-dB steps	0.75		0.75	dB
MATCHING						
Gain_match	Gain matching, main and auxiliary	All gains		±0.1	±0.2	dB
BW_match	–3-dB bandwidth matching, main and auxiliary	All gains		5%		
RT_match	Rise time matching, main and auxiliary	All gains		5%		
PD_match	Propagation delay matching, main and auxiliary	All gains		100		ps
ANALOG I/O						
CMRR_1	CM rejection ratio (see Table 8)	Preamp HG, 0-dB ladder, 1.9 V < CMVR < 3.1 V	45	86		dB
CMRR_2	CM rejection ratio (see Table 8)	Preamp LG, 0-dB ladder, 1.9 V < CMVR < 3.1 V	40	55		dB
CMVR_1	Input common mode voltage range	Preamp HG, all ladder steps, CMRR ≥ 45 dB	1.9		3.1	V
CMVR_2	Input common mode voltage range	Preamp LG, all ladder steps, CMRR ≥ 40 dB	1.9		3.1	V
$\lvert\Delta V_{O\_CM}\rvert\Delta_{I\_CM}\rvert$		All gains, 2 V < CMVR < 3 V	–60	–100		dB
CMRR_CM	CM rejection ratio relative to VCM (see Table 8)	Preamp LG, 0 dB		101		dB
Z_{in_diff}	Differential input impedance	All gains		150 || 1.5		KΩ || pF
Z_{in_CM}	CM input impedance	Preamp HG		420 || 1.7		KΩ || pF
		Preamp LG		900 || 1.7		
FS_{OUT1}	Full scale voltage swing	Main output, all gains, THD at 100 MHz ≤ –40 dBc	770(7)	800		mV_{PP}
FS_{OUT2}	Full scale voltage swing	Main output, clamped, 0-dB ladder		1800	1960	mV_{PP}
FS_{OUT3}	Full scale voltage swing	Auxiliary output, all gains THD at 100 MHz ≤ –40 dBc	770(7)	800		mV_{PP}
FS_{OUT4}	Full scale voltage swing	Auxiliary output, clamped, 0-dB ladder		1600	1760	mV_{PP}
V_{OUT_MAX1}	Voltage at each output pin (clamped)	Main output, all gains, V_{CM} = 1.2 V	0.5		1.8	V

(6) Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.
(7) Specified by design.

Electrical Characteristics (continued)

Unless otherwise noted, all limits are ensured for T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on) (see Table 8 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
V_{OUT_MAX2}	Voltage at each output pin (clamped)	Auxiliary output, all gains, V_{CM} = 1.2 V		0.8		2.2	V
V_{OUT_MAX3}	Voltage at each output pin (clamped)	Main output, all gains, V_{CM} = 1.45 V				2.05	V
V_{OUT_MAX4}	Voltage at each output pin (clamped)	Auxiliary output, all gains, V_{CM} = 1.45 V				2.45	V
Z_{OUT_DIFF}	Differential output impedance	All gains		92	100	108	Ω
V_{OOS}	Output offset voltage	All gains			±15	±40	mV
V_{OOS_shift1}	Output offset voltage shift	Preamp LG to preamp HG			13.7		mV
V_{OOS_shift2}	Output offset voltage shift	All gains, excluding preamp step			12.7		mV
TCV_{OOS}	Output offset voltage drift(6)	Preamp HG, 0-dB ladder			–24		µV/°C
		Preamp LG, 0-dB ladder			–7		
I_B	Input bias current(8)	T_A = –40°C to 85°C			40	100	µA
		T_A = –65°C to 150°C				140	
V_{OCM}	Output CM voltage	All gains	T_A = –40°C to 85°C		1.2		V
			T_A = –65°C to 150°C	0.95		1.45	
V_{OS_CM}	Output CM offset	All gains			±15	±30	mV
$TC\_V_{OS\_CM}$	CM offset voltage temperature coefficient	All gains			+55		µV/°C
BAL_Error_DC	Output gain balance error	DC, $\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$			–78		dB
BAL_Error_AC	Output gain balance error	250 MHz, $\frac{V_{O\_CM}}{V_{OUT}}$			–45		dB
PB	Phase balance error (see Table 8)	250 MHz			±0.8		deg
PSRR	Differential power supply rejection (see Table 8)	Preamp HG, 0-dB ladder		–60	–87		dB
		Preamp LG, 0-dB ladder		–50	–70		
PSRR_CM	CM power supply rejection (see Table 8)	Preamp LG, 0-dB ladder		–55	–71		dB
V_{CM_I}	V_{CM} input bias current(8)	All gains	T_A = –40°C to 85°C		±1	±10	nA
			T_A = –65°C to 150°C			±20	
$V_{CM\_AUX\_I}$	V_{CM_AUX} input bias current(8)	All gains	T_A = –40°C to 85°C		±1	±10	nA
			T_A = –65°C to 150°C			±20	
DIGITAL I/O							
V_{IH}	Input logic high	T_A = –65°C to 150°C		V_{DD}–0.6			V
V_{IL}	Input logic low	T_A = –65°C to 150°C				0.5	V
V_{OH}	Output logic high				V_{DD}		V
V_{OL}	Output logic low				0		V
R_{Hi_Z}	Output resistance	High impedance mode			5		MΩ
I_in	Input bias current				<1		µA
F_{SCLK}	SCLK rate					10	MHz
F_{SCLK_DT}	SCLK duty cyle			45%	50%	55%	

(8) Positive current is current flowing into the device.

Electrical Characteristics (continued)

Unless otherwise noted, all limits are ensured for T_A = 25°C, input CM = 2.5 V, V_{CM} = 1.2 V, V_{CM_Aux} = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), both main and auxiliary output specifications, full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on) (see Table 8 for abbreviations used).(1)

PARAMETER		TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER REQUIREMENTS							
I_{S1}	Supply current, V_{CC}	T_A = –40°C to 85°C		195	210	225	mA
		T_A = –65°C to 150°C				230	
I_{S1_off}	Supply current, V_{CC} aux off	T_A = –40°C to 85°C			150	165	mA
		T_A = –65°C to 150°C				170	
I_{DD}	Supply current, V_{DD}	T_A = –40°C to 85°C			180	350	µA
		T_A = –65°C to 150°C				400	
BANDWIDTH LIMITING FILTER SPECIFICATIONS							
Pass band tolerance, –3 dB bandwidth		All gains	20 MHz	0%	20%		
			100 MHz	0%	20%		
			200 MHz	0%	20%		
			350 MHz		±25%		
			650 MHz		±25%		
			750 MHz		±25%		
		Preamp LG, 0-dB ladder	350 MHz		±10%		
			650 MHz		±10%		
			750 MHz		±10%		

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
T_S	SDIO setup time	25			ns
T_H	SDIO hold time	25			ns
T_{CES}	$\overline{CS}$ enable setup time (from $\overline{CS}$ asserted to rising edge of SCLK)	25			ns
t_{CDS}	$\overline{CS}$ disable setup time (from $\overline{CS}$ de-asserted to rising edge of SCLK)	25			ns
T_{IAG}	Inter-acess gap	3			SCLK cycles

6.7 Typical Characteristics

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

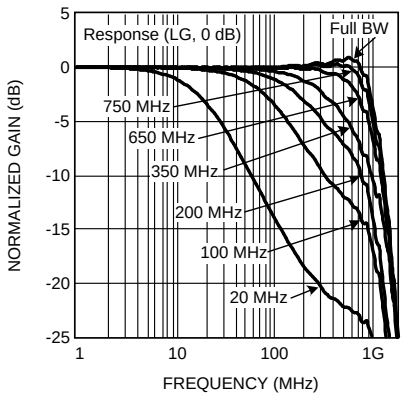


Figure 1. Response (LG, 0 dB)

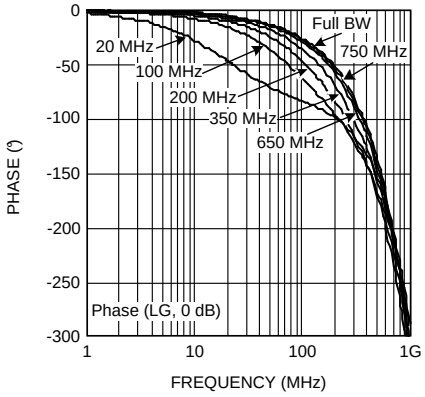


Figure 2. Phase (LG, 0 dB)

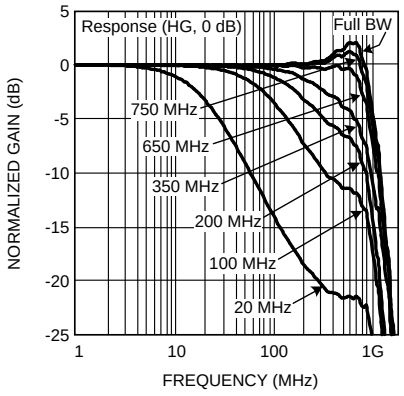


Figure 3. Response (HG, 0 dB)

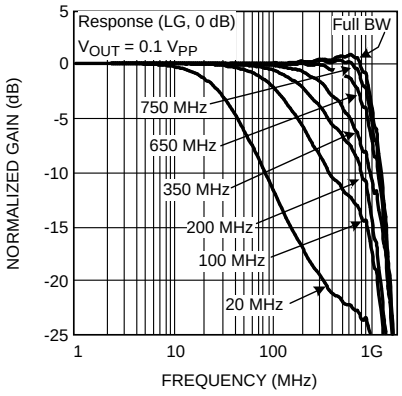


Figure 4. Small Signal Response (LG, 0 dB)

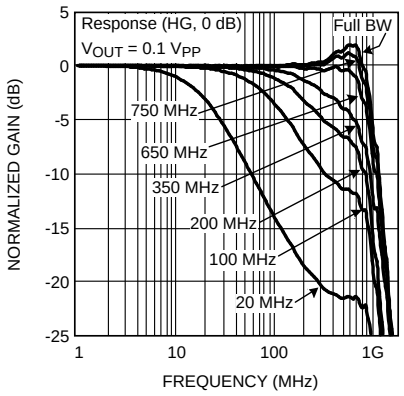


Figure 5. Small Signal Response (HG, 0 dB)

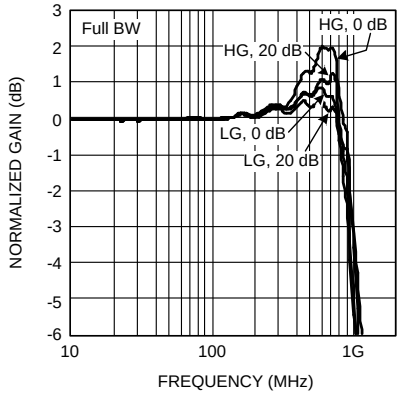


Figure 6. Response vs Gain

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

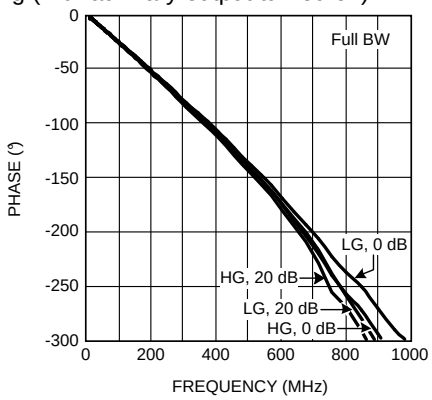


Figure 7. Phase vs Gain

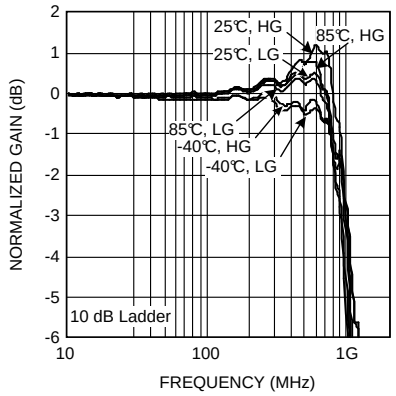


Figure 8. Response Over Temperature

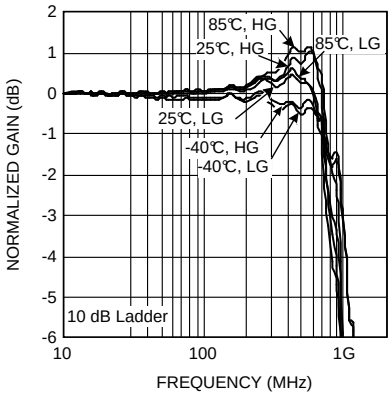


Figure 9. Auxiliary Response Over Temperature

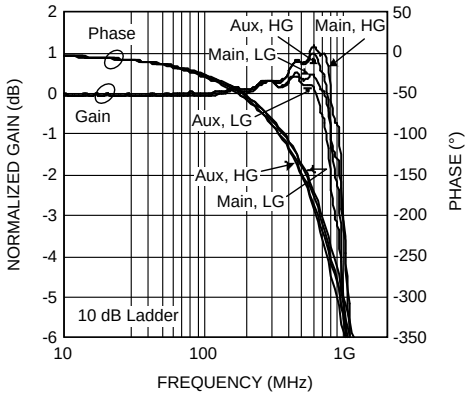


Figure 10. Main vs Auxiliary Response

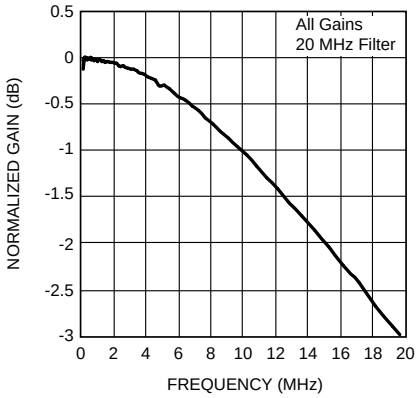


Figure 11. Response vs Gain

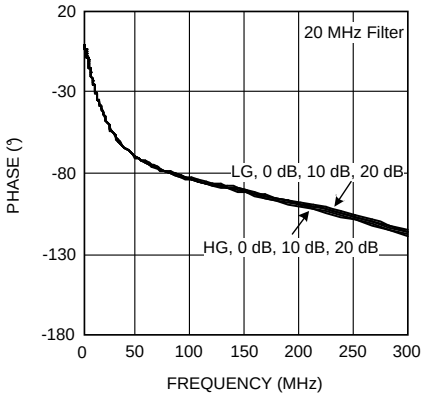


Figure 12. Phase vs Gain

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

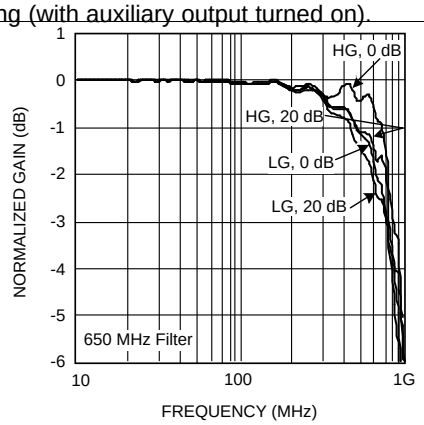


Figure 13. Response vs Gain

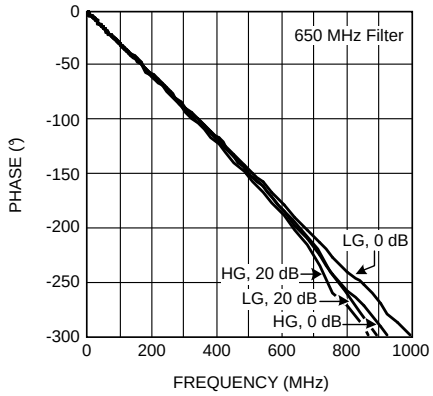


Figure 14. Phase vs Gain

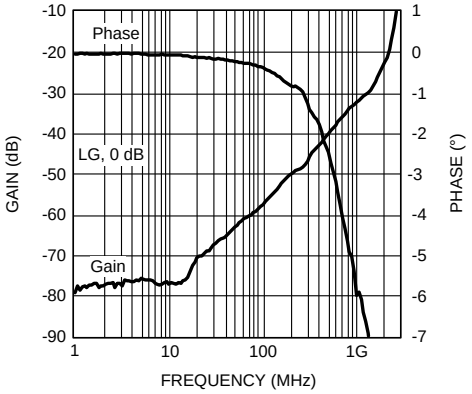


Figure 15. Balance Error

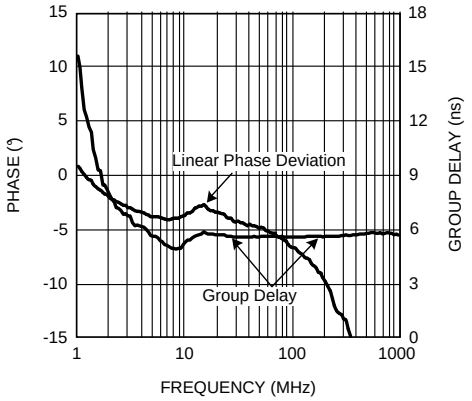


Figure 16. Linear Phase Deviation and Group Delay

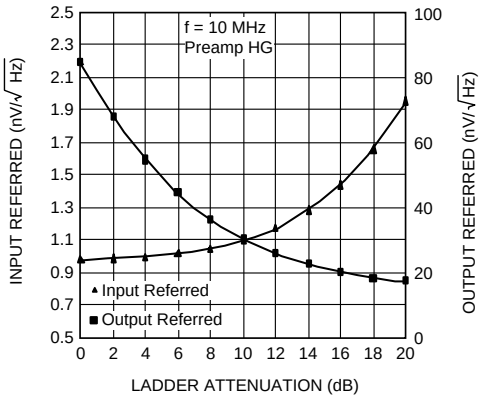


Figure 17. Noise vs Ladder Attenuation

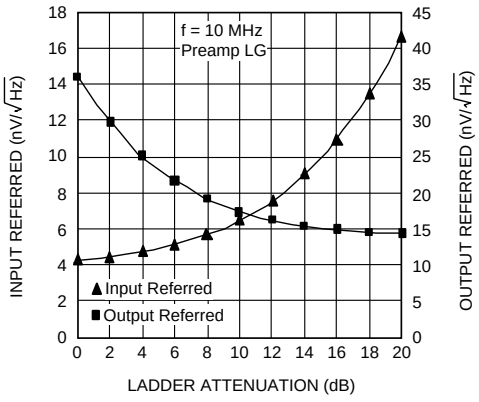


Figure 18. Noise vs Ladder Attenuation

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

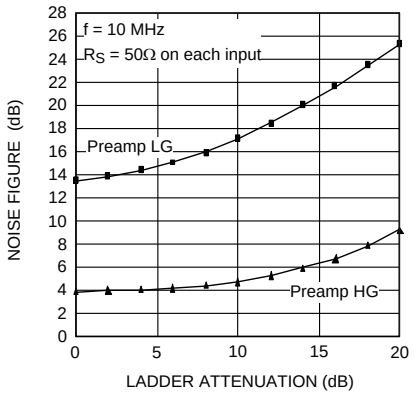


Figure 19. Noise Figure vs Gain

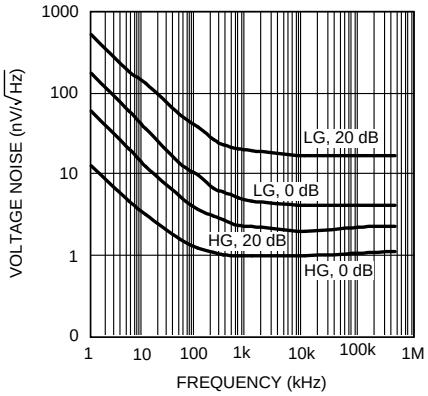


Figure 20. Input Voltage Noise vs Frequency

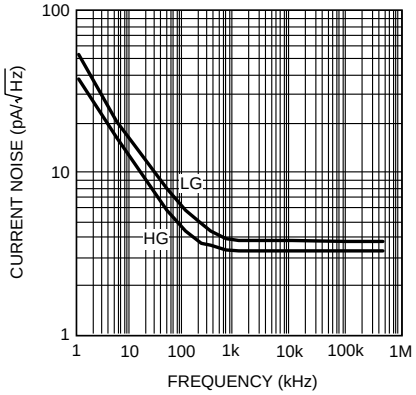


Figure 21. Input Current Noise vs Frequency

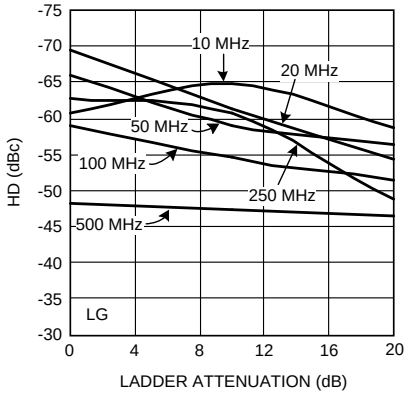


Figure 22. HD2 vs Ladder Attenuation

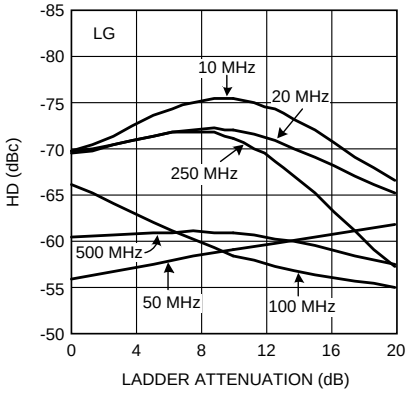


Figure 23. HD3 vs Ladder Attenuation

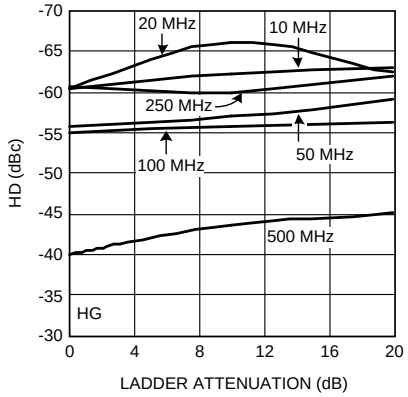


Figure 24. HD2 vs Ladder Attenuation

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

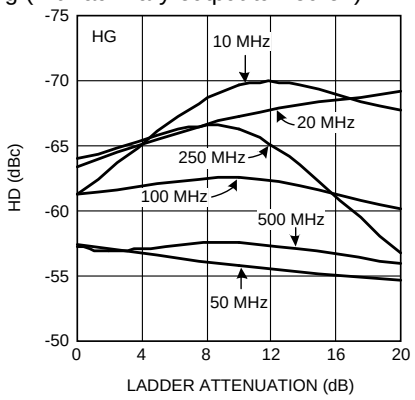


Figure 25. HD3 vs Ladder Attenuation

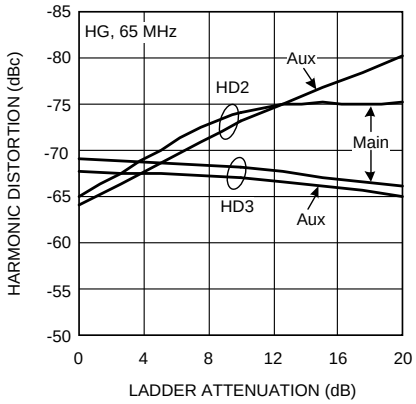


Figure 26. Main and Auxiliary Distortion Comparison

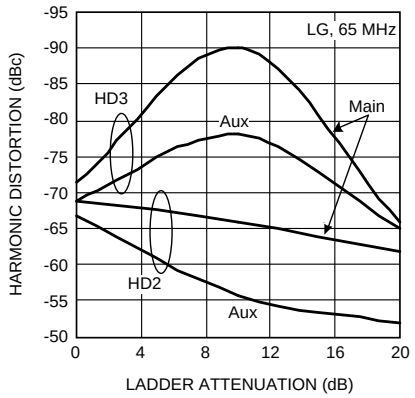


Figure 27. Main and Auxiliary Distortion Comparison

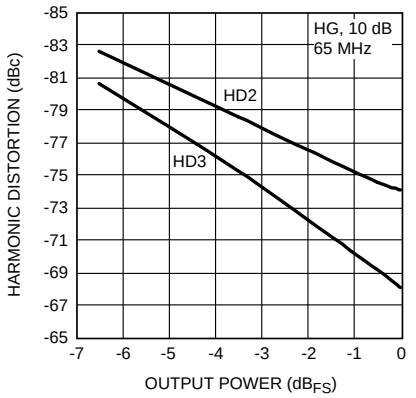


Figure 28. Distortion vs Output Power

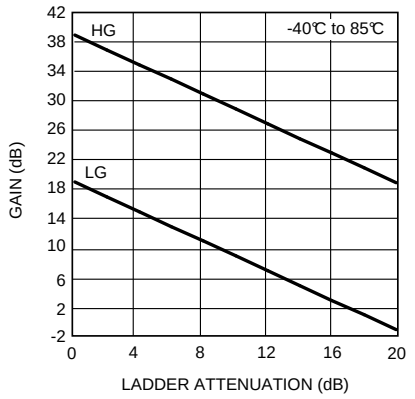


Figure 29. Gain vs Ladder Attenuation

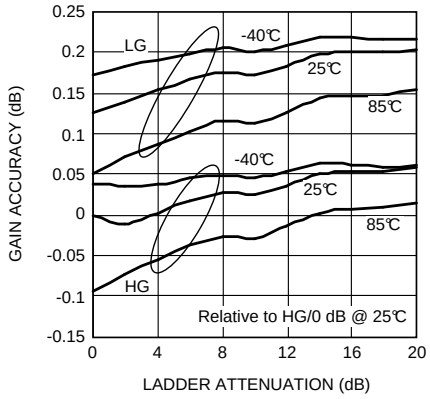


Figure 30. Gain Accuracy vs Ladder Attenuation

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

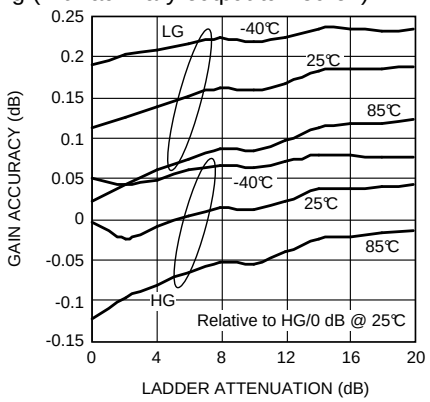


Figure 31. Auxiliary Gain Accuracy vs Ladder Attenuation

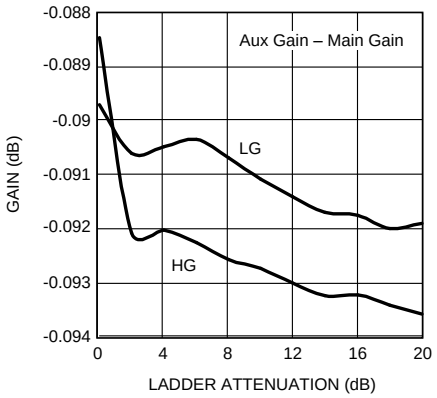


Figure 32. Gain Matching vs Ladder Attenuation

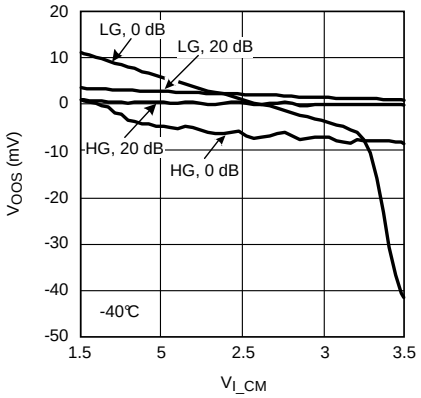


Figure 33. A_{V_CM}

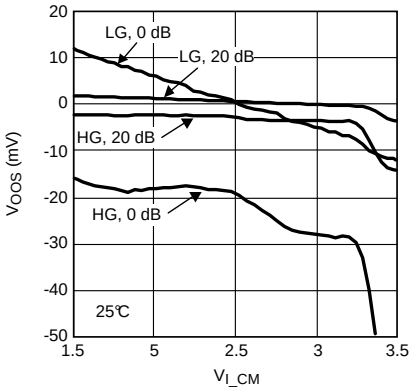


Figure 34. A_{V_CM}

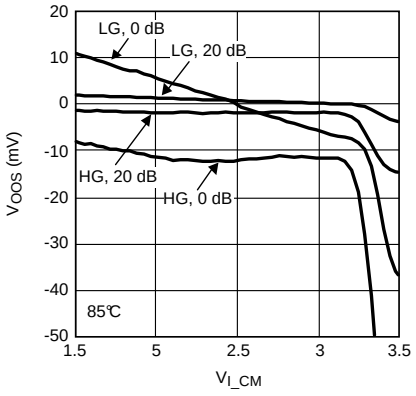


Figure 35. A_{V_CM}

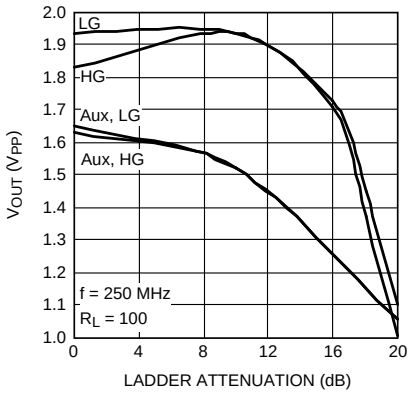


Figure 36. –1 dB Compression vs Ladder Attenuation

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

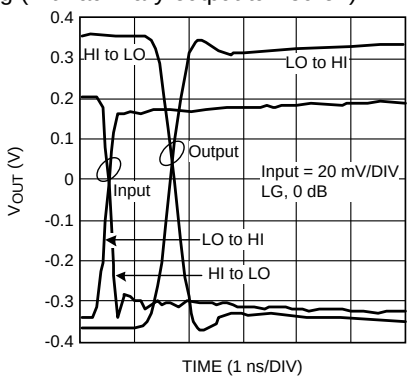


Figure 37. Step Response

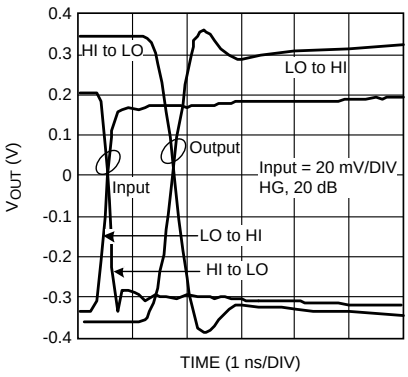


Figure 38. Step Response

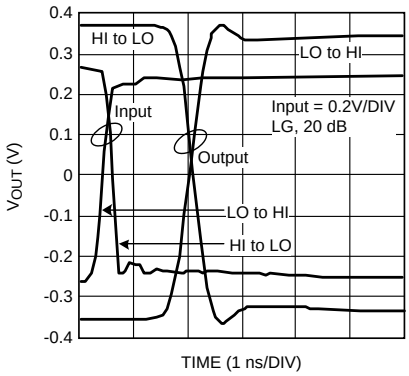


Figure 39. Step Response

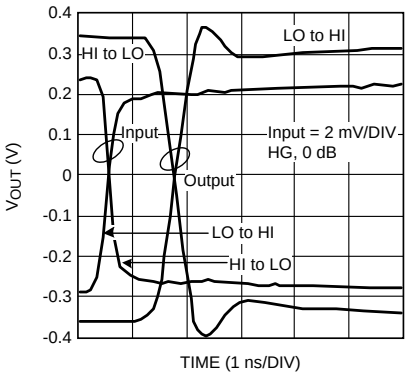


Figure 40. Step Response

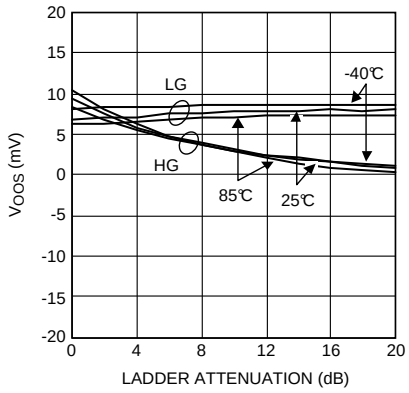


Figure 41. Output Offset Voltage (Typical Unit 1)

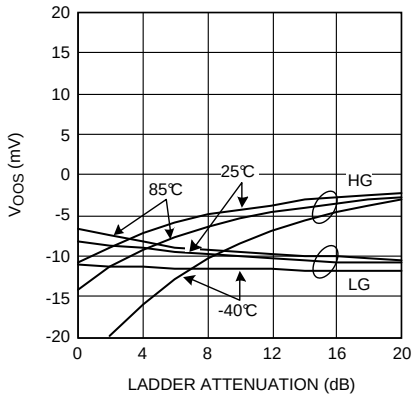


Figure 42. Output Offset Voltage (Typical Unit 2)

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

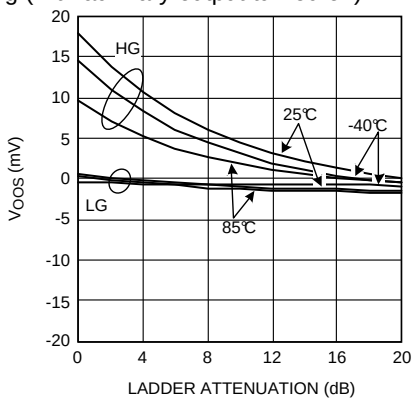


Figure 43. Output Offset Voltage (Typical Unit 3)

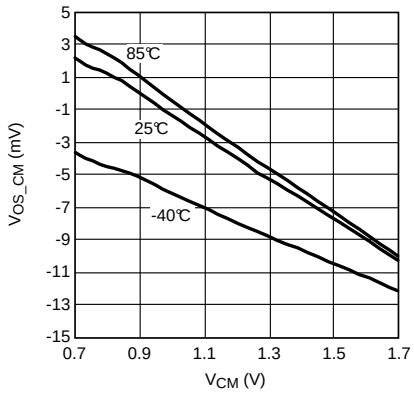


Figure 44. V_{OS_CM} vs V_{CM}

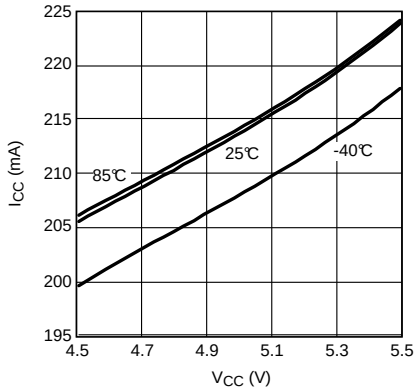


Figure 45. Supply Current vs Supply Voltage

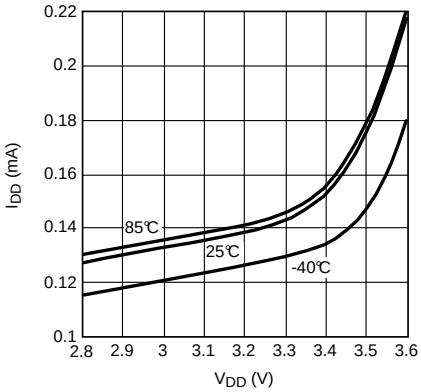


Figure 46. Supply Current vs Supply Voltage

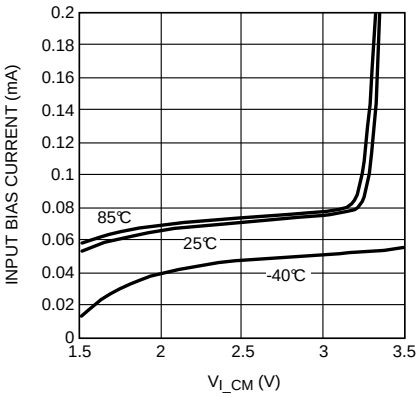


Figure 47. Input Bias Current vs Input CM

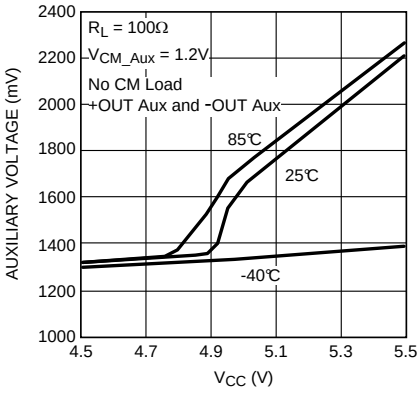


Figure 48. Auxiliary Output Voltage (Hi-Z Mode)

Typical Characteristics (continued)

Unless otherwise noted, input CM = 2.5 V, V_{CM} = 1.2 V, $V_{CM\ AUX}$ = 1.2 V, single-ended input drive, V_{CC} = 5 V, V_{DD} = 3.3 V, R_L = 100 Ω differential (both main and auxiliary outputs), V_{OUT} = 0.7 V_{PP} differential (both main and auxiliary outputs), main output specification (auxiliary is labeled), full bandwidth setting, gain = 18.8 dB (preamp LG, 0 dB ladder attenuation), and full power setting (with auxiliary output turned on).

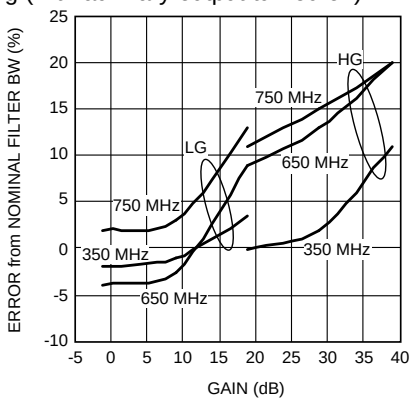


Figure 49. Filter BW vs Gain

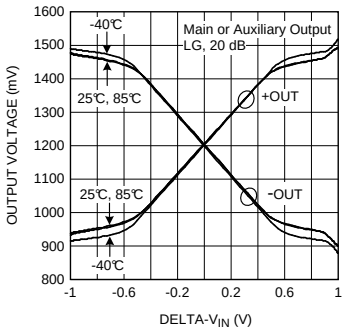


Figure 50. Output vs Input

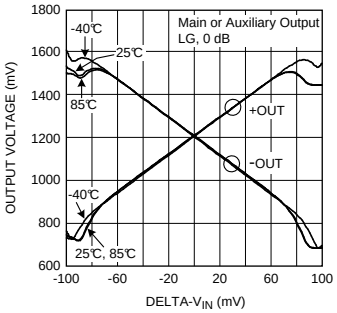


Figure 51. Output vs Input

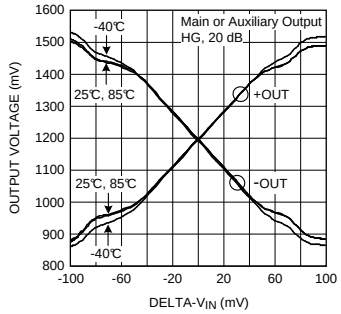


Figure 52. Output vs Input

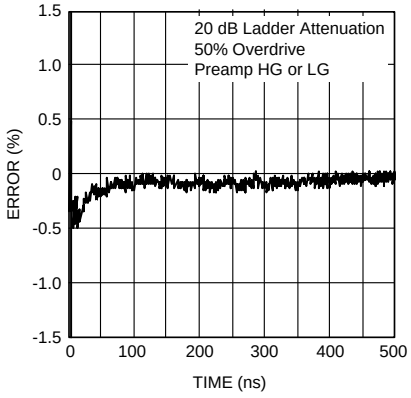


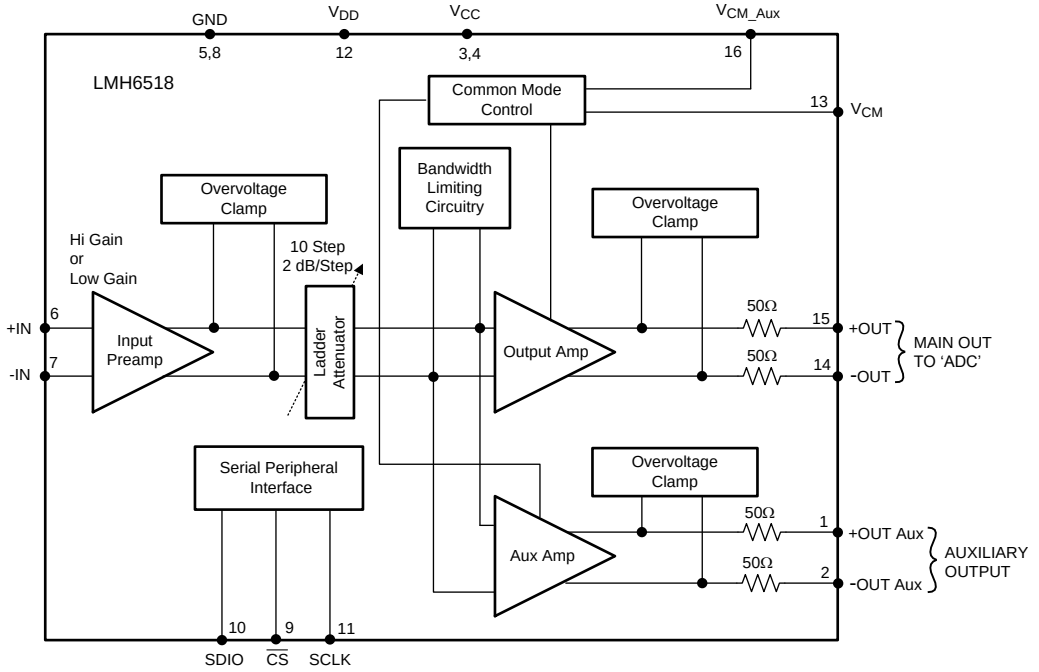
Figure 53. Overdrive Recovery Time (Return to Zero)

7 Detailed Description

7.1 Overview

The LMH6518 device is a digitally-controlled variable gain amplifier (DVGA) which is designed specifically as an oscilloscope analog front end (AFE). This device samples an analog voltage and conditions it for the analog to digital converter (ADC) input. It is specifically designed to drive TI's giga sample ADCs which have 100-Ω input impedance and 800-mV_{PP} full scale input voltage.

7.2 Functional Block Diagram



7.3 Feature Description

The LMH6518 offers several unique features in addition to being a general purpose digital variable gain amplifier (DVGA).

7.3.1 Input Preamplifier

The LMH6518 has a fully differential preamplifier which has a consistent 150-kΩ impedance across all gain settings. The LMH6518 is also driven with a single-ended signal source. The preamplifier has two gain settings. See *Input and Output Considerations* for details.

7.3.1.1 Primary Output Amplifier

The LMH6518 has two nearly identical amplifiers. The output amplifier was designed as the primary output amplifier. It features an internal 100-Ω termination for interfacing with 100-Ω input impedance ADCs. The output amplifier has a common mode voltage control pin which sets the output common mode of the amplifier.

7.3.1.2 Auxiliary Amplifier

The LMH6518 has a second output amplifier that was designed to provide a trigger signal when used as an oscilloscope AFE. The auxiliary amplifier has all of the features of the output amplifier and provides a duplicate signal for use in trigger circuits. The auxiliary amplifier has a common mode voltage control pin which sets the output common mode of the amplifier.

Feature Description (continued)

7.3.2 Overvoltage Clamp

THe LMH6518 features two levels of clamps used to protect the amplifier and the ADC from voltage transients. These clamps are placed after the input preamplifier and also after the final output amplifier. The clamp voltages are set using the SPI bus.

7.3.3 Attenuator

The primary gain control feature of the LMH65418 is the digital attenuator. The attenuator controls the overall gain of the amplifier. The attenuator has a range of 0 dB to 20 dB of attenuation.

7.3.4 Digital Control Block

The LMH6518 has digitally controlled gain as well as digitally controlled voltage clamps and digitally controlled bandwidth. If it is not used, this block can also disable the auxiliary amplifier. *Logic Functions* has details on the digital control registers and programming.

7.4 Device Functional Modes

7.4.1 Primary Amplifier

The main functional mode of the LMH6518 is as an AFE providing gain, voltage clamping, and frequency limiting. In this mode, the gain, bandwidth, and voltage swing are all programmable using the SPI control block.

7.4.2 Auxiliary Output

The secondary functional mode of the LMH6518 is the auxiliary output. This output is nearly identical to the primary amplifier. The only difference is that the auxiliary output has slightly lower distortion performance. The auxiliary output was designed to provide a trigger signal when used as an oscilloscope AFE.

7.5 Programming

7.5.1 Logic Functions

The following LMH6518 functions are controlled using the SPI-1 compatible bus:

- Filters (20, 100, 200, 350, 650, 750 MHz or full bandwidth)
- Power mode (Full power or auxiliary high impedance, Hi-Z)
- Preamp (HG or LG)
- Attenuation ladder (0 dB to 20 dB, 10 states)
- LMH6518 state *write* or *read* back

The SPI-1 bus uses 3.3-V logic. *SDIO* is the serial digital input-output which writes to the LMH6518 or reads back from it. *SCLK* is the bus clock with chip select function controlled by $\overline{CS}$.

Programming (continued)

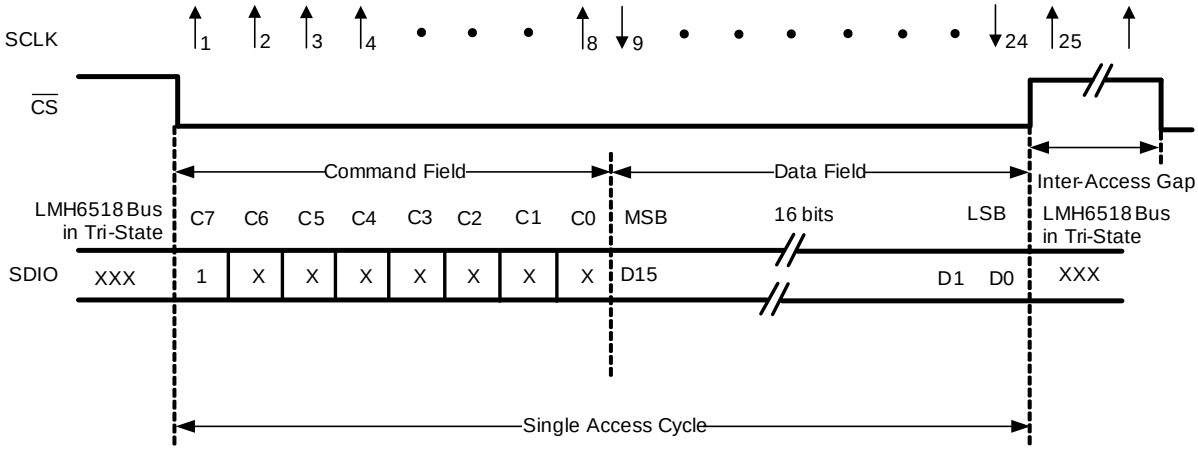


Figure 54. Serial Interface Protocol, Read Operation

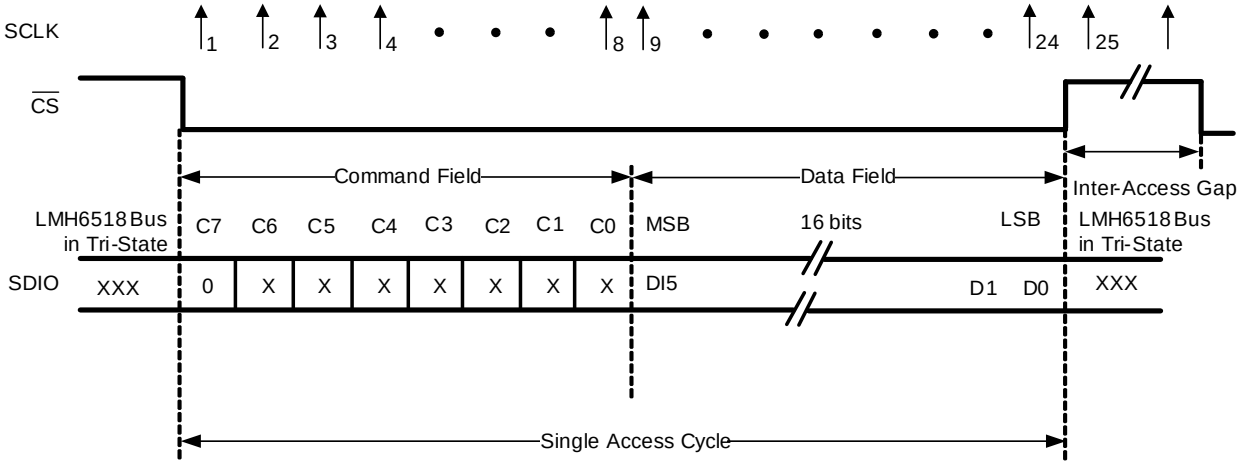


Figure 55. Serial Interface Protocol, Write Operation

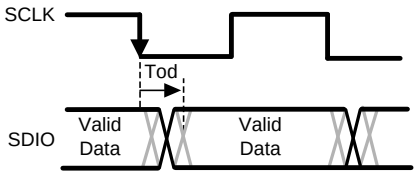


Figure 56. Read Timing

Programming (continued)

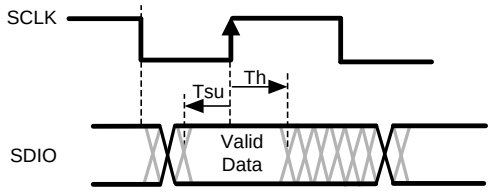


Figure 57. Write Timing

Table 1. Data Field

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
X	0	0	0	0	0 = Full power 1 = Aux Hi-Z	0	See Table 3			0	0 = LG 1 = HG	See Table 4			

NOTE

Bits D5, D9, and D11 to D14 must be 0. Otherwise, device operation is undefined and specifications are not ensured.

Table 2. Default Power-On Reset Condition

							FILTER				PREAMP	LADDER ATTENUATION			
D15 (MSB)	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0

Table 3. Filter Selection Data Field

FILTER			BANDWIDTH (MHz)
D8	D7	D6	
0	0	0	Full
0	0	1	20
0	1	0	100
0	1	1	200
1	0	0	350
1	0	1	650
1	1	0	750
1	1	1	Unallowed

NOTE

All filters are low-pass, single pole roll-off and operate on both main and auxiliary outputs. These filters are intended as signal path bandwidth and noise limiting.

Table 4. Ladder Attenuation Data Field

LADDER ATTENUATION				BANDWIDTH (dB)
D3	D2	D1	D0	
0	0	0	0	0
0	0	0	1	−2
0	0	1	0	−4
0	0	1	1	−6
0	1	0	0	−8
0	1	0	1	−10
0	1	1	0	−12
0	1	1	1	−14
1	0	0	0	−16
1	0	0	1	−18
1	0	1	0	−20
1	0	1	1	Unallowed
1	1	0	0	Unallowed
1	1	0	1	Unallowed
1	1	1	0	Unallowed
1	1	1	1	Unallowed

NOTE

An *unallowed* SPI-1 state may result in undefined operation where device behavior is not ensured.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMH6518 device is ideal in applications that require a differential signal path and drive a differential, high-bandwidth analog to digital converter. The LMH6581 has 900 MHz of bandwidth and drives signals up to 1.8 V_{PP}.

Typical applications for the LMH6518 include an oscilloscope AFE, gain control in a radio receiver, and a data acquisition system.

8.2 Typical Application

8.2.1 Oscilloscope Front End

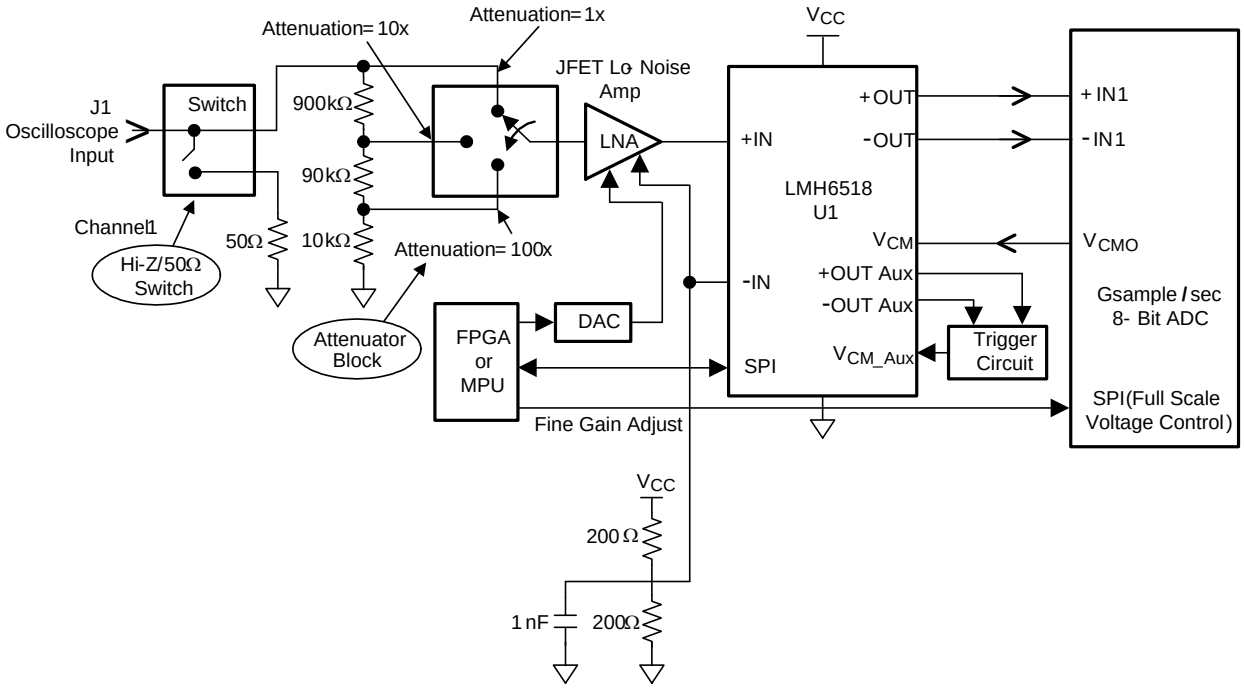


Figure 58. Digital Oscilloscope Front-End

8.2.1.1 Design Requirements

An oscilloscope is used to sample signals from millivolts to volts. To make the best use of the limited ADC input range, the oscilloscope input circuitry must have a wide gain range.

In this design example, the LMH6518 is driving an ADC12J2700 and has the following requirements:

- Common mode voltage = 1.225 V
- Full scale voltage = 650 mV_{PP} to 800 mV_{PP}
- Bandwidth = 900 MHz
- Trigger channel
- Spurious free dynamic range = 50 dB

Typical Application (continued)

8.2.1.2 Detailed Design Procedure

Figure 59 shows a block diagram of the LMH6518's main output signal path.

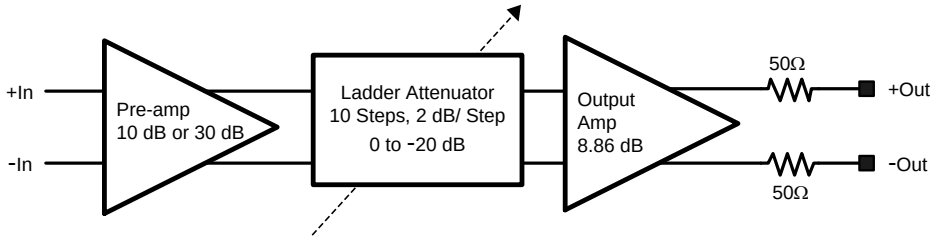


Figure 59. LMH6518 Signal Path Block Diagram

The auxiliary output (not shown) uses another but similar output amplifier that taps into the ladder attenuator output. In this data sheet, preamp gain of 30 dB is referred to as high gain (HG), and preamp gain of 10 dB as low gain (LG).

The LMH6518 2-dB/step gain resolution and 40-dB adjustment range (from −1.16 dB to 38.8 dB) allows this device to be used with the TI Gsps ADCs which have full scale (FS) adjustment through their extended control mode (ECM) to provide near-continuous variability (8.5-mdB resolution) which covers 42.6 dB FS input range using Equation 1.

$$\left(20 \times \log \frac{920\ mV_{PP}}{6.8\ mV_{PP}} = 42.6\ dB\right) \tag{1}$$

TI's Gsps ECM control allows the ADC FS to be set using the ADC SPI bus. The ADC FS voltage range is from 560 mV to 840 mV with 9 bits of FS voltage control.

The ADC ECM gain resolution is calculated with Equation 2.

$$\text{Gain Resolution} = 20 \log \frac{0.56 + \left(\frac{0.84 - 0.56}{2 \times 512}\right)}{0.56 - \left(\frac{0.84 - 0.56}{2 \times 512}\right)} = 8.5\ mdB \tag{2}$$

However, the *recommended* ADC FS operating range is narrower; it is from 595 mV to 805 mV with 700 mV_{PP} as the mid-point. Raising the value of ADC FS voltage is tantamount to reducing the signal path gain to accommodate a larger input and vice versa, thus providing a method of gain fine-adjust. The ADC ECM gain adjustment is −1.21 dB as in Equation 3.

$$\left(= 20 \times \log \frac{700\ mV}{805\ mV}\right) \text{ to } +1.41\ dB$$

$$\left(= 20 \times \log \frac{700\ mV}{595\ mV}\right) \tag{3}$$

Because the ADC FS fine-adjust range of 2.62 dB (= 1.41 dB + 1.21 dB) is larger than the LMH6518's 2-dB/step resolution, there is always at least one LMH6518 gain setting to accommodate any FS signal from 6.8 mV_{PP} to 920 mV_{PP}, at the LMH6518 input, with 0.62 dB (= 2.62-2) overlap.

Typical Application (continued)

Assuming a nominal 0.7-V_{PP} output, the LMH6518's minimum FS input swing is limited by the maximum signal path gain possible and vice versa with Equation 4.

$$\text{Maximum LMH6518 FS Input} \frac{0.7\ V_{PP}}{10\left(\frac{(38.8+1.41)\ dB}{20}\right)} = 6.8\ mV_{PP} \tag{4}$$

(or 8 mV_{PP} with no ADC fine adjust in Equation 5)

$$\text{Maximum LMH6518 FS Input} \frac{0.7\ V_{PP}}{10\left(\frac{(-1.16-1.21)\ dB}{20}\right)} = 920\ mV_{PP} \tag{5}$$

(or 800 mV_{PP} with no ADC FS adjust)

To accommodate a higher FS input, an additional attenuator is required before the LMH6518. This front-end attenuator is shown in the Figure 58 with its details shown in Figure 69. The highest minimum attenuation level is determined by the largest FS input signal (FS_{max}) in Equation 6.

$$\text{Attenuation (dB)} = 20 \times \log \frac{FS_{MAX}\ (V_{PP})}{800\ mV_{PP}} \tag{6}$$

So, to accommodate 80 V_{PP}, 40 dB minimum attenuation is required before the LMH6518.

In a typical oscilloscope application, the voltage range encountered is from 1 mV/DIV to 10 V/DIV with 8 vertical divisions visible on the screen. One of the primary concerns in a digital oscilloscope is SNR which translates to display trace width to thickness. Typically, oscilloscope manufacturers require the noise level to be low enough so that the *no-input* visible trace width is less than 1% of FS. Experience shows that this corresponds to a minimum SNR of 52 dB.

The factors that influence SNR are:

- Scope front end noise (Front-end attenuator + scope probe Hi-Z buffer which is discussed later in this data sheet and shown in Figure 58)
- LMH6518
- ADC

LMH6518 related SNR factors are:

- Bandwidth
- Preamp used (Preamp HG or LG)
- Ladder attenuation
- Signal level

SNR increases with the inverse square root of the bandwidth. So, reducing bandwidth from 450 MHz to 200 MHz, for example, improves SNR by 3.5 dB as seen in Equation 7.

$$\left(20 \times \log \frac{\sqrt{450\ MHz}}{\sqrt{200\ MHz}} = 3.5\ dB\right) \tag{7}$$

The other factors listed above, preamp and ladder attenuation, depend on the signal level and also impact SNR. The combined effect of these factors is summarized in Figure 60, where SNR is plotted as a function of the LMH6518 FS input voltage (assuming scope bandwidth of 200 MHz) and not including the ADC and the front end noise.

Typical Application (continued)

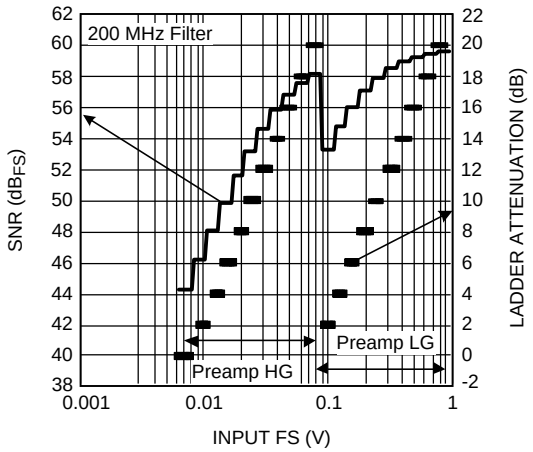


Figure 60. LMH6518 SNR and Ladder Attenuation Used vs Input

As seen in Figure 60, SNR of at least 52 dB is maintained for FS inputs above 24 mV_{PP} (3 mV/DIV on a scope) assuming the LMH6518's internal 200 MHz filter is enabled. Most oscilloscope manufacturers relax the SNR specifications to 40 dB for the highest gain (lowest scope voltage setting). From Figure 60, LMH6518's minimum SNR is 43.5 dB, thereby meeting the relaxed SNR specification for the lower range of scope front panel voltages.

In Figure 60, the step-change in SNR near Input FS of 90 mV_{PP} is the transition point from preamp LG to preamp HG with a subsequent 3 dB difference due to the preamp HG to 20-dB ladder attenuation's lower output noise compared to preamp LG to 2-dB ladder attenuation's noise. Judicious choice of front-end attenuators ensures that the 52-dB SNR specification is maintained for scope FS inputs ≥24 mV_{PP} by confining the LMH6518 gain range to the lower 30.5 dB using Equation 8 from the total range of 40 dB (= 38.8 – (−1.16)) is possible.

$$(= 20 \times \log \frac{0.8\ V_{PP}}{24\ mV_{PP}}) \tag{8}$$

For example, to cover the range of 1 mV/DIV to 10 V/DIV (80 dB range), Table 5 lists a configuration which affords good SNR.

Table 5. Oscilloscope Example Including Front-End Attenuators

ROW	SCOPE FS INPUT (V_{PP})	*S*, SCOPE VERTICAL SCALE (V/DIV)	PREAMP	LADDER ATTENUATION RANGE (dB)	*A*, FRONT-END ATTENUATION (V/V)	MINIMUM SNR (dB) WITH 200 MHz FILTER
1	8 m to 24 m	1 m to 3 m	HG	0 to 10	1	44
2	24 m to 80 m	3 m to 10 m	HG	10 to 20	1	52
3	80 m to 0.8	10 m to 0.1	LG	0 to 20	1	53.4
4	0.8 to 8	0.1 to 1	LG	0 to 20	10	53.4
5	8 to 80	1 to 10	LG	0 to 20	100	53.4

In Table 5, the highest FS input in row 5, column 2 (80 V_{PP}), *and* the LMH6518's highest FS input allowed (0.8 V_{PP}) set the front-end attenuator value with Equation 9.

$$100x\ (= \frac{80\ V_{PP}}{0.8\ V_{PP}}) \tag{9}$$

The 100x attenuator allows high-SNR operation to 30.5 dB down, as explained earlier, or 2.4 V_{PP} at scope input. In that same table, rows 1 to 3 with no front-end attenuation (1x) cover the scope FS input range from 8 mV_{PP} to 800 mV_{PP}. That leaves the scope FS input range of 0.8 V_{PP} to 2.4 V_{PP}. If the 100x attenuator were used for the entire scope FS range of 0.8 V_{PP} to 80 V_{PP}, SNR would dip below 52 dB for a portion of that range. Another attenuation level is thus required to maintain the SNR specification requirement of 52 dB.

One possible attenuation partitioning is to select the additional attenuator value to cover a 20 dB range above 0.8 V_{PP} FS (to 8 V_{PP}) with the 100x attenuator covering the remaining 20 dB range from 8 V_{PP} to 80 V_{PP}. Mapping 8 V_{PP} FS scope input to 0.8 V_{PP} at LMH6518 input means the additional attenuator is 10x, as shown in Table 5, row 4. The remaining scope input range of 8 V_{PP} to 80 V_{PP} is then covered by the 100x front-end attenuator derived earlier. The entire scope input range is now covered with SNR maintained about 52 dB for scope FS input ≥24 mV_{PP}, as shown in Table 5.

8.2.1.2.1 Settings and ADC SPI Code (ECM)

Covering the range from 1 mV/DIV to 10 V/DIV requires the following adjustment within the digital oscilloscope:

- Front-end attenuator
- LMH6518 preamp
- LMH6518 ladder attenuation
- ADC FS value (ECM)

The LMH6518 product folder contains a spreadsheet which allows one to calculate the front-end attenuator, LMH6518 preamp gain (HG or LG), ladder attenuation, and ADC FS setting based on the scope vertical scale (S in V/DIV).

Here is the step-by-step procedure that explains the operations performed by the said spreadsheet based on the scope vertical scale setting (S in V/div) and front-end attenuation *A* (from Table 5). A numerical example is also worked out for more clarification:

1. Determine the required signal path gain, K, with Equation 10:

$$K = 20 \times \log \frac{0.95 \times 700\ mV_{PP}}{\frac{8 \times S(V/div)}{A}} = -21.6 + 20 \times \log \frac{A}{S(V/div)} \quad (10)$$

   (assuming the full scale signal occupies 95% of the 0.7 V_{PP} FS for 5% overhead which occupies 8 vertical scope divisions).

   Required condition: −2.37 dB ≤ K ≤ 40.3 dB

   Example: With S = 110 mV/DIV, Table 5 shows that A = 10 V/V in Equation 11.

$$\rightarrow K = -21.6 + 20 \times \log \frac{10}{110\ mV} = 17.57\ dB \quad (11)$$

2. Determine the LMH6518 gain, G:
   - G is the closest LMH6518 gain, to the value of K where:
   - G = (38.8 – 2n)dB; n = 0, 1, 2, …, 20
   - For this example, the closest G to K = 17.57 dB is 16.8 dB (with n = 11). The next LMH6518 gain, 18.8 dB (with n = 10) is incorrect as 16.8 is closer. If 18.8 dB were mistakenly chosen, the ADC FS setting is out of range.
   - Therefore: *G = 16.8 dB*
3. Determine preamp (HG or LG) and ladder attenuation:
   - If G ≥ 18.8 dB → Preamp is HG and ladder attenuation = 38.8 – G
   - If G < 18.8 dB → Preamp is LG and ladder attenuation = 18.8 – G
   - For this example, with G = 16.8 → *Preamp LG* and *Ladder Attenuation = 2 dB* (= 18.8 to 16.8).
4. Determine the required ADC FS voltage, FS_E, with Equation 12:

$$FS_E = \frac{S \times 8}{A} \times 1.05 \times 10^{\frac{\breve{G}}{20}} \quad (12)$$

   The *1.05* factor is to add 5% FS overhead margin to avoid ADC overdrive with Equation 13.

$$FS_E = \frac{S \times 8}{10} \times 1.05 \times 10^{\frac{16.8}{20}} = 639.3\ mV \quad (13)$$

   Required condition: 0.56 V ≤ FS_E ≤ 0.84 V

Recommend condition: 0.595 V ≤ FS_E ≤ 0.805 V for optimum ADC FS

5. Determine the ADC ECM code ratio with Equation 14:

$$\text{ECM (ratio)} = \frac{FS_E - 0.56}{0.28} \tag{14}$$

where

- 0.28 V = (0.84 – 0.56) V
- 0.56 V is the lower end of the ADC FS adjustability
- For this example:

$$\text{ECM (ratio)} = \frac{0.6393 - 0.56}{0.28} = 0.283$$

   – Required condition: 0 ≤ ECM (ratio) ≤ 1

6. Determine the ECM binary code sent on ADC SPI bus:
   – Convert the ECM value represented by the ratio calculated above, to binary:
   – ECM (binary) = DEC2BIN{ECM(ratio) × 511, 9}
   – Where *DEC2BIN* is a spreadsheet function which converts the decimal ECM ratio, from step 5 above, multiplied by 511 distinct levels, into binary 9 bits.

NOTE

The Web based spreadsheet computes ECM without the use of *DEC2BIN* function to ease usage by all spreadsheet users who may not have this function installed.

   – For this example: ECM (binary) = DEC2BIN(0.283 × 511, 9) = 010010000. This is the number sent to the ADC on the SPI bus to program the ADC to proper FS voltage.

8.2.1.2.2 Input and Output Considerations

The LMH6518's ideal input and output conditions, considered individually, are listed in Table 6.

Table 6. LMH6518's Ideal Input and Output Conditions

IMPEDANCE FROM EACH INPUT TO GROUND (Ω)	COMMON MODE INPUT (V)	DIFFERENTIAL INPUT (V_{PP})	LOAD IMPEDANCE (Ω)	DIFFERENTIAL OUTPUT (V)	COMMON MODE OUTPUT (V)
≤50	1.5 to 3.1	<0.8	100 (differential) and 50 (single-ended)	<0.77	0.95 to 1.45

In addition to the individual conditions listed in Table 6, the input and output terminal conditions must match differentially (that is, +IN to −IN and +OUT to −OUT), as well, for best performance.

The input is differential but is driven single-ended as long as the conditions of Table 6 are met, and there is good matching between the driven and undriven inputs from DC to the highest frequency of interest. If not, there is a settling time impact among other possible performance degradations. The data sheet specifications are with single-ended input, unless specified. Figure 61 is the recommended bench-test schematic to drive one input and to bias the other input with good matching in mind.

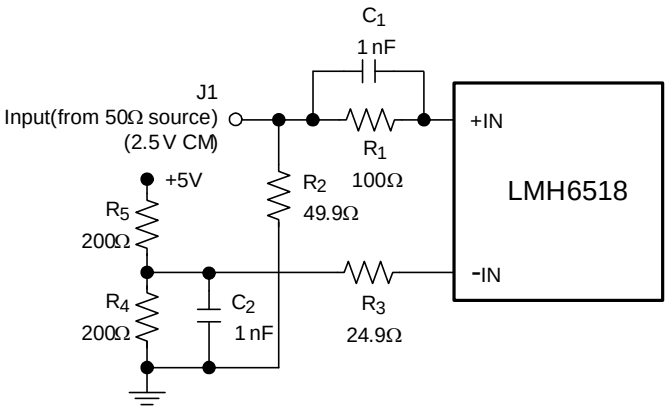


Figure 61. Recommended Single-Ended Bench-Test Input Drive from 50-Ω Source

With Figure 61, each LMH6518 input sees 25 Ω to ground at higher frequencies when the capacitors look like shorts. This impedance increases to 125 Ω at DC for both inputs, thereby preserving the required matching at any frequency. This configuration, using properly selected R's and C's, allows four times less biasing power dissipation than when undriven inputs are biased with an effective 25 Ω from the LMH6518 input to ground.

It is possible to drive the LMH6518 input from a ground-referenced, 50-Ω source by providing level shift circuitry on the driven input. Figure 62 shows a circuit where half the input signal reaches the LMH6518 input while the negative supply voltage (V_{EE}) ensures that the 50Ω source at J1 does not experience any biasing current while providing 50-Ω termination to the source. The driven input (+IN) is biased to 2.5 V (V_{CC}/2) in Figure 62.

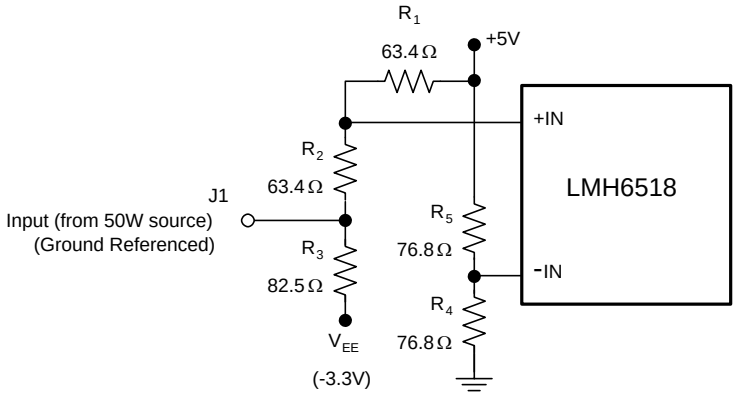


Figure 62. LMH6518 Driven by a Ground Referenced Source

In Figure 62, the equivalent impedance from each LMH6518 input to ground is around 38 Ω. The power consumption of this configuration is approximately 0.5 W (in R_1 – R_5) which is higher than that of Figure 61 because of additional power dissipated to perform the level shifting. Additional 50-Ω attenuators is placed between J1 and R_2/R_3 junction in Figure 62 to accommodate higher input voltages.

It is also possible to shift the LMH6518 *output* common mode level using a level shift approach similar to that of Figure 62. The circuit in Figure 63 shows an implementation where the LMH6518's nominal 1.2 V CM output, set by a 1.2 V on V_{CM} input from the Gsps ADC, is shifted lower for proper interface to different ADCs (which require V_{CM} = 0 V and have high input impedance).

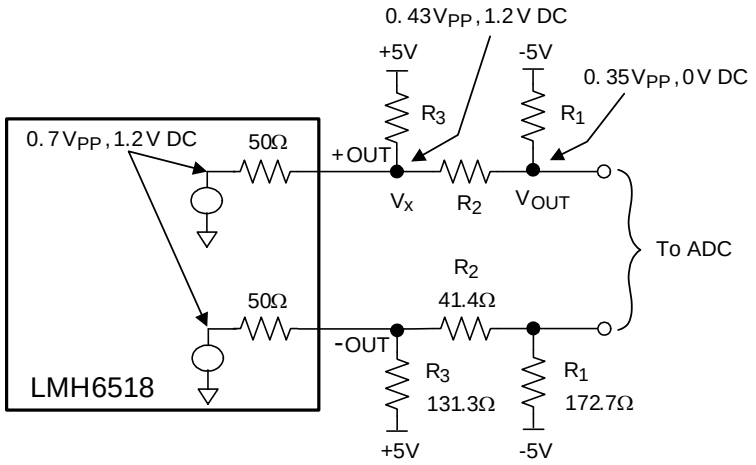


Figure 63. Output CM Shift Scheme

In Figure 63, Vx is kept at 1.2 V by proper selection of external resistor values, so that the LMH6518 outputs are not CM-loaded. As was the case with input level shifting, this output-level shifting also consumes additional power (0.58 W).

8.2.1.2.2.1 Output Swing, Clamping, and Operation Beyond Full Scale

One of the major concerns in interfacing to low voltage ADC's (such as the Gsps ADC that the LMH6518 is intended to drive) is ensuring that the ADC input is not violated with excessive drive. For this reason, plus the important requirement of an oscilloscope to recover quickly and gracefully from an overdrive condition, the LMH6518 is fitted with three overvoltage clamps; one at the preamp output, and one at the main and auxiliary outputs (each). The preamp clamp is responsible for preventing the preamp from saturation (to minimize recovery time) with large ladder attenuation when preamp output swing is at its highest. On the other hand, the output clamps perform this function when ladder attenuation is lower. Therefore, the output amplifier is closer to saturation and prolonged recovery (if not properly clamped). The combination of these clamps results in Figure 50, Figure 51, Figure 52, and Figure 66. With these four graphs, it is possible to observe where output limiting starts due to the clamp action. LMH6518 owes its fast recovery time (<5 ns) from 50% overdrive to the said clamps.

Figure 50, Figure 51, Figure 52, and Figure 66 in *Typical Characteristics* is used to determine the LMH6518 linear swing beyond full scale. This information sets the overdrive limit for both oscilloscope waveform capture and signal triggering. The preamp clamp is set tighter than the output clamp, evidenced by lower output swing with 20-dB ladder attenuation than with 0 dB. With high ladder attenuation (20 dB) defining the limit, the graphs show that the +OUT and −OUT difference of 0.4 V is well inside the clamp range, thereby ensuring 0.8 V_{PP} of unhindered output swing. This corresponds to an overdrive capability of approximately ±7% beyond full scale.

From Figure 58, the signal path consists of the input impedance switch, the attenuator switch, low noise amplifier (LNA, JFET amplifier) to drive the LMH6518 input (+IN), and the DAC to provide offset adjust. The LNA must have the following characteristics:

- Set U1's common mode level to $V_{CC}/2$ (approximately 2.5 V)
- Low drift (1 mV shift at LNA output could translate into 88 mV shift at LMH6518 output at maximum gain, or approximately 13% of FS)
- Low output impedance (≤ 50 Ω) to drive U1 for good settling behavior
- Low noise (<0.98 nV/$\sqrt{\text{Hz}}$) to reduce the impact on the LMH6518 noise figure. Note that Figure 58 does not show the necessary capacitors across the resistors in the front-end attenuators (see Figure 69). These capacitors provide frequency response compensation and limit the noise contribution from the resistors so that they do not impact the signal path noise. For more information about front-end attenuator design, including frequency compensation, see *Related Documentation* for additional resources.
- Gain of 1 V/V (or close to 1 V/V)

- Excellent frequency response flatness from DC to >500 MHz to 800 MHz to not impact the time domain performance

The undriven input (−IN) is biased to $V_{CC}/2$ using a voltage driver. The impedance driving the LMH6518's −IN must be closely matched to the LNA's output impedance for good settling time performance.

JFET LNA Implementation shows one possible implementation of the LNA buffer along with performance data.

When the LMH6518's auxiliary output is not used, it is possible to disable this output using SPI-1 (see *Logic Functions* for SPI register map). *Electrical Characteristics* shows that by doing so, device power dissipation decreases by the reduction in supply current of about 60 mA. As seen in Figure 64, in the absence of heavy common loading, the auxiliary output is at a voltage close to 1.7 V (V_{CC} = 5 V). With higher supply voltages, the auxiliary voltage also increases. It is important to ensure any circuitry tied to this output is capable of handling the 2.3 V possible under V_{CC} worst case condition of 5.5 V.

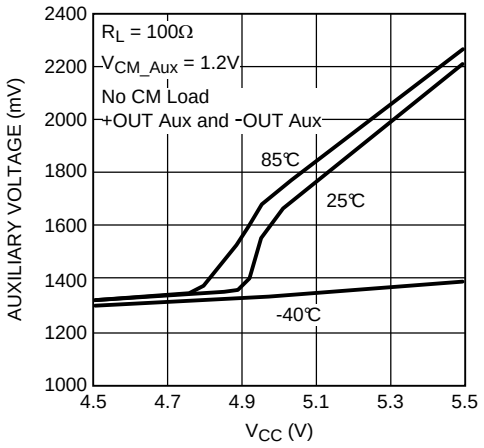


Figure 64. Auxiliary Output Voltage as a Function of V_{CC}

8.2.1.2.3 Oscilloscope Trigger Applications

With the Auxiliary output of the LMH6518 offering a second output that follows the main one (except for a slightly reduced distortion performance), the oscilloscope trigger function is implemented by tapping this output. The auxiliary common mode is set with the V_{CM_Aux} input of the LMH6518. If required, the trigger function is placed at a distance from the main signal path by taking advantage of the differential auxiliary output and rejecting any board related common mode interference pick-up at the receive end.

If trigger circuitry is physically close to the LMH6518, the circuit diagram shown in Figure 65 allows operation using only one of two auxiliary outputs. Unused outputs require proper termination using R_1, R_{11} combination. U3 (DAC101C085) generates a 0- 2.5 V trigger level, with 2.4 mV resolution as in Equation 15 or 0.7% (= 2.4 mV × 100/0.35 V_{PP}) of FS, which is compared to the LMH6518 +OUT AUX by using an ultra-fast comparator, U2 (LMH7220). U2's complimentary LVDS output is terminated in the required 100-Ω load (R_{10}), for best performance, where the LVDS trigger output is available.

$$\left(=\frac{2.5V}{2^{10}}\right) \tag{15}$$

The LMH7220's offset voltage (±9.5 mV) and offset voltage drift (±50 µV/°C) error is 5.9 LSB of the trigger DAC (U3) as in Equation 16.

$$\left(9.5\ mV + 50\ \frac{\mu V}{°C} \times 100℃ = 1.45\ mV \equiv 5.9\ LSB\right) \tag{16}$$

The offset voltage related portion of this error is nulled-out, if necessary, during the oscilloscope initial calibration. To do so, the LMH6518 input is terminated properly with no input applied and U3 output is adjusted around V_{CM_Aux} voltage (1.2 V ±10 mV) while looking for U2's output transition. U3's output, relative to V_{CM_Aux} at transition corresponds to U2's offset error which is factored into the trigger readings and thus eliminated, leaving only the offset voltage temperature drift component (= 2 LSB).

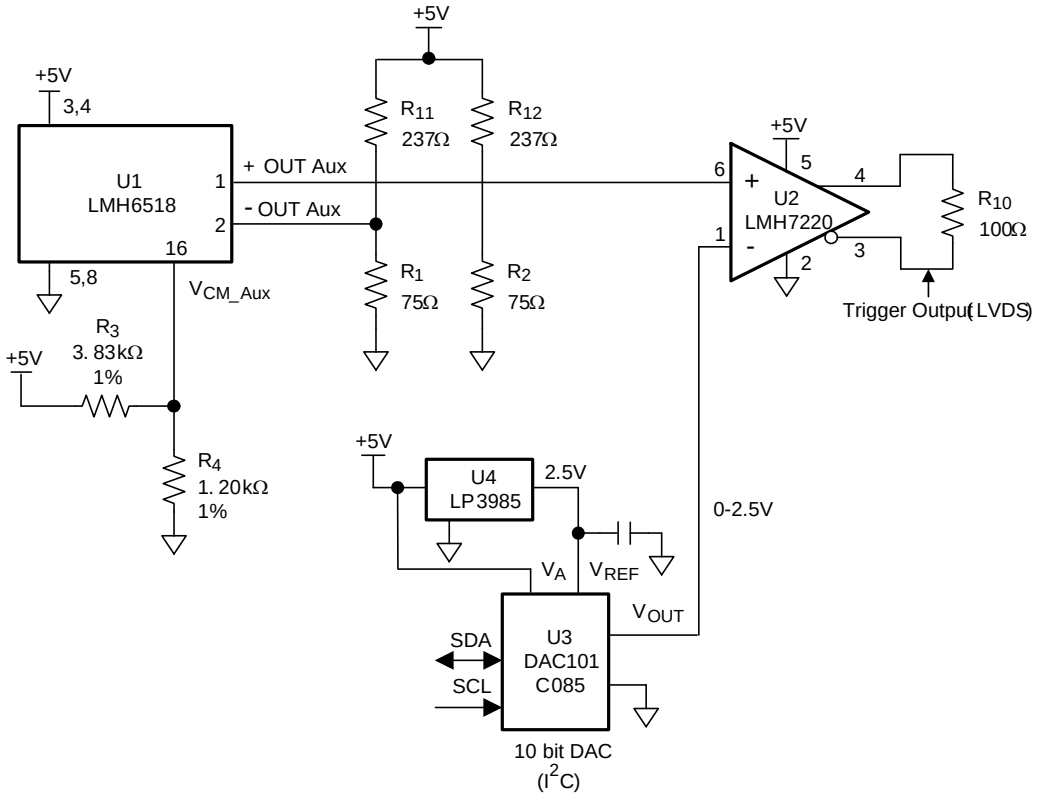


Figure 65. Single-Ended Trigger from LMH6518 Auxiliary Output

U2's minimum toggle rate specification of 750 Mb/s with ±50 mV overdrive allow the oscilloscope to trigger on repetitive waveforms well above the 500 MHz oscilloscope bandwidth applications, when the input signal is at least 14.3% of FS swing with Equation 17.

$$\left(= \frac{50\ mV}{\frac{0.7V}{2}} \times 100\right) \tag{17}$$

The worst case single event minimum discernable pulse width is set by the LMH7220's propagation delay specification of 3.63 ns (20 mV overdrive).

Both the main and the auxiliary outputs recover gracefully and quickly from a 50% overdrive condition as tabulated in *Electrical Characteristics* under overdrive recovery time. However, overdrive conditions beyond 50% could result in longer recovery times due to the interaction between an internal clamp and the common mode feedback loop that sets the output common mode voltage. This may have an impact on both the displayed waveform and the oscilloscope trigger. The result is a loss of trigger pulse or visual distortion of the displayed waveform. To avoid this scenario, the oscilloscope must detect an excessive overdrive and go into trigger-loss mode. Done this way, the oscilloscope display would show the last waveform that did not violate the overdrive condition. Preferably, there is a visual indicator on the screen that alerts the user of the excessive condition, and returns the display to normal once the condition is corrected.

8.2.1.3 Application Curves

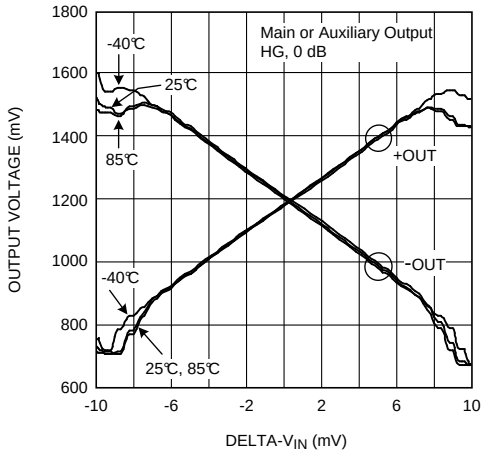


Figure 66. V_{OUT} vs V_{IN}

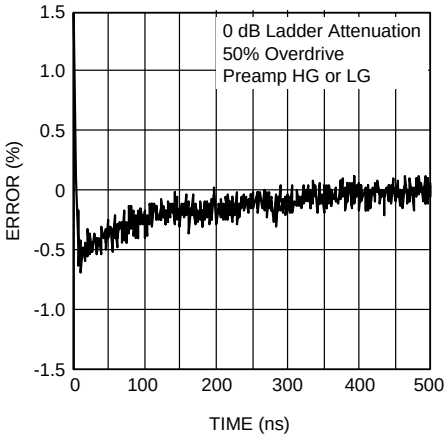


Figure 67. Overdrive Recovery

8.2.2 JFET LNA Implementation

Figure 68 shows the schematic drawing for a possible implementation of the LNA buffer.

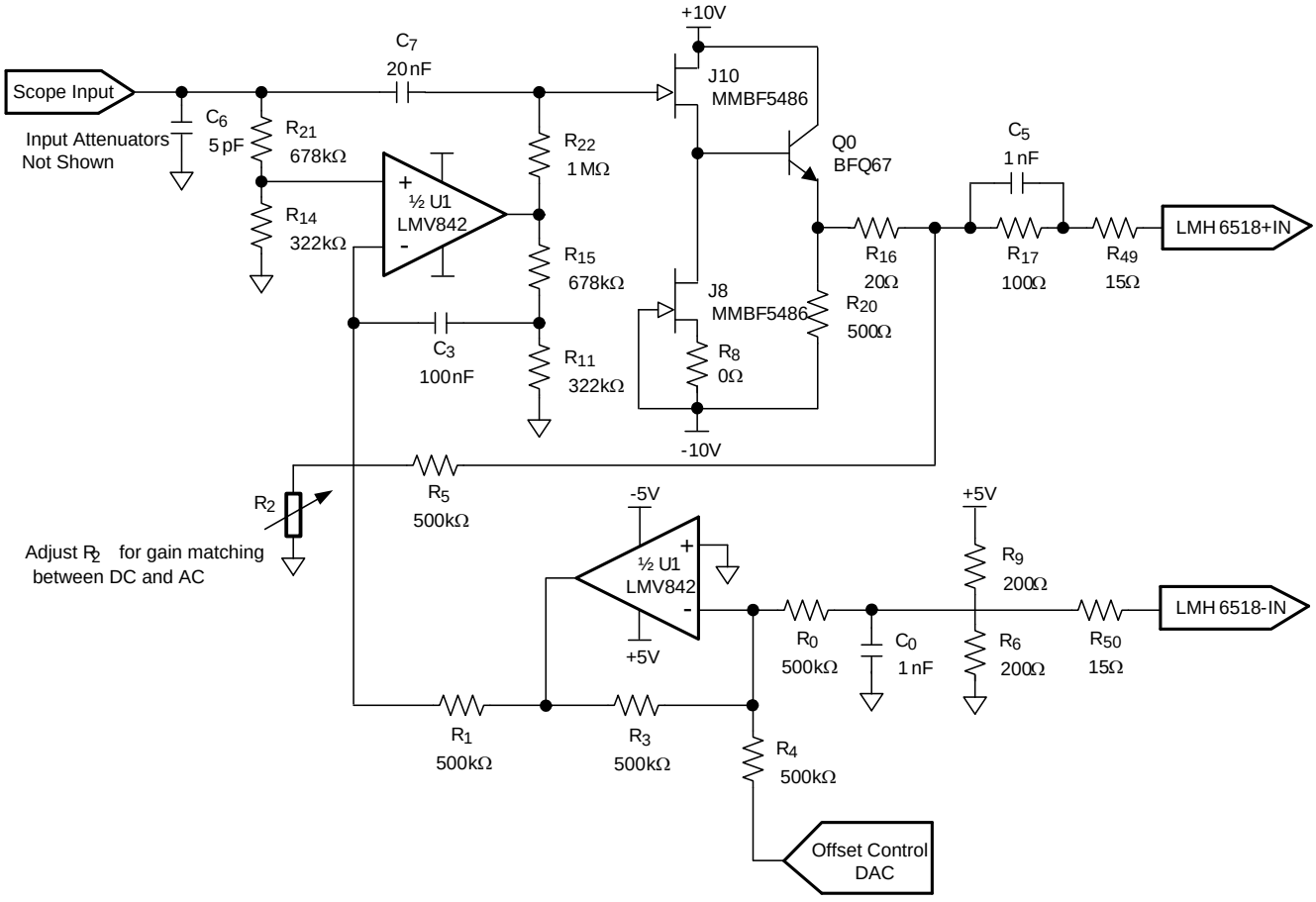


Figure 68. JFET LNA Implementation

8.2.2.1 Design Requirements

This circuit uses an N-Channel JFET (J10) in source-follower configuration to buffer the input signal with J8 acting as a constant current source. This buffer presents a fixed input impedance (1 MΩ||10 pF) with a gain close to 1 V/V.

The signal path is AC-coupled through C_7 with DC (and low frequency) at LMH6518 +IN maintained through the action of U1. NPN transistor Q0 is an emitter follower which isolates the buffer from the load (LMH6518 input and board traces).

The undriven input of the LMH6518 (−IN) is biased to 2.5 V by R_6, R_9 voltage divider. The lower half of U1 inverts this voltage and the upper half of U1 compares it to the combination of the driven output level at LMH6518 +IN and the scaled version of scope input at R_{14}, R_{21} junction, and adjusts J10 Gate accordingly to set the LMH6518 +IN. This control loop has a frequency response that covers DC to a few Hz, limited by the roll-off capacitor C_3 and R_{15} combination (first order approximation). DC and low frequency gain is given by Equation 18.

$$\text{Gain (DC)} = \frac{R_{14}}{R_{14} + R_{21}} \left(1 + \frac{R_5}{R_1 \parallel R_2}\right) \cong 1 \text{ V/V} \tag{18}$$

With the values in Figure 68 → R_2 approximately 452 kΩ.

For a flat frequency response, the DC (low frequency) gain requires lowering to match the less-than-1 V/V AC (high frequency) path gain through the JFETs. This is done by increasing the value of R_2.

Choose values of R_{15} and R_{11} so that the frequency response at J10 Gate (and consequently the output) remain flat when C_7 starts to conduct as in Equation 19.

$$\frac{R_{21}}{R_{14}} = \frac{R_{15}}{R_{11}} \tag{19}$$

Offset correction is done by varying the voltage at R_4, using a DAC or equivalent as shown, to shift the LMH6518 +IN voltage relative to −IN. The result is a circuit which shifts the ground referenced scope input to 2.5 V (V_{CC}/2) CM with adjustable offset and without any JFET or BJT related offsets.

Note that the front-end attenuator (not shown) lower leg resistance is increased for proper divider-ratio to account for the 1-MΩ shunt due to the series combination of R_{21} and R_{14}. For example, a 10:1 front-end attenuator is formed by a series 900 kΩ and a shunt 111 kΩ for a scope BNC input impedance of 1 MΩ (= 900 K + (111 K || 1 M)).

Table 7 lists other possible JFET candidates that fall in the range of speed (f_t) and low noise requirement.

Table 7. Suitable JFET Candidates Specifications

COMPANY	PART NUMBER	V_P (V)	I_{dss} (mA)	gm (mS)	INPUT C (pF)	NOISE (1) (nV/RtHz)	BREAK DOWN (V)	CALCULATED f_t (MHz)
Interfet	IF140	–2.2	10	5.5	2.3	4	–20	380
Interfet	IF142	–2.2	10	5.5	2.3	4	–25	380
Interfet	2N5397/8	–2.5	13	8	5	2.5	–25	254
Interfet	2N5911/2	–2.5	13	8	5	2.5	—	254
Interfet	J308/9/10	–2.3	21	17	5.8	—	–25	466
Philips	BF513	–3	15	10	5	—	—	318
Fairchild	MMBF5486	–4	14	7	4	2.5	–25	278
Vishay Siliconix	SST441	–3.5	13	6	3.5	4	–35	272

(1) Noise data at approximately I_{dss}/2

The LNA noise could degrade the scope's SNR if it is comparable to the input referred noise of the LMH6518. LNA noise is influenced by the following operating conditions:

a. JFET equivalent input noise
b. BJT base current

Reducing either *a* or *b* above, or both, reduces noise. One way to reduce *a* is to increase R_8 (currently set to 0 Ω). This reduces the noise impact of J8 but requires a JFET which has a higher I_{dss} rating to maintain the operating current of J10 so that J10's noise contribution is minimized. Reducing the BJT base current is accomplished with increasing R_{20} at the expenses of higher rise/fall times. A higher β also reduces the base current (keep in mind that β and f_t at the operating collector current is what matters).

Figure 70 shows the impact of the JFET buffer noise on SNR, compared to SNR in Figure 60, assuming either 3 nV/√Hz or 1.5 nV/√Hz buffer noise for comparison.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Attenuator Design

Figure 69 shows a front-end attenuator designed to work with Figure 68.

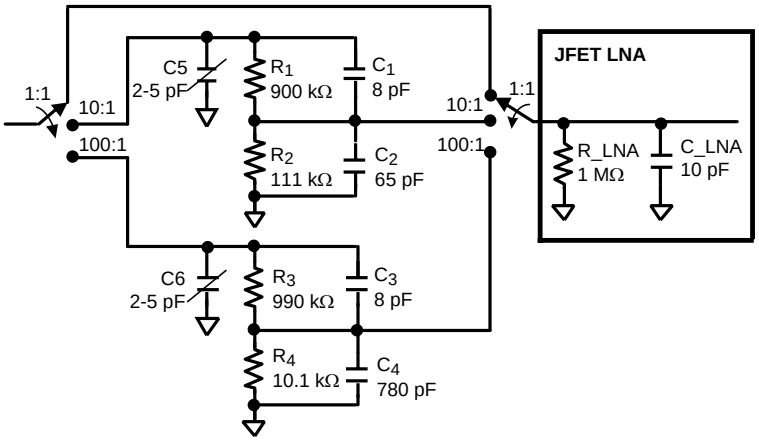


Figure 69. Front End Attenuator for JFET LNA Implementation

R_LNA and C_LNA are the input impedance components of the JFET LNA. The 10:1 and 100:1 attenuators bottom resistors (R_2 and R_4) are adjusted higher to compensate for the LNA's 1-MΩ input impedance, compared to the case where a high-input-impedance LNA is used. The two switches used on the input and output of the attenuator block are low-capacitance, high-isolation switches to reduce any speed or crosstalk impact. C_1 to C_4 provide the proper frequency response (and step response) by creating zeros that flatten the response for wide-band operation. For the 10:1 attenuator, $R_1C_1 = R_2C_2$. The same applies to the 100:1 attenuator. The shunt capacitors, C_1 to C_4, have a important other benefit in that they roll-off the resistor thermal noise at a low frequency (low pass response, −3 dB down at approximately 20 kHz) thereby eliminating any significant noise contribution from the attenuation resistors. Otherwise, the channel noise is dominated by the attenuator resistor thermal noise. C_2 and C_6 trimmer capacitors are adjusted to match the input capacitance regardless of attenuator used.

8.2.2.3 Application Curve

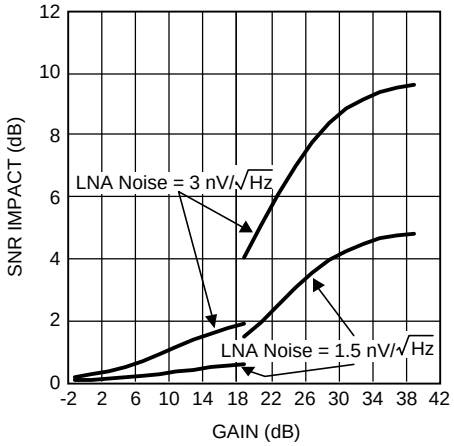


Figure 70. LNA Buffer SNR Impact

9 Power Supply Recommendations

The LMH6581 requires two power supplies. The analog signal path is powered by a single 5-V (±5%) supply and the digital control is powered by a single 3.3-V (±5%) supply. The 5-V supply must be capable of providing the 230 mA of quiescent current plus any load current. Ensure the loads of both amplifiers are included.

The 3.3-V digital supply requires only a small, 400-µA current.

Supply bypass capacitors must be placed at pins 3, 4, and 12. Low-ESR, ceramic capacitors of 0.01 µF are recommended.

10 Layout

10.1 Layout Guidelines

Layout is critical to achieve specified performance. Circuit symmetry is necessary for good HD2 performance. Input traces must have impedance-controlled transmission lines. To reduce output to input coupling, use ground plane to fill between the amplifier input and output traces. Output termination resistors are provided on chip internally to the LMH6518. When driving an ADC, the ADC must be placed physically close to the LMH6518 output pins. Use controlled impedance transmission lines if the ADC must not placed closer than 10 mm from the amplifier output pins.

10.2 Layout Example

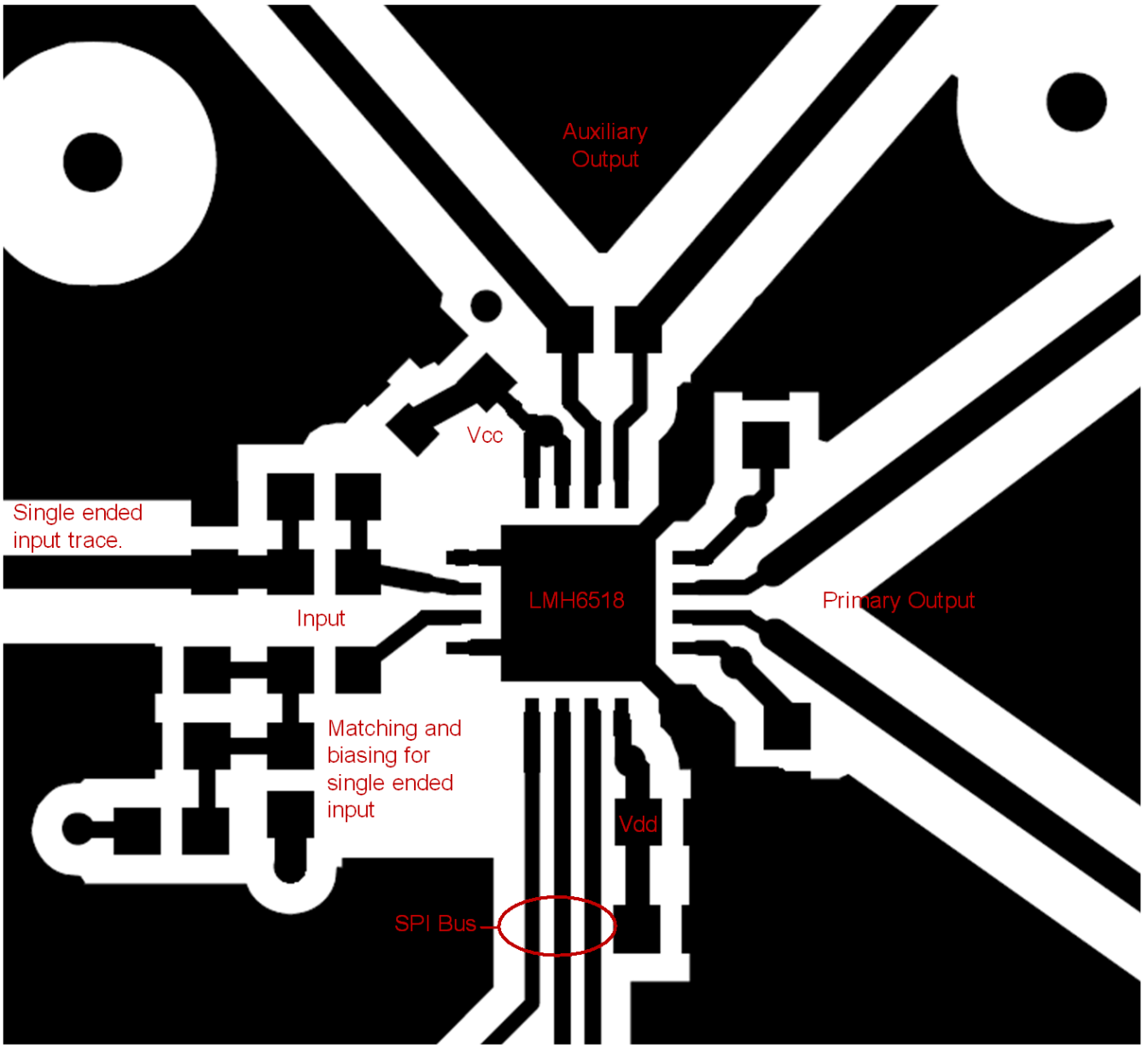


Figure 71. LMH6518 Layout Schematic

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.1.2 Device Nomenclature

Table 8. Definition of Terms and Specifications

TERM	DEFINITION
A_{V_CM} (dB)	Change in output offset voltage (ΔV_{OOS}) with respect to the change in input common mode voltage (ΔV_{I_CM})
A_{V_DIFF} (dB)	Gain with 100-Ω differential load
CM	Common mode
CMRR (dB)	Common mode rejection defined as: A_{V_DIFF} (dB) – A_{V_CM} (dB)
CMRR_CM	Common mode rejection relative to V_{CM} defined as: ΔV_{OOS} /ΔV_{CM}
HG	Preamp high gain
Ladder	Ladder attenuator setting (0-20 dB)
LG	Preamp low gain
Max Gain	Gain = 38.8 dB
Min Gain	Gain = −1.16 dB
+OUT	Positive main output
−OUT	Negative main output
+OUT AUX	Positive auxiliary output
−OUT AUX	Negative auxiliary output
PB	Phase balance defined as the phase difference between the complimentary outputs relative to 180°
PSRR	Input referred V_{OOS} shift divided by change in V_{CC}
PSRR_CM	Output common mode voltage change (ΔV_{O_CM}) with respect to V_{CC} voltage change (ΔV_{CC})
V_{CM}	Input pin voltage that sets main output CM
V_{CM_Aux}	Input pin voltage that sets auxiliary output CM
V_{I_CM}	Input CM voltage (average of +IN and −IN)
ΔV_{IN} (V)	Differential voltage across device inputs
V_{OOS}	DC offset voltage. Differential output voltage measured with inputs shorted together to $V_{CC}/2$
V_{O_CM}	Output common mode voltage (DC average of V_{+OUT} and $V_{–OUT}$)
V_{OS_CM}	CM offset voltage: $V_{O\_CM} – V_{CM}$
ΔV_{O_CM}	Variation in output common mode voltage (V_{O_CM})
$\frac{\Delta V_{O\_CM}}{\Delta V_{OUT}}$	Balance error. Measure of the output swing balance of +OUT and −OUT, as reflected on the output common mode voltage (V_{O_CM}), relative to the differential output swing (V_{OUT}). Calculated as output common mode voltage change (ΔV_{O_CM}) divided by the output differential voltage change (ΔV_{OUT}, which is nominally around 700 mV_{PP})
ΔV_{OUT}	Change in differential output voltage (Corrected for DC offset, V_{OOS})

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

Wideband Amplifiers by Peter Staric and Erik Margan, published by Springer (2006). (Section 5.2)

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH6518SQ/NOPB	ACTIVE	WQFN	RGH	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	Samples
LMH6518SQE/NOPB	ACTIVE	WQFN	RGH	16	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	Samples
LMH6518SQX/NOPB	ACTIVE	WQFN	RGH	16	4500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	L6518SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

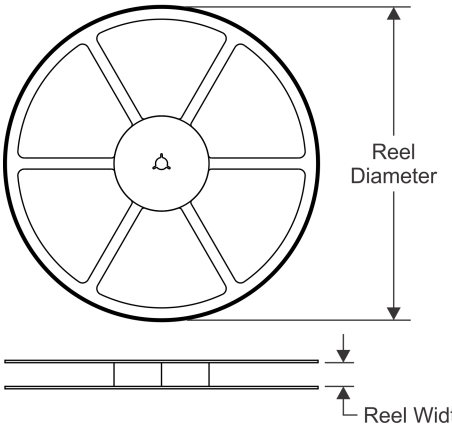
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

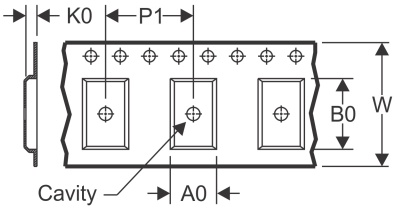
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

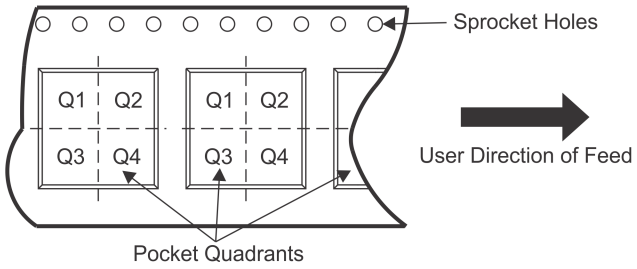


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

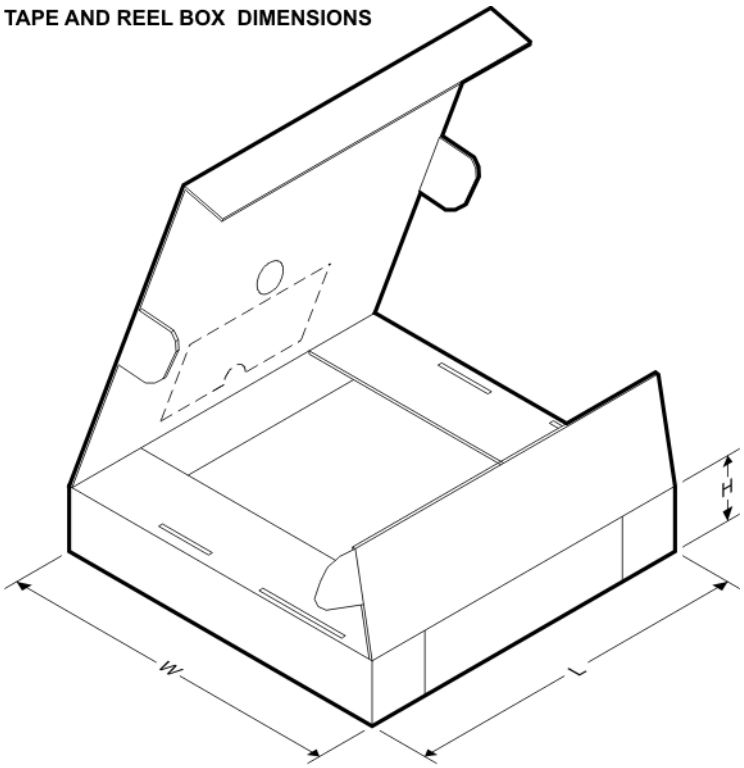
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH6518SQ/NOPB	WQFN	RGH	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQE/NOPB	WQFN	RGH	16	250	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LMH6518SQX/NOPB	WQFN	RGH	16	4500	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

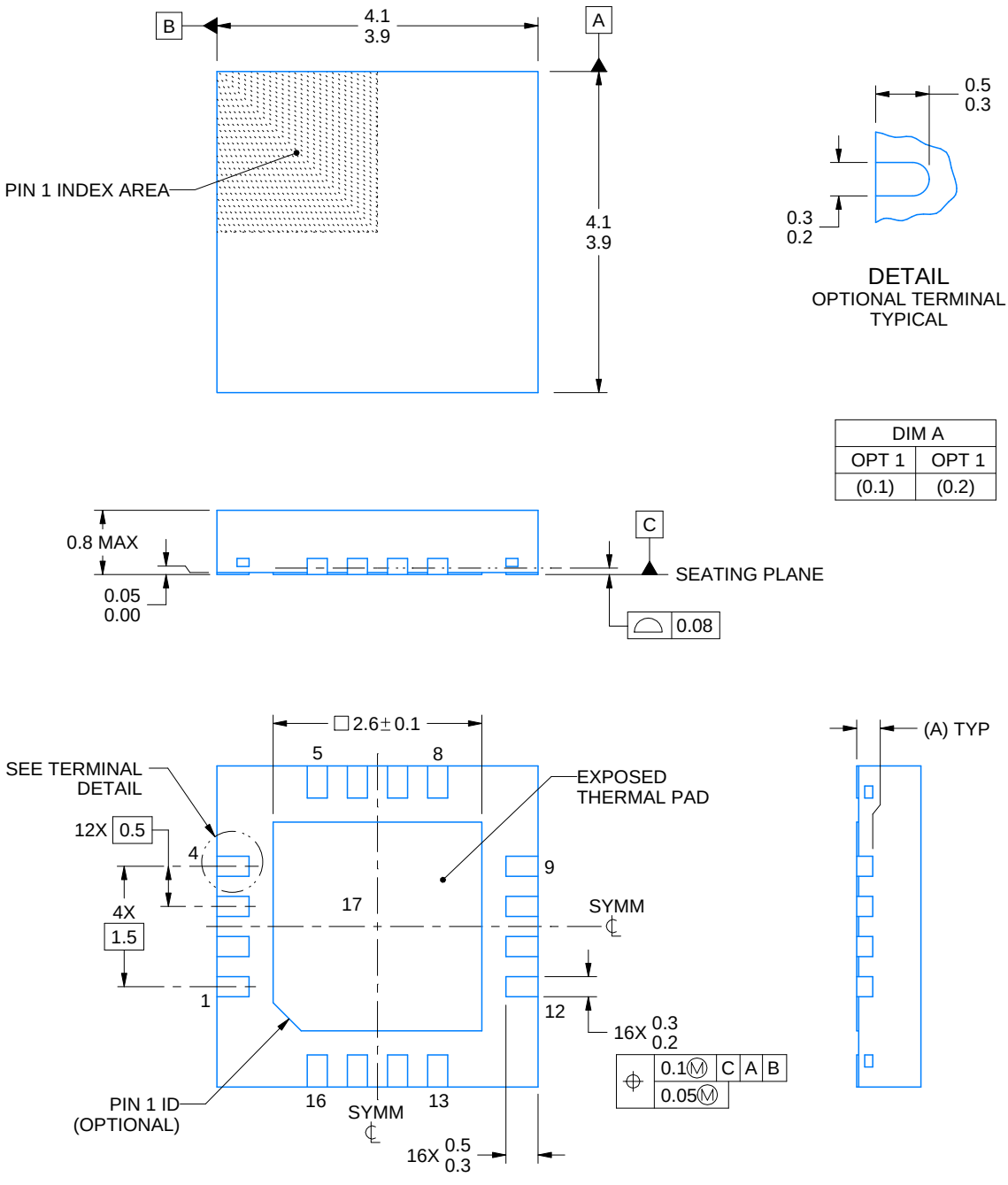
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH6518SQ/NOPB	WQFN	RGH	16	1000	208.0	191.0	35.0
LMH6518SQE/NOPB	WQFN	RGH	16	250	208.0	191.0	35.0
LMH6518SQX/NOPB	WQFN	RGH	16	4500	853.0	449.0	35.0

PACKAGE OUTLINE

RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

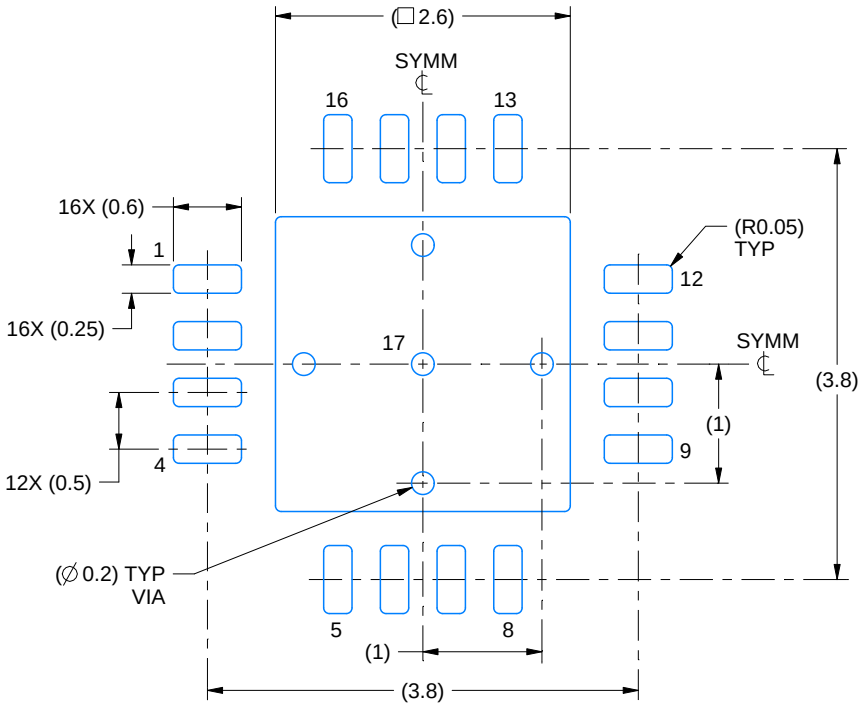
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

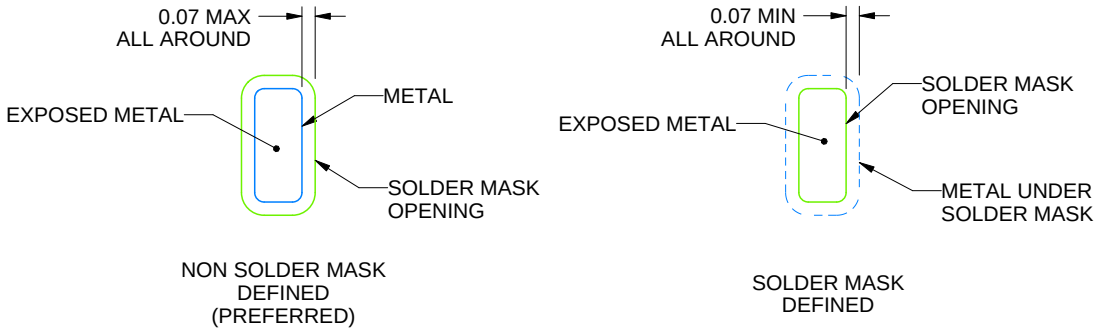
RGH0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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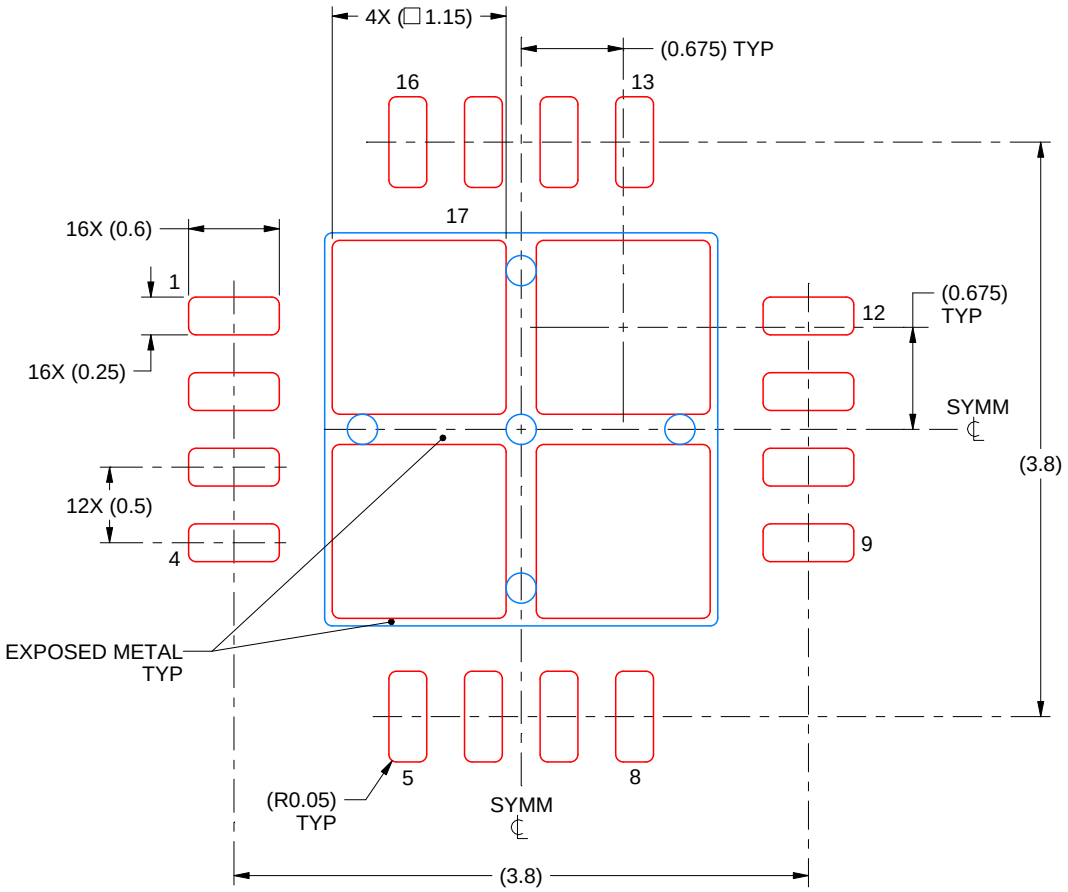
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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