RM25C256DS
256-Kbit 1.65V Minimum Non-volatile Serial EEPROM SPI Bus

Advance Datasheet

Features

- Memory array: 256Kbit non-volatile serial EEPROM memory
- Single supply voltage: 1.65V - 3.6V
  Serial peripheral interface (SPI) compatible
  -Supports SPI modes 0 and 3
- 1.6 MHz maximum clock rate for normal read
- 20 MHz maximum clock rate for fast read
- Flexible Programming
  - Byte/Page Program (1 to 64 Bytes)
  - Page size: 64 Bytes
- 128-byte, One-Time Programmable (OTP) Security Register
  - 64 bytes factory programmed with a unique identifier
  - 64 bytes user programmable
- Low Energy Byte Write
  -Byte Write consuming 50 nJ
- Low power consumption
  -0.20 mA active Read current (Typical)
  -0.7 mA active Write current (Typical)
  -0.5 µA ultra deep power-down current
- Auto Ultra-Deep Power-Down
  -Device can enter Ultra-Deep Power-Down automatically after finishing a Write operation
- Fast Write
  -Page Write in 1.5 ms (64 byte page)
  -Byte Write within 60 µs
- Industry's lowest read cycle latency
- Unlimited read cycles
- Hardware reset
- Page or chip erase capability
- 8-lead SOIC, TSSOP and UDFN packages
- RoHS-compliant and halogen-free packaging
- Data Retention: >40 years at 125°C
- Endurance: 100,000 write cycles (for both byte and page write cycles)
  - No degradation across temperature range
- No data loss under UV exposure on bare die or WLCSP
- Based on Adesto's proprietary CBRAM® technology

Description

The Adesto® RM25C256DS is a 256Kbit, serial EEPROM memory device that utilizes Adesto's CBRAM® resistive technology. The memory devices use a single low-voltage supply ranging from 1.65V to 3.6V.

The RM25C256DS is accessed through a 4-wire SPI interface consisting of a Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCK), and Chip Select ($\overline{CS}$). The maximum clock (SCK) frequency in normal read mode is 1.6MHz. In fast read mode the maximum clock frequency is 20MHz.

Adesto's EEPROM endurance can be as much as 40X higher than industry standard EEPROM devices operating in byte write mode at 85°C. Unlike EEPROMs based on floating gate technology (which require read-modify-write on a whole page for every write operation) CBRAM write endurance is based on the capability to write each byte individually, irrespective of whether the user writes single bytes or an entire page. Additionally, unlike floating gate technology, CBRAM does not experience any degradation of endurance across the full temperature range. By contrast, in order to modify a single byte, most EEPROMs modify and write full pages of 32, 64 or 128 bytes. This provides significantly less endurance for floating gate devices used in byte write mode when compared to page write mode.

The device supports direct write eliminating the need to pre-erase. Writing into the device can be done from 1 to 64 bytes at a time. All writing is internally self-timed. For compatibility with other devices, the device also features an Erase function which can be performed on 64-byte pages or on the whole chip.

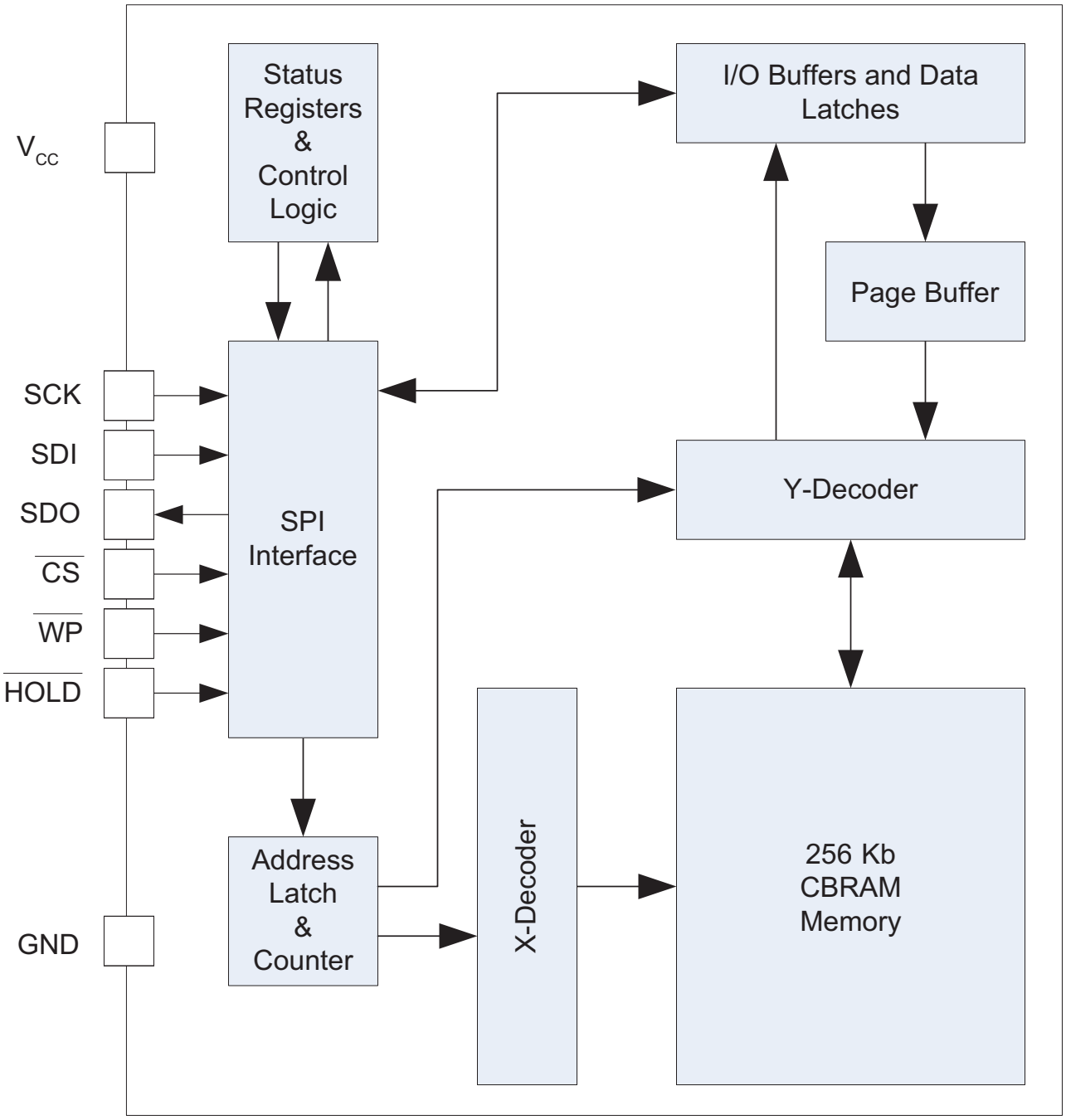
The device has both Byte Write and Page Write capability. Page Write is from 1 to 64 bytes. The Byte Write operation of CBRAM consumes only 10% of the energy consumed by a Byte Write operation of EEPROM devices of similar size.

The Page Write operation of CBRAM is 4-6 times faster than the Page Write operation of similar EEPROM devices.

Both random and sequential reads are available. Sequential reads are capable of reading the entire memory in one operation.

1. Block Diagram

Figure 1-1. Block Diagram



2. Absolute Maximum Ratings

Table 2-1. Absolute Maximum Ratings[1]

Parameter	Specification
Operating ambient temp range	-40°C to +85°C
Storage temperature range	-65°C to +150°C
Input supply voltage, VCC to GND	- 0.3V to 3.6V
Voltage on any pin with respect to GND	-0.5V to (V_{CC} + 0.5V)
ESD protection on all pins (Human Body Model)	>2kV
Junction temperature	125°C
DC output current	5mA

1. CAUTION: Stresses greater than Absolute Maximum Ratings may cause permanent damage to the devices. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in other sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may reduce device reliability.

3. Electrical Characteristics

3.1 DC Operating Characteristics

Applicable over recommended operating range: T_A = -40°C to +85° C, VCC = 1.65V to 3.6V

Symbol	Parameter	Condition	Min	Typ	Max	Units
		T_A = -40°C to +85° C, V_{CC} = 1.65V to 3.6V				
V_{CC}	Supply Range (1)		1.65		3.6	V
V_{Vccl}	V_{CC} Inhibit				1.55	V
I_{CC1}	Supply current, Fast Read	V_{CC}= 3.3V SCK at 10 MHz SDO = Open, Read		0.4	0.6	mA
I_{CC2}	Supply Current, Read Operation	V_{CC}= 3.3V SCK at 1.0 MHz SDO = Open, Read		0.18	0.2	mA
I_{CC3}	Supply Current, Program or Erase	V_{CC}= 3.3V, $\overline{CS}$ = V_{CC}		0.7	1.3	mA
I_{CC4}	Supply Current, Standby, LPSE=0	V_{CC}= 3.3V, $\overline{CS}$ = V_{CC}	@25°C	71	77	µA
			@85°C	89	97	
	Supply Current, Standby, LPSE=1		@25°C	34	39	
			@85°C	52	61	
	Supply Current, Standby, Auto Power Down enabled		@25°C	1.6	2.7	
			@85°C	9	12	
I_{CC5}	Supply Current, Power Down	V_{CC}= 3.3V Power Down	@25°C	1.6	2.8	µA
			@85°C	9	12	
I_{CC6}	Supply Current, Ultra Deep Power Down	V_{cc} = 3.3V, Ultra Deep Power Down	@25°C	0.04	0.15	µA
			@85°C	0.5	0.7	
I_{IL}	Input Leakage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ V_{IN}=0V to V_{CC}			1	µA
I_{OL}	Output Leakage	SDO , $\overline{CS}$ = V_{CC} V_{IN}=0V to V_{CC}			1	µA
V_{IL}	Input Low Voltage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$	-0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$	V_{CC} x 0.7		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100µA	V_{CC} - 0.2			V

1. A low ESR 100nF capacitor should be connected between each supply pin and GND.

3.2 AC Operating Characteristics

Applicable over recommended operating range: TA = -40°C to +85° C, VCC = 1.65V to3.6V. CL = 1 TTL Gate plus 10pF (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
f_{SCKF}	SCK Clock Frequency for Fast Read Mode	0		20	MHz
f_{SCK}	SCK Clock Frequency for Normal Read Mode	0		1.6	MHz
f_{APD}	SCK Clock Frequency for Auto Power-Down Mode	0		1.0	MHz
t_{RI}	SCK Input Rise Time			1	µs
t_{FL}	SCK Input Fall Time			1	µs
t_{SCKH}	SCK High Time	7.5			ns
t_{SCKL}	SCK Low Time	7.5			ns
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CL}	$\overline{CS}$ Low Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	10			ns
t_{CSH}	$\overline{CS}$ Hold Time	10			ns
t_{DS}	Data In Setup Time	4			ns
t_{DH}	Data In Hold Time	4			ns
t_{HS}	$\overline{HOLD}$ Setup Time	30			ns
t_{HD}	$\overline{HOLD}$ Hold Time	30			ns
t_{OV}	Output Valid			6.5	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{LZ}	$\overline{HOLD}$ to output Low Z	0		200	ns
t_{HZ}	$\overline{HOLD}$ to output High Z			200	ns
t_{DIS}	Output Disable Time			100	ns
t_{PW}	Page Write Cycle Time, 64 byte page (up to 30K write cycles)		1.5	2.5	ms
	Page Write Cycle Time, 64 byte page (up to 100K write cycles)		9		
t_{BP}	Byte Write Cycle Time		60	100	µs
t_{PUD}	V_{cc} Power-up Delay (1)			75	µs
t_{RPD}	Exit Power-Down Time	50			µs
t_{RESET}	Exit Ultra-Deep Power-Down Time	70			µs
t_{RDPD}	Chip Select High to Standby Mode			8	µs
C_{IN}	SCK, SDI, $\overline{CS}$, $\overline{HOLD}$, $\overline{WP}$ V_{IN}=0V			6	pF
C_{OUT}	SDO V_{IN}=0V			8	pF
Endurance		100,000 (2)			Write Cycles
Retention		40			Years

1. VCC must be within operating range.

2. Adesto memory products based on CBRAM technology are “Direct-Write” memories. Endurance cycle calculations follow JEDEC specification JESD22-A117B. Endurance data characterized at 2.5V, +85° C. Endurance specification is identical for both byte and page write (unlike current EEPROM technologies where byte write operations result in lower endurance).

3.3 AC Test Conditions

AC Waveform	Timing Measurement Reference Level	
V_{LO} = 0.2V		
V_{HI} = 3.4V	Input	0.5 V_{cc}
C_L = 30pF (for 1.6 MHz SCK)	Output	0.5 V_{cc}
C_L = 10pF (for 10 MHz SCK)		

4. Timing Diagrams

Figure 4-1. Synchronous Data Timing

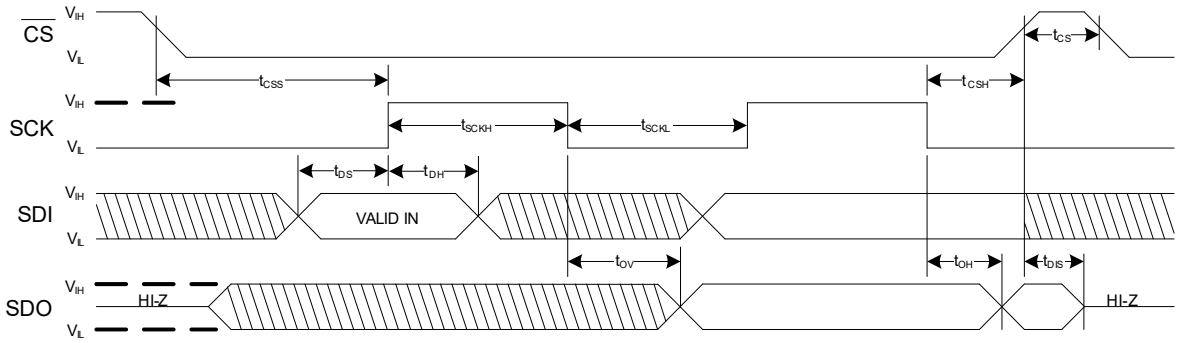


Figure 4-2. Hold Timing

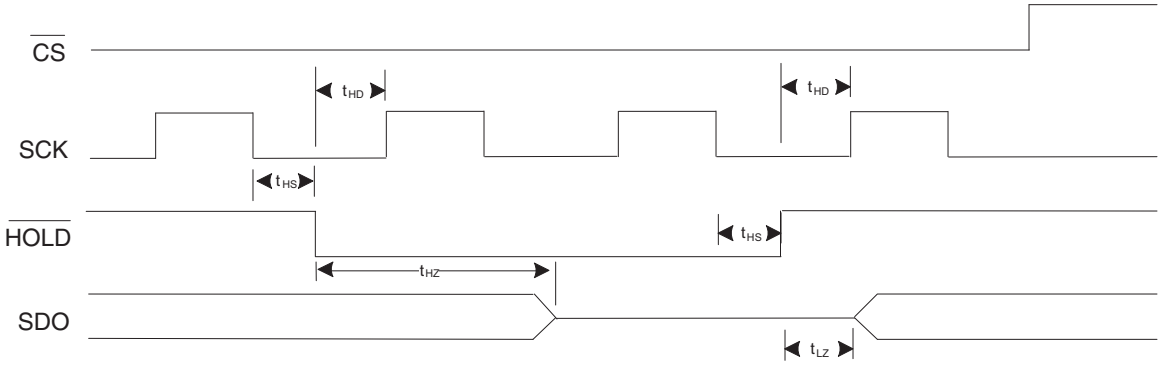
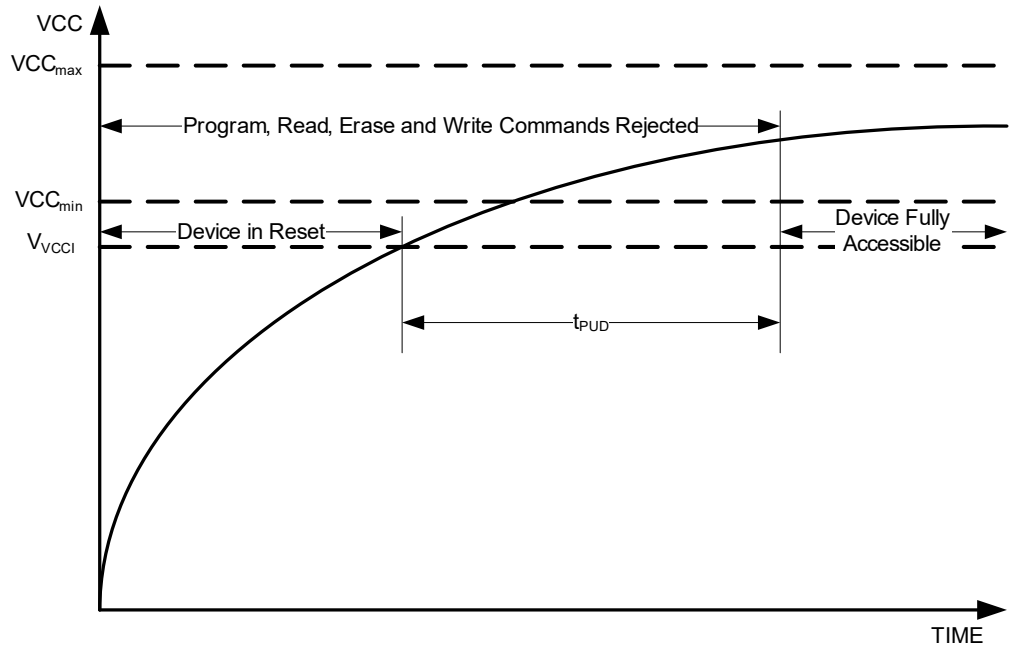


Figure 4-3. Power-up Timing



5. Pin Descriptions and Pin-out

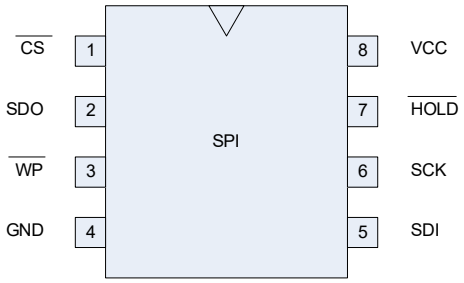
Table 5-1. Pin Descriptions

Mnemonic	Pin Number	Pin Name	Description
$\overline{CS}$	1	Chip Select	Making $\overline{CS}$ low activates the internal circuitry for device operation. Making $\overline{CS}$ high deselects the device and switches into standby mode to reduce power. When the device is not selected ($\overline{CS}$ high), data is not accepted via the Serial Data Input pin (SDI) and the Serial Data Output pin (SDO) remains in a high-impedance state. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
SDO	2	Serial Data Out	Sends read data or status on the falling edge of SCK. A pull-up resistor, connected only when the device is in Ultra-Deep Power-Down mode, ensures that the SDO line always has a valid logic value.
$\overline{WP}$	3	Write Protect	N/A
GND	4	Ground	
SDI	5	Serial Data In	Device data input; accepts commands, addresses, and data on the rising edge of SCK. To minimize power consumption, the master should ensure that this pin always has a valid logic level.

Mnemonic	Pin Number	Pin Name	Description
SCK	6	Serial Clock	Provides timing for the SPI interface. SPI commands, addresses, and data are latched on the rising edge on the Serial Clock signal, and output data is shifted out on the falling edge of the Serial Clock signal. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
$\overline{HOLD}$	7	Hold	When pulled low, serial communication with the master device is paused, without resetting the serial sequence.
V_{cc}	8	Power	Power supply pin.

Figure 5-1. Pin Out

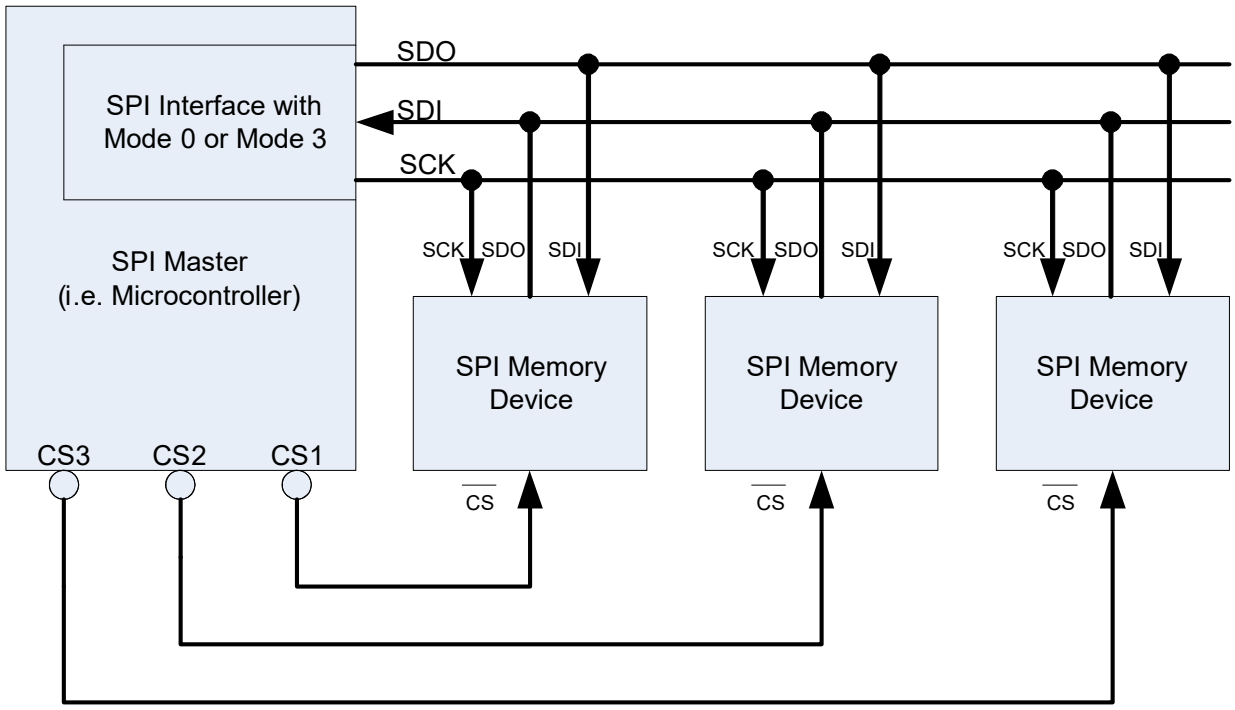
SOIC, UDFN and TSSOP



6. SPI Modes Description

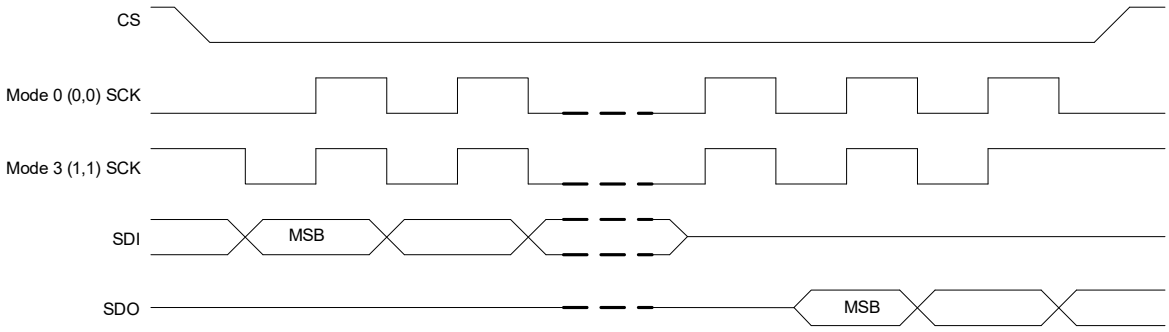
Multiple Adesto SPI devices can be connected onto a Serial Peripheral Interface (SPI) serial bus controlled by an SPI master, such as a microcontroller, as shown in Figure 6-1.

Figure 6-1. Connection Diagram, SPI Master and SPI Slaves



The Adesto RM25C256DS supports two SPI modes: Mode 0 (0, 0) and Mode 3 (1, 1). The difference between these two modes is the clock polarity when the SPI master is in standby mode ($\overline{CS}$ high). In Mode 0, the Serial Clock (SCK) stays at 0 during standby. In Mode 3, the SCK stays at 1 during standby. An example sequence for the two SPI modes is shown in Figure 6-2. For both modes, input data (on SDI) is latched in on the rising edge of Serial Clock (SCK), and output data (SDO) is available beginning with the falling edge of Serial Clock (SCK).

Figure 6-2. SPI Modes



7. Registers

7.1 Instruction Register

The Adesto RM25C256DS uses a single 8-bit instruction register. The instructions and their operation codes are listed in Table 7-1. All instructions, addresses, and data are transferred with the MSB first, and begin transferring with the first low-to-high SCK transition after the $\overline{CS}$ pin goes low.

Table 7-1. Device Operating Instructions

Instruction	Description	Operation Code	Address Cycles	Dummy Cycles	Data Cycles
WRSR	Write Status Register	01H	0	0	1
WR	Write 1 to 32 bytes	02H	2	0	1-32
READ	Read data from memory array	03H	2	0	1 to ∞
FREAD	Fast Read data from data memory	0BH	2	1	1 to ∞
WRDI	Write Disable	04H	0	0	0
RDSR	Read Status Register	05H	0	0	1 to ∞
WREN	Write Enable	06H	0	0	0
PERS	Page Erase 64 bytes	42H	2	0	0
CERS	Chip Erase	60H	0	0	0
		C7H	0	0	0
WRSR2	Write Status Register2	31H	0	0	1
PD	Power-Down	B9H	0	0	0
ROTPSR	Read the OTP Security Register	77H	0	0	1-64
UDPD	Ultra-Deep Power-Down	79H	0	0	0
POTPSR	Programming the OTP Security Register	9BH	0	0	3
RES	Resume from Power-Down	ABH	0	0	0

7.2 Status Register Byte 1

The Adesto RM25C256DS uses a 2-byte Status Register. The Write In Progress (WIP) and Write Enable (WEL) status of the device can be determined by reading the first byte of this register. The non-volatile configuration bits are also in the first byte. The Status Register can be read at any time, including during an internally self-timed write operation.

The Status Register Byte 1 format is shown in Table 7-2. The Status Register Byte 1 bit definitions are shown in Table 7-3.

Table 7-2. Status Register Byte 1 Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SRWD	APDE	LPSE	0	BP1	BP0	WEL	WIP

Table 7-3. Status Register Byte 1 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	WIP	**Write In Progress** “0” indicates the device is ready “1” indicates that the program/erase cycle is in progress and the device is busy	R	No
1	WEL	**Write Enable Latch** “0” Indicates that the device is disabled “1” indicates that the device is enabled	R/W	No
2	BP0	Block Protection Bits. "0" indicates the specific blocks are not protected. "1" indicates that the specific blocks are protected.	R/W	Yes
3	BP1			
4	UDPD	**Ultra-Deep Power-Down Status.** Read as “0” if device is in Standby or in an active read/write operation, Read as “1” if device is in Ultra-Deep Power-Down. Reading this bit after power-up or after exiting Ultra-Deep Power-Down will indicate when the device is ready for operation.	R	No
5	LPSE	**Low Power Standby Enable.** "0" indicates that the device will not use Low Power Standby Mode. "1" indicates that the device will use Low Power Standby Mode.	R/W	Yes
6	APDE	**Auto Power-Down Enable.** "0" indicates that the device will use Standby Mode. "1" indicates that the device will use Power-Down Mode instead of Standby Mode.	R/W	Yes
7	SRWD	**$\overline{\text{WP}}$ pin enable.** See Table 8-1.	R/W	Yes

7.3 Status Register Byte 2

The Adesto RM25C256DS uses the second byte in the Status Register to hold volatile configuration bits. The Status Register Byte 2 format is shown in table Table 7-4. The Status Register Byte 2 bit definitions are shown in table Table 7-5.

Table 7-4. Status Register Byte 2 Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	SLOWOSC	AUDPD

Table 7-5. Status Register Byte 2 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	AUDPD	**Auto Ultra-Deep Power-Down Mode after Write Operation** “1” specifies that the device will enter the Ultra-Deep Power-Down mode after a Write operation is completed. “0” specifies that the device will enter the Standby mode after a Write operation is completed.	R/W	No
1	SLOW OSC	**Slow Oscillator During Write Operation** "1" specifies that during the self-times Write operation the device will periodically slow down on-chip oscillator. "0" specifies that during the self-times Write operation the device will not slow down on-chip oscillator	R/W	No
2	N/A	Reserved. Read as “0”	N/A	No
3	N/A	Reserved. Read as “0”	N/A	No
4	N/A	Reserved. Read as “0”	N/A	No
5	N/A	Reserved. Read as “0”	N/A	No
6	N/A	Reserved. Read as “0”	N/A	No
7	N/A	Reserved. Read as “0”	N/A	No

8. Write Protection

The Adesto RM25C256DS has two protection modes: hardware write protection, via the $\overline{WP}$ pin associated with the SRWD bit in the Status Register, and software write protection in the form of the SRWD, WEL, BP0, and BP1 bits in the Status Register.

8.1 Hardware Write Protection

There are three hardware write protection features:

- All write instructions must have the appropriate number of clock cycles before $\overline{CS}$ goes high or the write instruction will be ignored.
- If the VCC is below the VCC Inhibit Voltage (V_{Vccl}, see DC Characteristics), all Read, Write, and Erase sequence instructions will be ignored.
- The $\overline{WP}$ pin provides write protection for the Status Register. When $\overline{WP}$ is low, the Status Register is write protected if the SRWD bit in the Status Register is High. When WP is high, the Status Register is writable independent of the SRWD bit. See Table 8-1.

Table 8-1. Hardware Write Protection on Status Register

SRWD	$\overline{WP}$	Status Register
0	Low	Writable
1	Low	Protected
0	High	Writable
1	High	Writable

8.2 Software Write Protection

There are two software write protection features:

- Before any program, erase, or write status register instruction, the Write Enable Latch (WEL) bit in the Status Register must be set to a one by execution of the Write Enable (WREN) instruction. If the WEL bit is not enabled, all program, erase, or write register instructions will be ignored.
- The Block Protection bits (BP0 and BP1) allow a part or the whole memory area to be write protected. See Table 8-2.

Table 8-2. Block Write Protect Bits

BP1	BP0	Protected Region	RM25C256DS	
			Protected Address	Protected Area Size
0	0	None	None	0
0	1	Top ¼	6000-7FFF	8K bytes
1	0	Top ½	4000-7FFF	16K bytes
1	1	All	0-7FFF	All

9. Reducing Energy Consumption

In normal operation, when the device is idle, ($\overline{CS}$ is high, no Write or Erase operation in progress), the device is in Standby Mode, waiting for the next command. To reduce device energy consumption, the Power-Down or Ultra-Deep Power-Down modes may be used.

To minimize power consumption, the master should ensure that the SCK, SDI and CS pins always has a valid logic level, these pins should not be left floating when the device is in Standby, Power-Down or Ultra-Deep Power-Down modes.

9.1 Power-Down Mode

Power-Down mode allows the user to reduce the power of the device to its lowest power consumption state. The PD command is used to instruct the device to enter Power-Down mode.

All instructions given during the Power-Down mode are ignored except the Resume From Power-Down (RES) instruction. Therefore this mode can be used as an additional software write protection feature.

9.2 Ultra-Deep Power-Down Mode

The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby and Power-Down modes by shutting down additional internal circuitry. The UDPD command is used to instruct the device to enter Ultra-Deep Power-Down mode.

When the device is in the Ultra-Deep Power-Down mode, all commands including the Read Status Register and Resume From Power-Down commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

To test if the device is in Ultra-Deep Power-Down mode without risk of bringing it out of Ultra-Deep Power-Down mode, use the Read Status Register Byte 1 instruction. The UDPD bit in Status Register Byte 1 will be 1 (pulled high by the internal pull-up resistor) if the device is in Ultra-Deep Power-Down mode, 0 otherwise.

Only the Exit Ultra-Deep Power-Down signal sequences described in Section 10.15 will bring the device out of the Ultra-Deep Power-Down mode.

9.3 Auto Ultra-Deep Power-Down Mode after Write Operation

The Auto Ultra-Deep Power-Down Mode after Write Operation allows the device to further reduce its energy consumption by automatically entering the Ultra-Deep Power-Down Mode after completing an internally timed Write operation. The operation can be any one of the commands WR (Write), or WRSR (Write Status Register). Note that the WRSR2 command does not cause the device to go into Ultra-Deep Power-Down Mode.

Only the Exit Ultra-Deep Power-Down signal sequences described in Section 10.15 will bring the device out of the Ultra-Deep Power-Down Mode.

9.4 Auto Power-Down Enable

For frequencies lower than f_{APD} (see AC Operating Characteristics), the APDE bit in the Status Register may be enabled. The device will then automatically enter Power-Down mode instead of Standby mode when idle. ($\overline{CS}$ is high, no Write or Erase operation in progress).

In this mode, the device will behave normally to all commands, and will leave Power-Down mode once $\overline{CS}$ is pulled down.

If Auto Power-Down is enabled, and the SCK Clock Frequency is increased to a speed higher than f_{APD}, the device may not react as expected to the command. Before changing SCK frequency, the APDE bit in the Status Register must be disabled.

Note that the PD or UDPD commands may still be used as additional software write protection features when Auto Power-Down is enabled. Note that if the PD command is issued while Auto Power-Down is enabled, the device will enter Power-Down mode, and all instructions given will be ignored except the Resume From Power-Down (RES) instruction. The device will not wake up immediately after $\overline{CS}$ is pulled down.

9.5 Low Power Standby Enable

For frequencies lower than f_{APD} (see AC Operating Characteristics), the LPSE bit in the Status Register may be enabled. The device will then automatically enter Low Power Standby mode when idle. ($\overline{CS}$ is high, no Write or Erase operation in progress).

In this mode, the device will behave normally to all commands, and will leave Low Power Standby mode once $\overline{CS}$ is pulled down.

If Low Power Standby Mode is enabled, and the SCK Clock Frequency is increased to a speed higher than f_{APD}, the device may not react as expected to the command. Before changing SCK frequency, the LPSE bit in the Status Register must be disabled.

Note that the PD or UDPD commands may still be used as additional software write protection features when Low Power Standby Mode is enabled. Note that if the PD command is issued while Low Power Standby Mode is enabled, the device will enter Power-Down mode, and all instructions given will be ignored except the Resume From Power-Down (RES) instruction. The device will not wake up immediately after $\overline{CS}$ is pulled down.

9.6 Slow Oscillator During Write Operation

The Slow Oscillator During Write Operation mode allows the device to further reduce its average current consumption by periodically slowing down the internal oscillator. This creates a duty cycle effect with time periods of high activity followed by timer periods of low activity. While this operating mode will increase the effective Write time, the average current over this Write time will be lower compared to the mode without this feature.

9.7 Exit Ultra-Deep Power-Down mode

Only the Exit Ultra-Deep Power-Down signal sequences described in Section 10.15 will bring the device out of the Ultra-Deep Power-Down mode.

10. Command Descriptions

10.1 WREN (Write Enable, 06h):

The device powers up with the Write Enable Latch set to zero. This means that no write or erase instructions can be executed until the Write Enable Latch is set using the Write Enable (WREN) instruction. The Write Enable Latch is also set to zero automatically after any non-read instruction. Therefore, all page programming instructions and erase instructions must be preceded by a Write Enable (WREN) instruction. The sequence for the Write Enable instruction is shown in Figure 10-1.

Figure 10-1. WREN Sequence (06h)

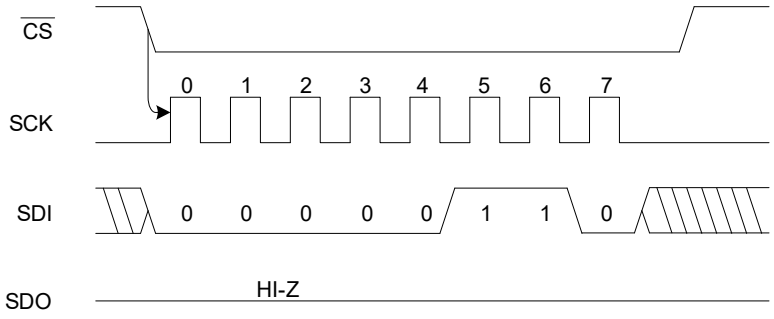


Table 10-1 is a list of actions that will automatically set the Write Enable Latch to zero when successfully executed. If an instruction is not successfully executed, for example if the CS pin is brought high before an integer multiple of 8 bits is clocked, the Write Enable Latch will not be reset.

Table 10-1. Write Enable Latch to Zero

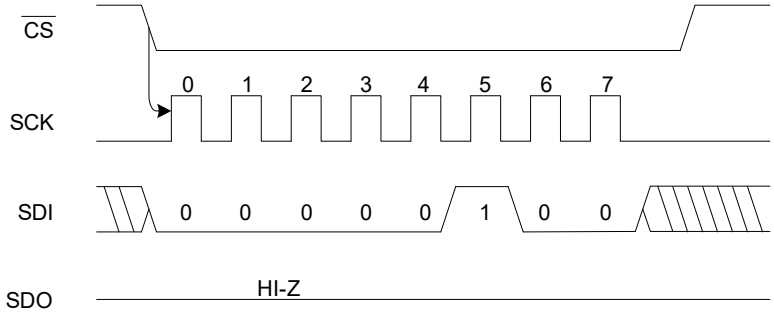
Instruction/Operation
Power-Up
WRDI (Write Disable)
WR (Write)
WRSR (Write Status Register)
WRSR2 (Write Status Register2)

Instruction/Operation
PERS (Page Erase)
CERS (Chip Erase)
PD (Power-Down)

10.2 WRDI (Write Disable, 04h):

To protect the device against inadvertent writes, the Write Disable instruction disables all write modes. Since the Write Enable Latch is automatically reset after each successful write instruction, it is not necessary to issue a WRDI instruction following a write instruction. The WRDI instruction is independent of the status of the WP pin. The WRDI sequence is shown in Figure 10-2.

Figure 10-2. WRDI Sequence (04h)

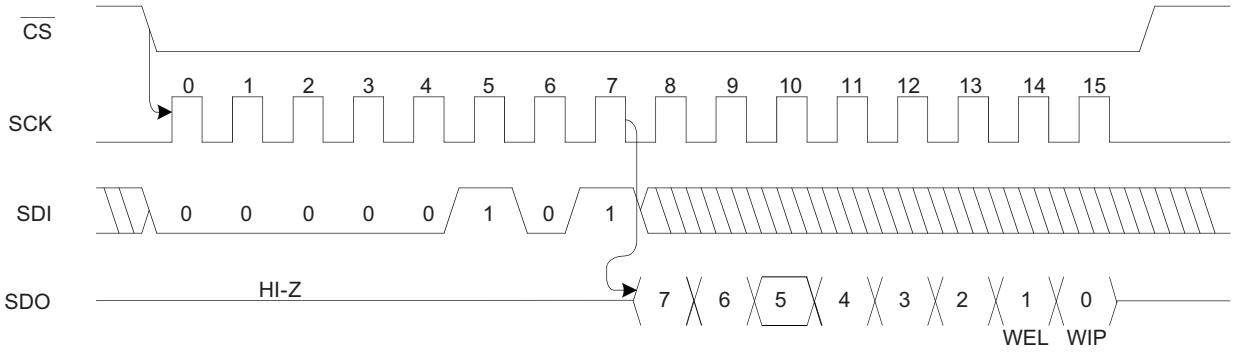


10.3 RDSR (Read Status Register Byte 1, 05h):

The Read Status Register Byte 1 instruction provides access to the Status Register and indication of write protection status of the memory.

Caution: The Write In Progress (WIP) and Write Enable Latch (WEL) indicate the status of the device. The RDSR sequence is shown in Figure 10-3.

Figure 10-3. RDSR Sequence (05h)

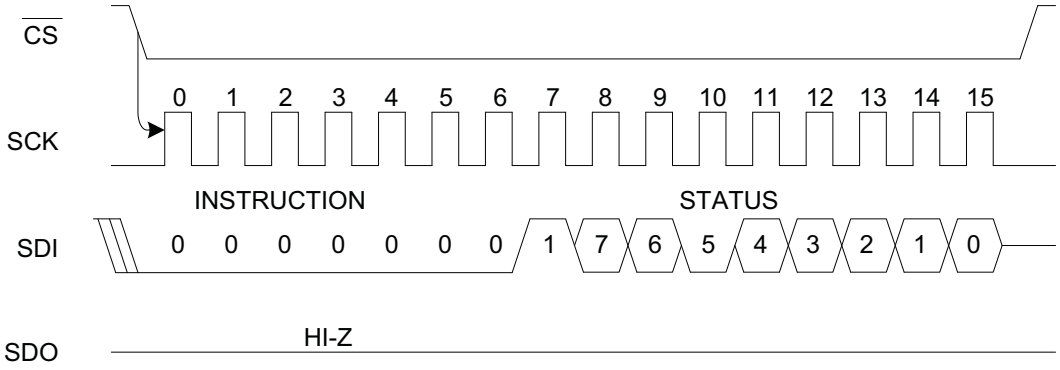


10.4 WRSR (Write Status Register Byte 1, 01h):

The Write Status Register (WRSR) instruction allows the user to select one of three levels of protection. The memory array can be block protected (see Table 8-2) or have no protection at all. The SRWD bit (in conjunction with the $\overline{WP}$ pin) sets the write status of the Status Register (see Table 8-1).

Only the BP0, BP1, APDE, LPSE and SRWD bits are writable and are nonvolatile cells. When the $\overline{WP}$ pin is low, and the SRWD bit in the Status Register is a one, a zero cannot be written to SRWD to allow the part to be writable. To set the SRWD bit to zero, the $\overline{WP}$ pin must be high. The WRSR sequence is shown in Figure 10-4.

Figure 10-4. WRSR Sequence (01h)



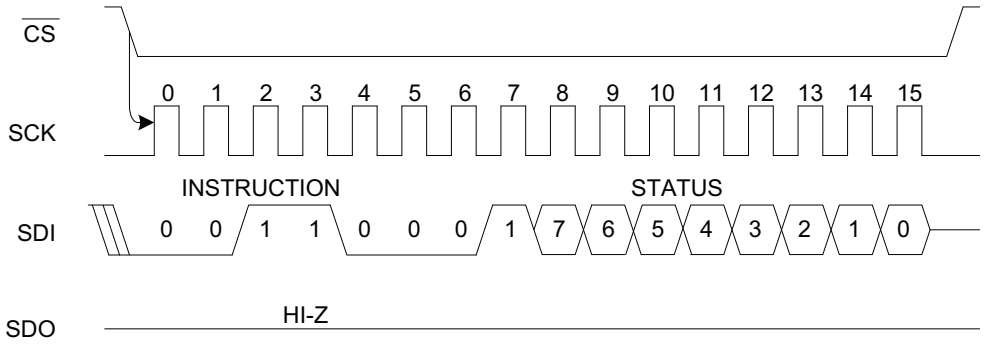
10.5 WRSR2 (Write Status Register Byte 2, 31h):

The Write Status Register Byte 2 (WRSR2) instruction allows the user to set or clear the SLOWOSC or AUDPD bits.

The user must set the WEL bit before issuing this command. Once the device accepts the WRSR2 command the WIP bit will be set to indicate that the device is busy. Once the device completes the operation, the WEL and WIP bits will be automatically cleared.

The WRSR sequence is shown in Figure 10-5.

Figure 10-5. WRSR2 Sequence (31h)



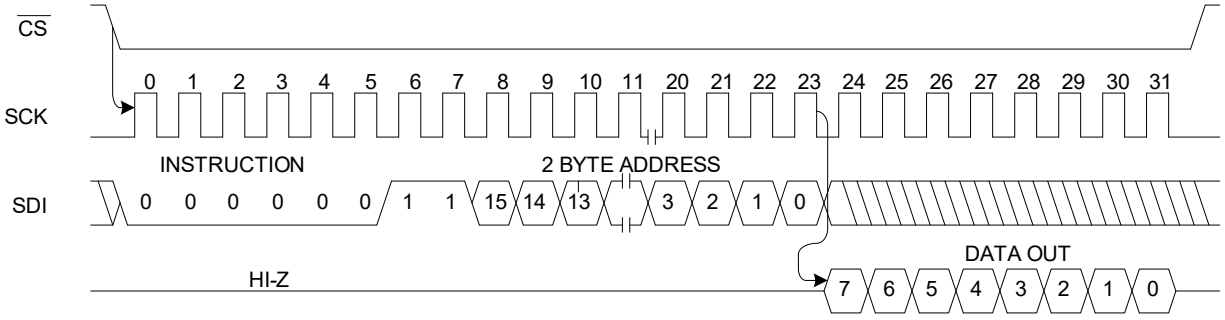
10.6 READ (Read Data, 03h):

Reading the Adesto RM25C256DS via the Serial Data Output (SDO) pin requires the following sequence: First the $\overline{CS}$ line is pulled low to select the device; then the READ op-code is transmitted via the SDI line, followed by the address to be read (A15-A0). Although not all 16 address bits are used, a full 2 bytes of address must be transmitted to the device. For the 256Kb device, only address A0 to A14 are used; the rest are don't cares and must be set to “0”.

Once the read instruction and address have been sent, any further data on the SDI line will be ignored. The data (D7-D0) at the specified address is then shifted out onto the SDO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the byte of data comes out. This completes the reading of one byte of data.

The READ sequence can be automatically continued by keeping the $\overline{CS}$ low. At the end of the first data byte the byte address is internally incremented and the next higher address data byte will be shifted out. When the highest address is reached, the address counter will roll over to the lowest address (00000), thus allowing the entire memory to be read in one continuous read cycle. The READ sequence is shown in Figure 10-6.

Figure 10-6. Single Byte READ Sequence (03h)



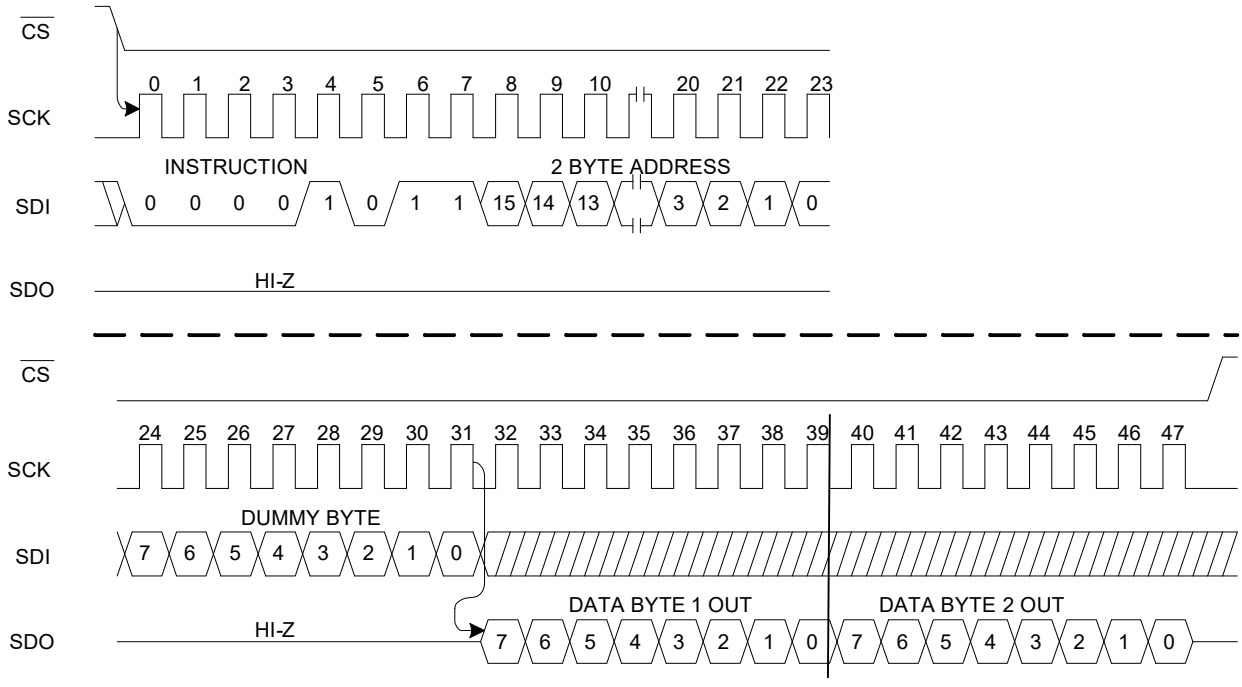
10.7 FREAD (Fast Read Data, 0Bh):

The Adesto RM25C256DS also includes the Fast Read Data command, which facilitates reading memory data at higher clock rates, up to 10 MHz. After the $\overline{CS}$ line is pulled low to select the device, the FREAD op-code is transmitted via the SDI line. This is followed by the 2-byte address to be read (A15-A0) and then a 1-byte dummy. For the 256-Kbit device, only address A0 to A14 are used; the rest are don't cares and must be set to "0".

The next 8 bits transmitted on the SDI are dummy bits. The data (D7-D0) at the specified address is then shifted out onto the SDO line. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the data comes out. This completes the reading of one byte of data.

The FREAD sequence can be automatically continued by keeping the $\overline{CS}$ low. At the end of the first data byte, the byte address is internally incremented and the next higher address data byte is then shifted out. When the highest address is reached, the address counter rolls over to the lowest address (00000), allowing the entire memory to be read in one continuous read cycle. The FREAD sequence is shown in Figure 10-7.

Figure 10-7. Two Byte FREAD Sequence (0Bh)

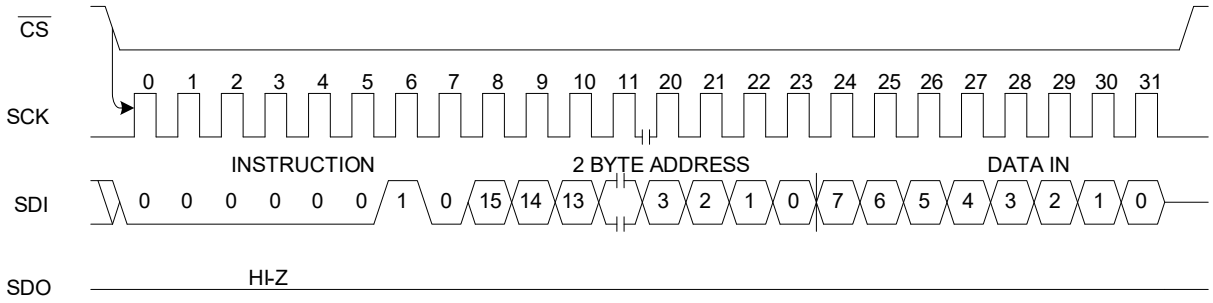


10.8 WRITE (Write Data, 02h):

Product	Density	Page Size (bytes)
RM25C256CDS	256 Kbit	64

The Write (WR) instruction allows bytes to be written to the memory. But first, the device must be write-enabled via the WREN instruction. The $\overline{CS}$ pin must be brought high after completion of the WREN instruction; then the $\overline{CS}$ pin can be brought back low to start the WR instruction. The $\overline{CS}$ pin going high at the end of the WR input sequence initiates the internal write cycle. During the internal write cycle, all commands except the RDSR instruction are ignored.
A WR instruction requires the following sequence: After the $\overline{CS}$ line is pulled low to select the device, the WR op-code is transmitted via the SDI line, followed by the byte address (A15-A0) and the data (D7-D0) to be written. For the 256Kb device, only address A0 to A14 are used; the rest are don't cares and must be set to “0”. The internal write cycle sequence will start after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.
The Write In Progress status of the device can be determined by initiating a Read Status Register (RDSR) instruction and monitoring the WIP bit. If the WIP bit (Bit 0) is a “1”, the write cycle is still in progress. If the WIP bit is “0”, the write cycle has ended. Only the RDSR instruction is enabled during the write cycle. The sequence of a one-byte WR is shown in Figure 10-8.

Figure 10-8. One Byte Write Sequence (0Bh)



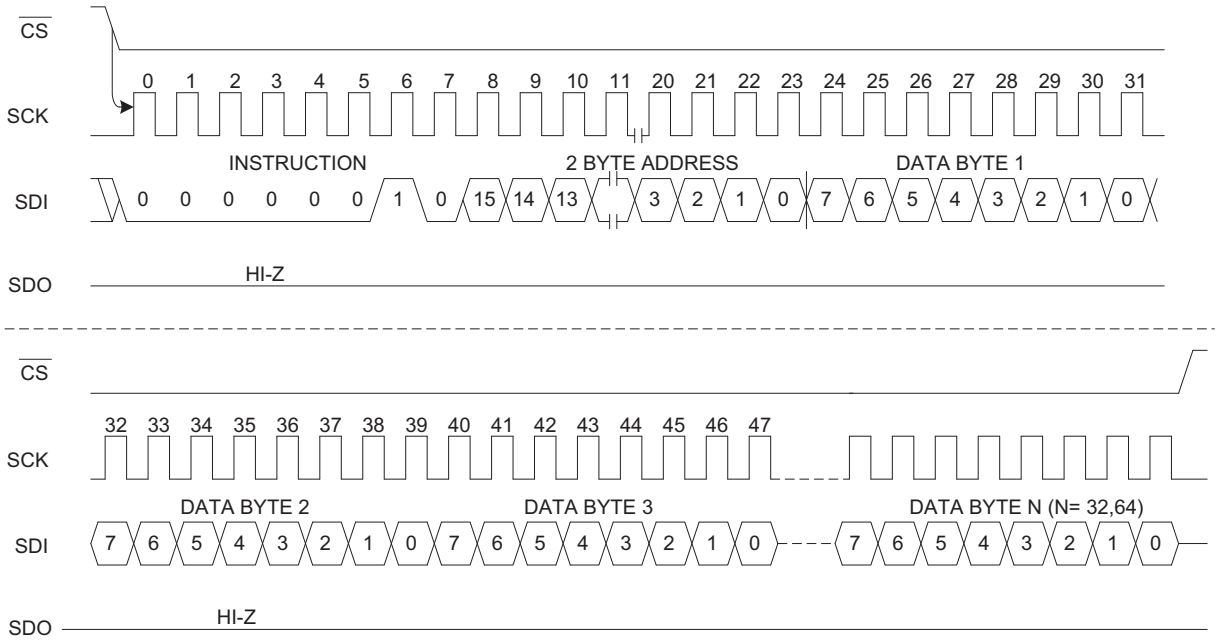
The Adesto RM25C256DS is capable of a 64-byte write operation.

For the RM25C256DS: After each byte of data is received, the six low-order address bits (A5-A0) are internally incremented by one; the high-order bits of the address will remain constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 6 least significant bits [A5-A0] are all zero). If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are ensured to be written correctly within the same page. If less than 64 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

The Adesto RM25C256DS is automatically returned to the write disable state at the completion of a program cycle. The sequence for a 64 byte WR is shown in Figure 10-9. Note that the Multi-Byte Write operation is internally executed by sequentially writing the words in the Page Buffer.

NOTE: If the device is not write enabled (WREN) previous to the Write instruction, the device will ignore the write instruction and return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re initiate the serial communication.

Figure 10-9. WRITE Sequence (02h)



10.9 OTP Security Register

The RM25C256DS device contains a specialized One-Time Programmable Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as an One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed. The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Adesto and will contain a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 10-2. Security Register

	Security Register Byte Number							
	0	1	· · ·	63	64	65	· · ·	127
Data Type	One-Time User Programmable				Factory Programmed by Adesto			

10.9.1 Programming the OTP Security Register (9Bh, 00h, 00h)

The user programmable portion of the Security Register does not need to be erased before it is programmed.

To program the Security Register, a 3-byte opcode sequence of 9Bh, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Security Register should take place in a time of t_P, during which time the RDY/$\overline{BUSY}$ bit in the Status Register will indicate that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

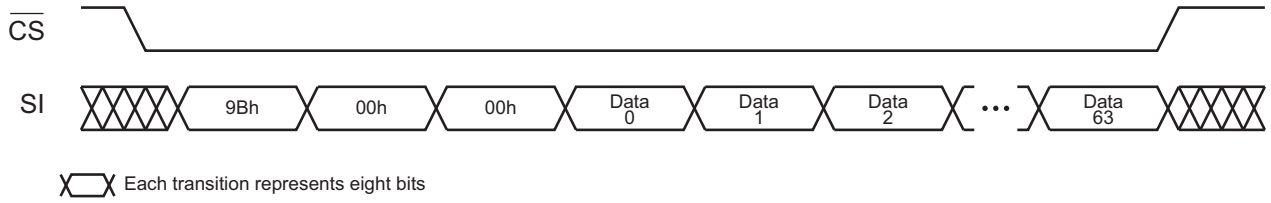
If the full 64 bytes of data are not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data will wrap back around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte will be stored at byte location 0 of the Security Register.

Warning: **The user programmable portion of the Security Register can only be programmed one time.** Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command utilizes the internal buffer for processing. Therefore, the contents of the Buffer will be altered from its previous state when this command is issued.

Figure 10-10.Program Security Register

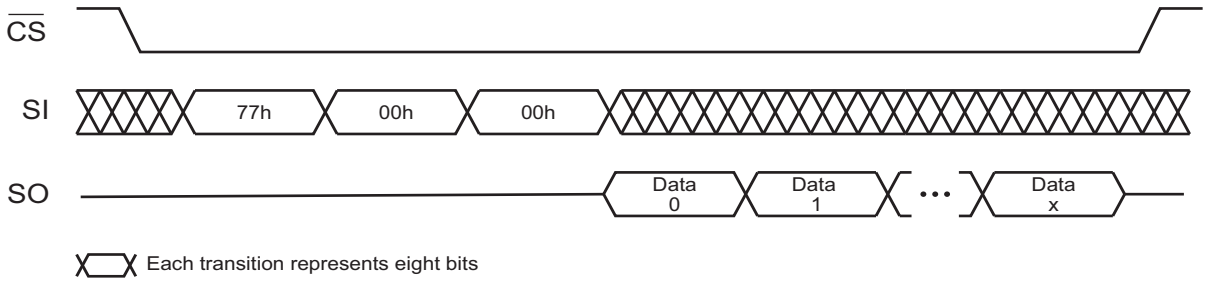


10.9.2 Reading the OTP Security Register (77h)

To read the Security Register, an opcode of 77h and two bytes of 00h must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin will result in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin will terminate the Read Security Register operation and put the SO pin into a high-impedance state.

Figure 10-11.Read Security Register



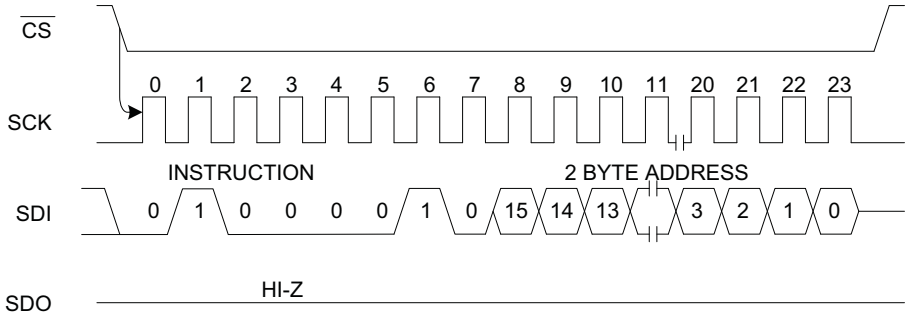
10.10 PERS (Page Erase 64 bytes, 42h):

Page Erase sets all bits inside the addressed 64-byte page to a 1. A Write Enable (WREN) instruction is required prior to a Page Erase. After the WREN instruction is shifted in, the $\overline{CS}$ pin must be brought high to set the Write Enable Latch.

The Page Erase sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code, then 2 address bytes. Any address inside the page to be erased is valid. This means the bottom six bits (A5-A0) of the address are ignored. Once the address is shifted in, the $\overline{CS}$ pin is brought high, which initiates the self-timed Page Erase function. The WIP bit in the Status Register can be read, using the RDSR instruction, to determine when the Page Erase cycle is complete.

The sequence for the PERS is shown in Figure 10-12.

Figure 10-12.PERS Sequence (42h)



10.11 CERS (Chip Erase):

Chip Erase sets all bits inside the device to a 1. A Write Enable (WREN) instruction is required prior to a Chip Erase. After the WREN instruction is shifted in, the $\overline{CS}$ pin must be brought high to set the Write Enable Latch.

The Chip Erase sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code. There are two different instruction codes for CER, 60h and C7h. Either instruction code will initiate the Chip Erase sequence. No address bytes are needed. Once the instruction code is shifted in, the $\overline{CS}$ pin is brought high, which initiates the self-timed Chip Erase function. The WIP bit in the Status Register can be read, using the RDSR instruction, to determine when the Chip Erase cycle is complete.

The sequence for the 60h CER instruction is shown in Figure 10-13. The sequence for the C7h CER instruction is shown in Figure 10-14.

Figure 10-13.CERS Sequence (60h)

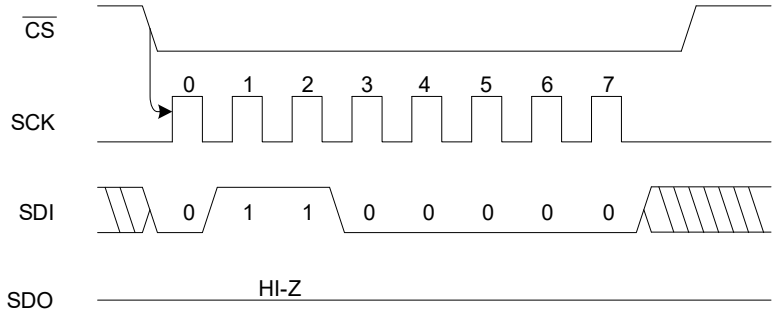
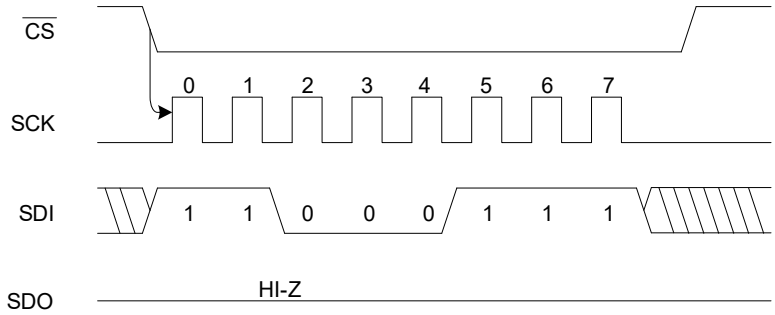


Figure 10-14.CERS Sequence (C7h)



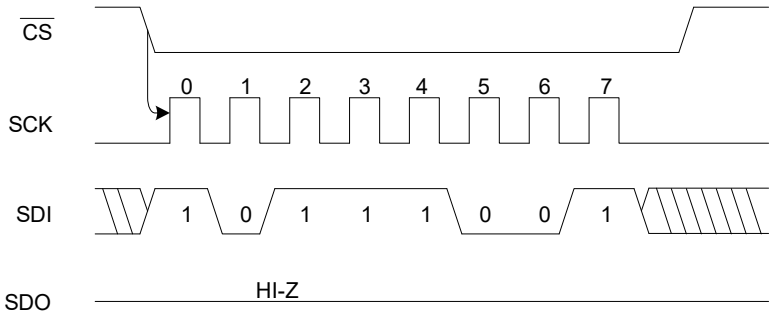
10.12 PD (Power-Down, B9h):

Power-Down mode allows the user to reduce the power of the device to its lowest power consumption state.

All instructions given during the Power-Down mode are ignored except the Resume from Power-Down (RES) instruction. Therefore this mode can be used as an additional software write protection feature.

The Power-Down sequence is initiated by bringing the $\overline{CS}$ pin low; this is followed by the instruction code. Once the instruction code is shifted in the $\overline{CS}$ pin is brought high, which initiates the PD mode. The sequence for PD is shown in Figure 10-15.

Figure 10-15.PD Sequence (B9h)



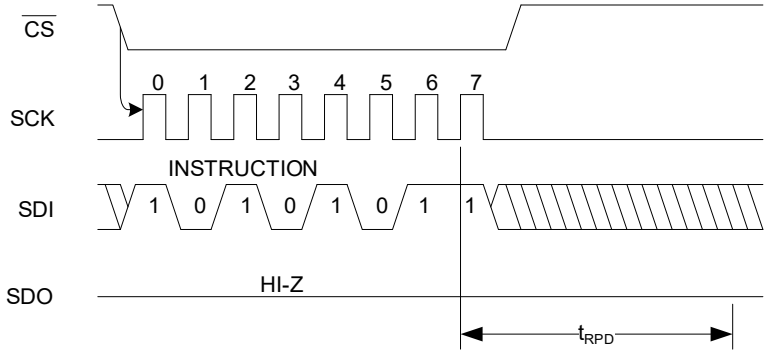
10.13 RES (Resume from Power-Down, ABh):

The Resume from Power-Down mode is the only command that will wake the device up from the Power-Down mode. All other commands are ignored.

In the simple instruction command, after the $\overline{CS}$ pin is brought low, the RES instruction is shifted in. At the end of the instruction, the $\overline{CS}$ pin is brought back high.

The rising edge of the SCK clock number 7 (8^{th} rising edge) initiates the internal RES instruction. The device becomes available for Read and Write instructions 75µS after the 8^{th} rising edge of the SCK (t_{PUD}, see AC Characteristics). The sequence for simple RES instruction is shown in Figure 10-16.

Figure 10-16.Simple RES Sequence (ABh)



10.14 UDPD (Ultra-Deep Power-Down, 79h)

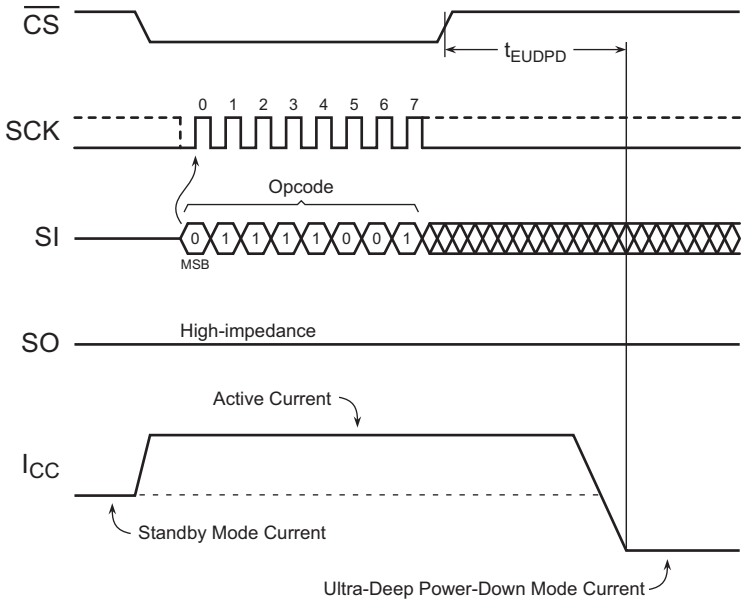
The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby and Power-Down modes by shutting down additional internal circuitry. When the device is in the Ultra-Deep Power-Down mode, all commands including the Read Status Register and Resume from Deep Power-Down commands will be ignored. Since all commands will be ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

10.14.1 UDPD mode

Entering the Ultra-Deep Power-Down mode is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode will be ignored. When the $\overline{CS}$ pin is deasserted, the device will enter the Ultra-Deep Power-Down mode within the maximum time of t_{EUDPD}.

The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device will abort the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted. In addition, the device will default to the standby mode after a power cycle. The Ultra-Deep Power-Down command will be ignored if an internally self-timed operation such as a program or erase cycle is in progress. The sequence for UDPD is shown in Figure 10-17.

Figure 10-17.Ultra-Deep Power-Down (79h)



10.15 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode, one of the following operations can be performed:

10.15.1 Exit Ultra-Deep Power-Down / Hardware Reset

Issue the Exit Ultra-Deep Power-Down / Hardware Reset sequence as described in Section 10.16, Hardware Reset.

10.15.2 Power Cycling

The device can also exit the Ultra-Deep Power Mode by power cycling the device. The system must wait for the device to return to the standby mode before normal command operations can be resumed. Upon recovery from Ultra-Deep Power-Down all internal registers will be at their Power-On default state.

10.16 Hardware Reset

The Exit Ultra-Deep Power-Down / Hardware Reset command sequence can be used to wakeup the device from Ultra-Deep Power-Down. This sequence can also be used to reset the device to its power on state without cycling power. It is in any case recommended to run a Hardware Reset command sequence after every time the device is powered up.

The reset sequence does not use the SCK pin. The SCK pin has to be held low (mode 0) or high (mode 3) through the entire reset sequence.This prevents any confusion with a command, as no command bits are transferred (clocked).

A reset is commanded when the data on the SDI pin is 0101 on four consecutive positive edges of the $\overline{CS}$ pin with no edge on the SCK pin throughout. This is a sequence where

1) $\overline{CS}$ is driven active low to select the device. This powers up the SPI slave.

2) Clock (SCK) remains stable in either a high or low state.

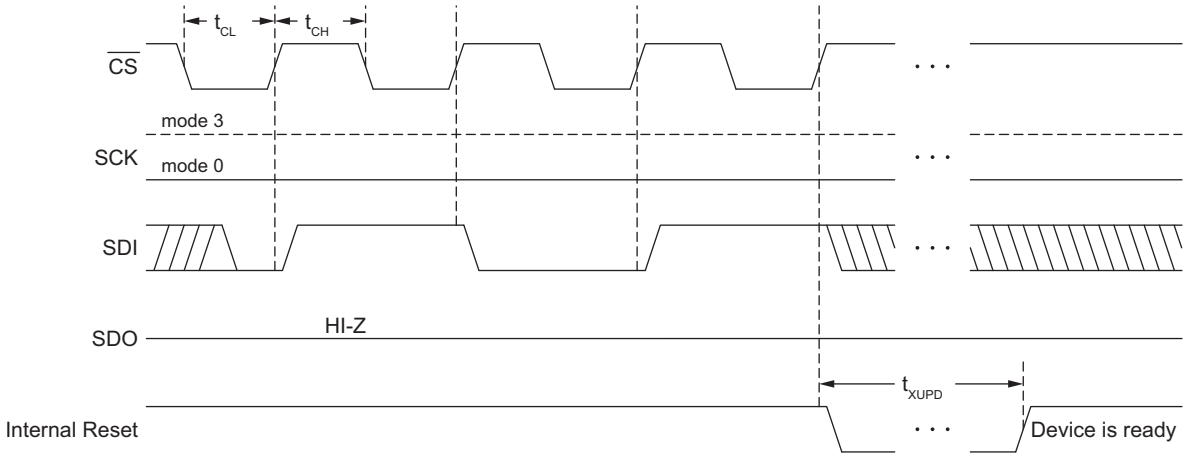
3) SDI is driven low by the bus master, simultaneously with $\overline{CS}$ going active low. No SPI bus slave drives SDI during $\overline{CS}$ low before a transition of SCK ie: slave streaming output active is not allowed until after the first edge of SCK.

4) $\overline{CS}$ is driven inactive. The slave captures the state of SI on the rising edge of $\overline{CS}$.

The above steps are repeated 4 times, each time alternating the state of SI.

After the fourth $\overline{CS}$ pulse, the slave triggers its internal reset. SI is low on the first $\overline{CS}$, high on the second, low on the third, high on the fourth. This provides a 5h, unlike random noise. Any activity on SCK during this time will halt the sequence and a Reset will not be generated. Figure 10-18 below illustrates the timing for the Hardware Reset operation.

Figure 10-18.Hardware Reset



11. Typical Characteristics

Figure 11-1. Icc4 , Auto Powerdown

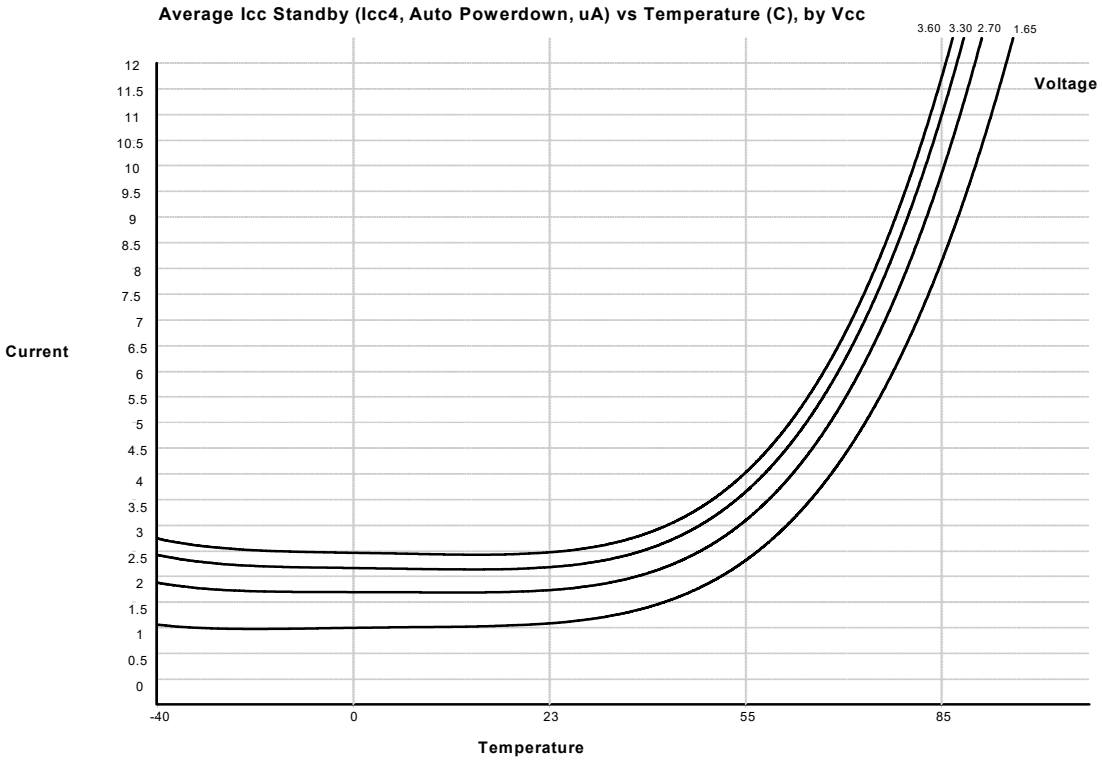


Figure 11-2. Icc4, Mode 0

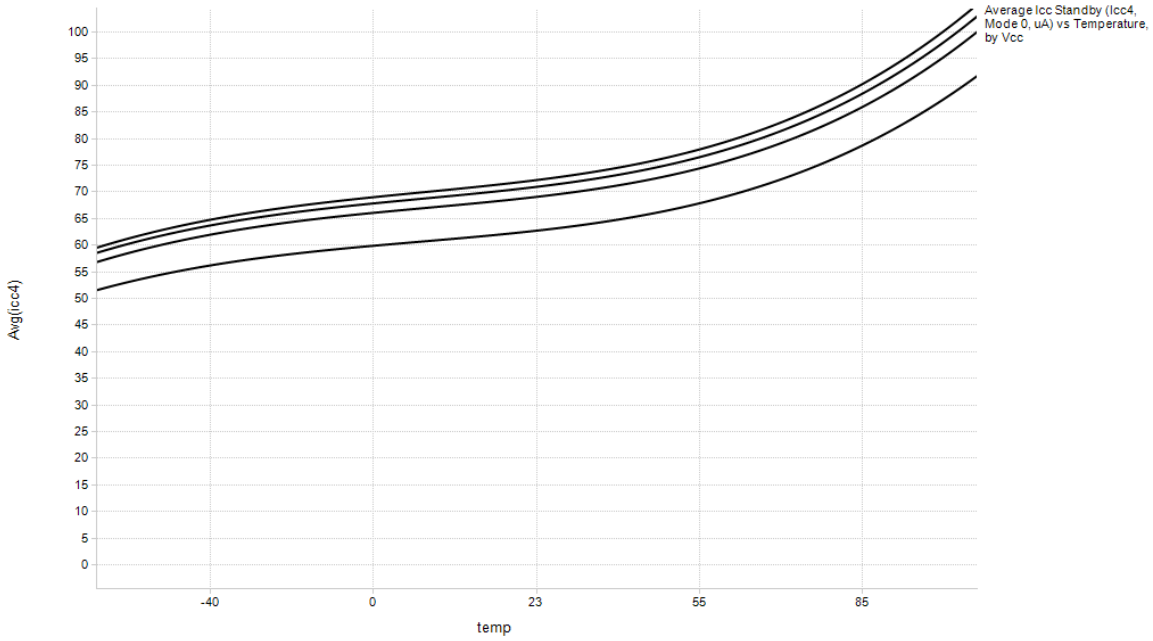


Figure 11-3. Icc4, Mode 1

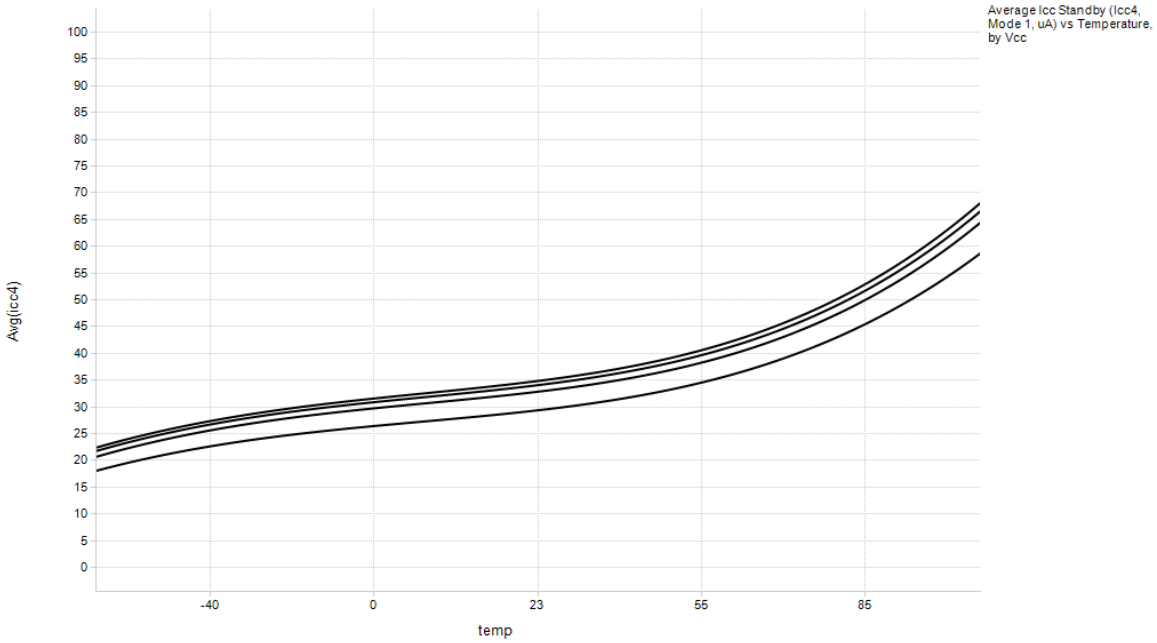


Figure 11-4. Icc5

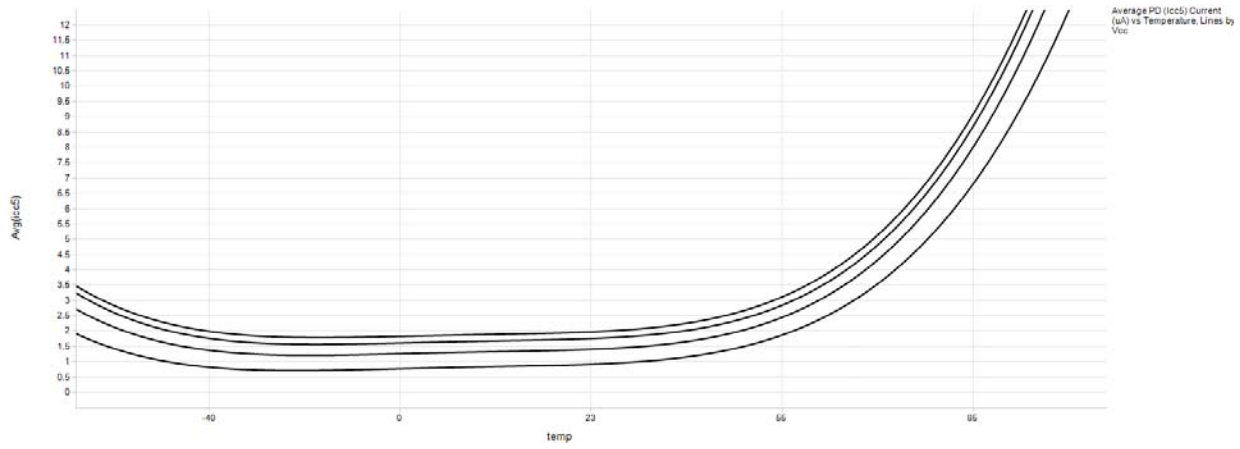
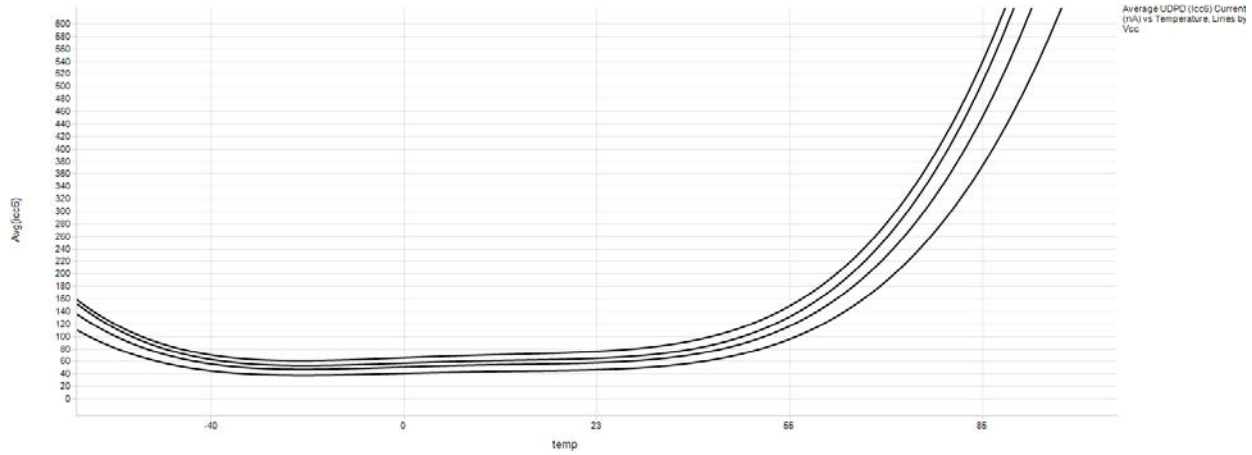
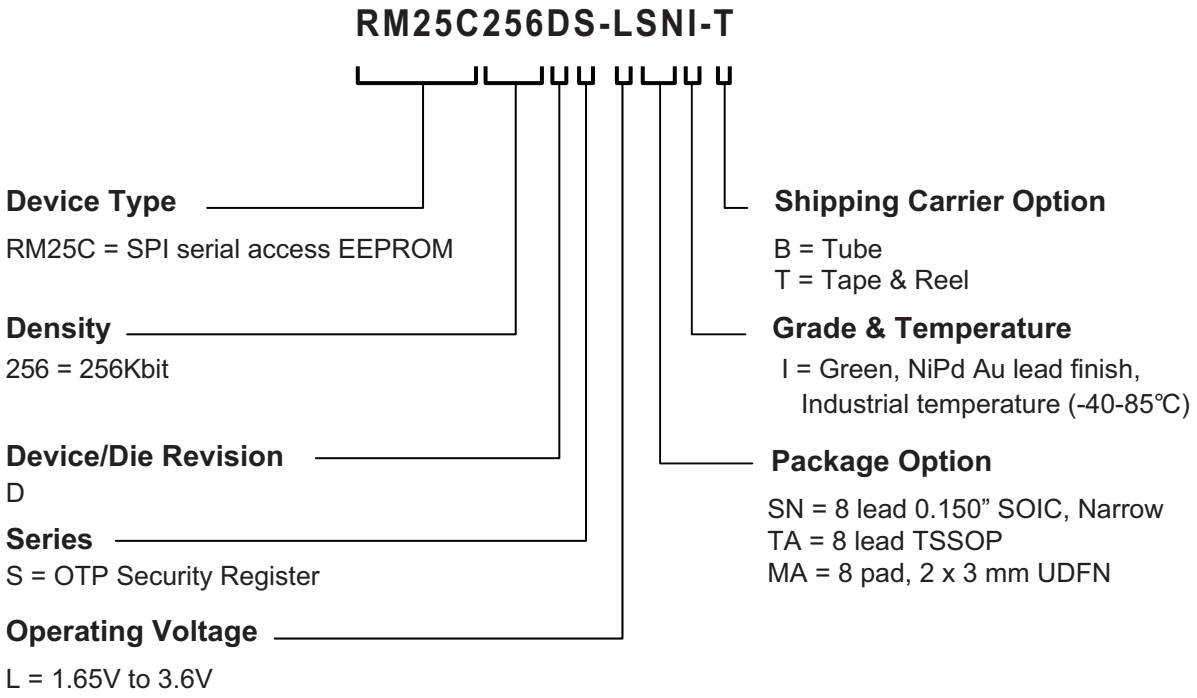


Figure 11-5. Icc6



12. Ordering Information

12.1 Ordering Detail



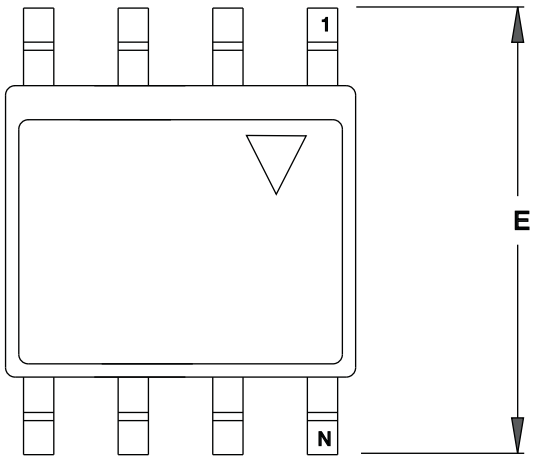
12.2 Ordering Codes

Ordering Code	Package	Density	Operating Voltage	f_{SCK}	Device Grade	Ship Carrier	Qty. Carrier
RM25C256CDS-LSNI-B	SN	256 Kbit	1.65V to 3.6V	20 MHz	Industrial (-40°C to 85°C)	Tube	100
RM25C256CDS-LSNI-T						Reel	4000
RM25C256CDS-LTAI-B	TA	256 Kbit	1.65V to 3.6V	20 MHz	Industrial (-40°C to 85°C)	Tube	100
RM25C256CDS-LTAI-T						Reel	4000
RM25C256CDS-LMAI-T	MA	256 Kbit	1.65V to 3.6V	20 MHz	Industrial (-40°C to 85°C)	Tube	5000

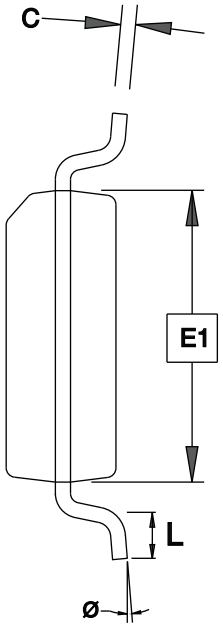
Package Type	
SN	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
TA	8-lead 3 x 4.4 mm, Thin Shrink Small Outline Package
MA	8-pad, 2 x 3 x 0.6mm, Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)

13. Package Information

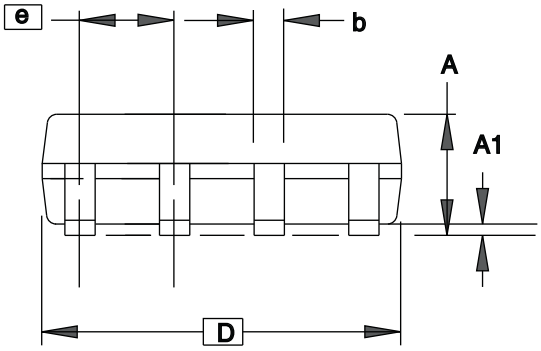
13.1 SN (JEDEC SOIC)



TOP VIEW



END VIEW



SIDE VIEW

Notes: This drawing is for general information only.
Refer to JEDEC Drawing MS-012, Variation AA
for proper dimensions, tolerances, datums, etc.

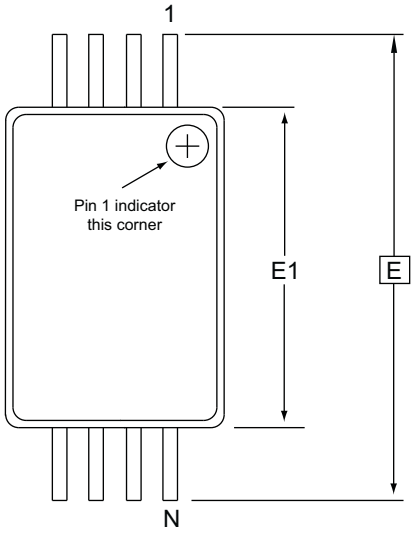
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

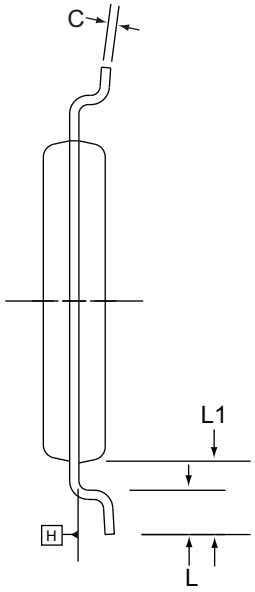
8/20/14

adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE 8S1, 8-lead (0.150"Wide Body), Plastic Gull Wing Small Outline (JEDEC SOIC)	GPC SWB	DRAWING NO. 8S1	REV. G

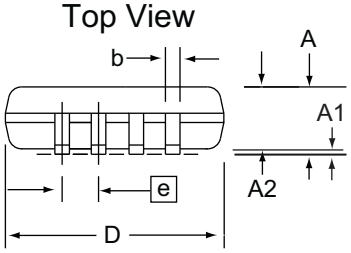
13.2 TA-TSSOP



Top View



End View



Side View

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-153, Variation AA, for proper dimensions, tolerances, datums, etc.
2. Dimension D does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15mm (0.006in) per side.
3. Dimension E1 does not include inter-lead Flash or protrusions. Inter-lead Flash and protrusions shall not exceed 0.25mm (0.010in) per side.
4. Dimension b does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08mm total in excess of the b dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protrusion and adjacent lead is 0.07mm.
5. Dimension D and E1 to be determined at Datum Plane H.

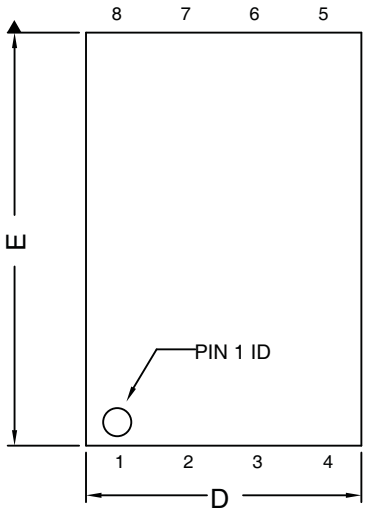
COMMON DIMENSIONS
(Unit of Measure = mm)

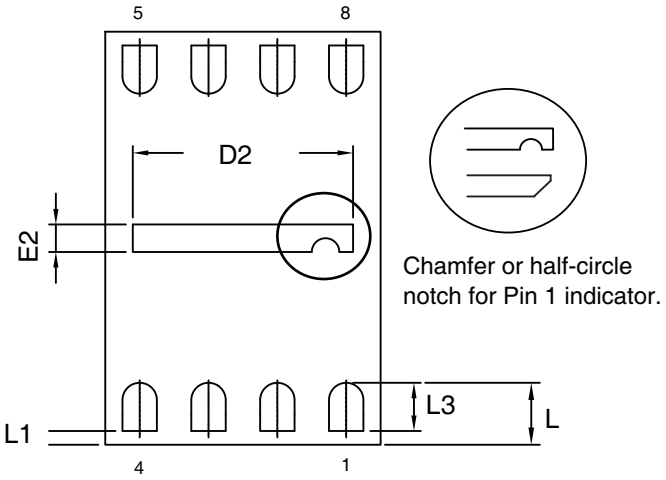
SYMBOL	MIN	NOM	MAX	NOTE
A	-	-	1.20	
A1	0.05	-	0.15	
A2	0.80	1.00	1.05	
D	2.90	3.00	3.10	2, 5
E		6.40 BSC		
E1	4.30	4.40	4.50	3, 5
b	0.19	–	0.30	4
e		0.65 BSC		
L	0.45	0.60	0.75	
L1		1.00 REF		
C	0.09	-	0.20	

12/8/11

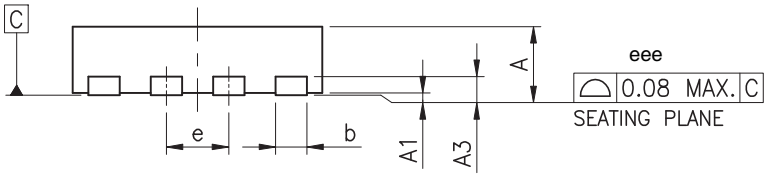
adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	TITLE TA, 8-lead 4.4mm Body, Plastic Thin Shrink Small Outline Package (TSSOP)	GPC TNR	DRAWING NO. 8X	REV. E

13.3 MA- – 2 x 3 UDFN





Chamfer or half-circle notch for Pin 1 indicator.



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX
A	0.45		0.60
A1	0.00		0.05
A3		0.150 REF	
b	0.20		0.30
D		2.00 BSC	
D2	1.50	1.60	1.70
E		3.00 BSC	
E2	0.10	0.20	0.30
e		0.50 BSC	
L	0.40	0.45	0.50
L1	0.00	0.10	
L3	0.30		0.50
eee	–	–	0.08

Notes: 1. All dimensions are in mm. Angles in degrees.
2. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.

8/26/14

	TITLE	GPC	DRAWING NO.	REV.
adesto TECHNOLOGIES Package Drawing Contact: contact@adestotech.com	8MA3, 8-pad, 2 x 3 x 0.6 mm Body, 0.5 mm Pitch, 1.6 x 0.2 mm Exposed Pad, Saw Singulated Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN/USON)	YCQ	8MA3	GT

13.4 Revision History

Doc. Rev.	Date	Comments
RM25C256DS-A	7/2016	Initial document release
RM25C256DS-B	11/2016	Updated Endurance and Data Retention specifications. Updated T_{PW} and T_{BW} specifications. Updated DC specifications and Typical Characteristics curves.
RM25C256DS-C	11/2017	Added patent information.

Corporate Office

California | USA
Adesto Headquarters
3600 Peterson Way
Santa Clara, CA 95054
Phone: (+1) 408.400.0578
Email: contact@adestotech.com