

U\_B2B-Connectors  
B2B-Connectors.SchDoc

U\_B13  
B13.SchDoc

U\_B14  
B14.SchDoc

U\_B15  
B15.SchDoc

U\_B16  
B16.SchDoc

U\_B34  
B34.SchDoc

U\_FPGA-MGT  
FPGA-MGT.SchDoc

U\_FPGA-CFG  
FPGA-CFG.SchDoc

U\_FPGA-PWR  
FPGA-PWR.SchDoc

U\_Clock  
Clock.SchDoc

U\_DDR3-RAM  
DDR3-RAM.SchDoc

U\_ETHERNET  
ETHERNET.SchDoc

U\_CPLD  
CPLD.SchDoc

U\_PWR1  
PWR1.SchDoc

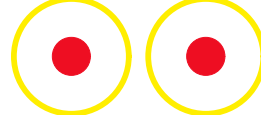
U\_PWR2  
PWR2.SchDoc

Serial  
Serialnumber 6,3 x 6.3mm

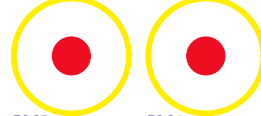
FIDU-DOT - small FIDU-DOT - small



PM1 PM2  
FIDU-DOT - small FIDU-DOT - small

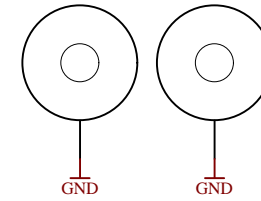


PM3 PM4  
FIDU-DOT - small FIDU-DOT - small

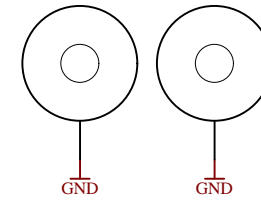


PM5 PM6

Mount.Hole 3.2mm Mount.Hole 3.2mm




Mount.Hole 3.2mm Mount.Hole 3.2mm



Top of Board



	Title: <b>TE0712</b>		
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	Filename: <b>TE0712.SchDoc</b>		

A

B

C

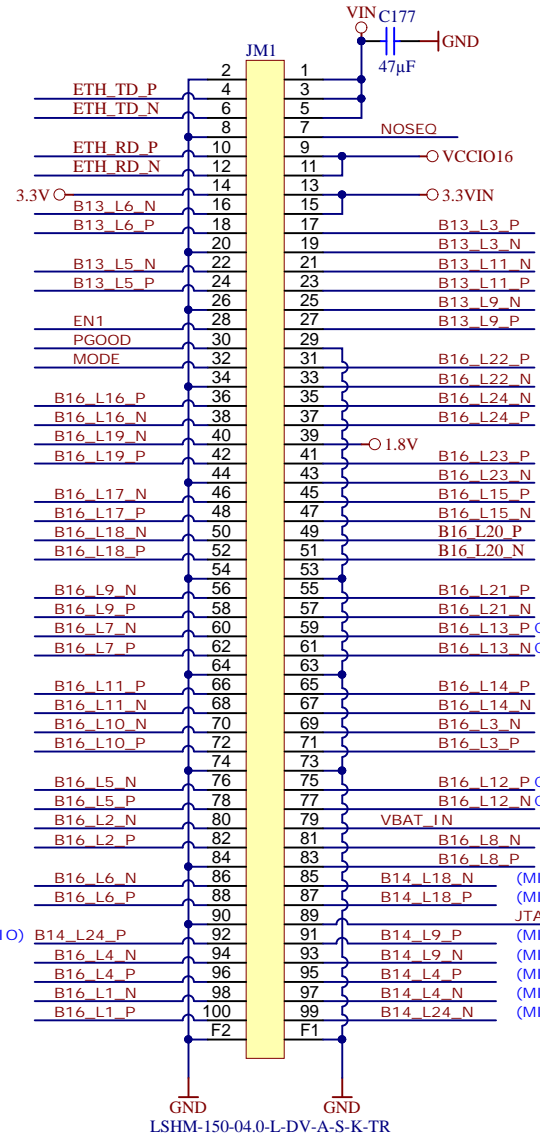
D

A

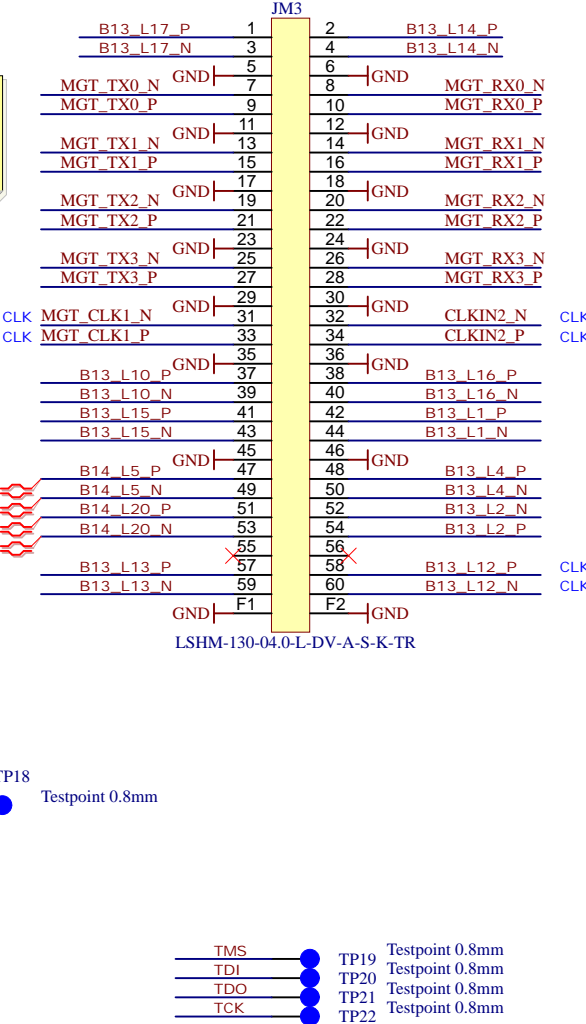
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C

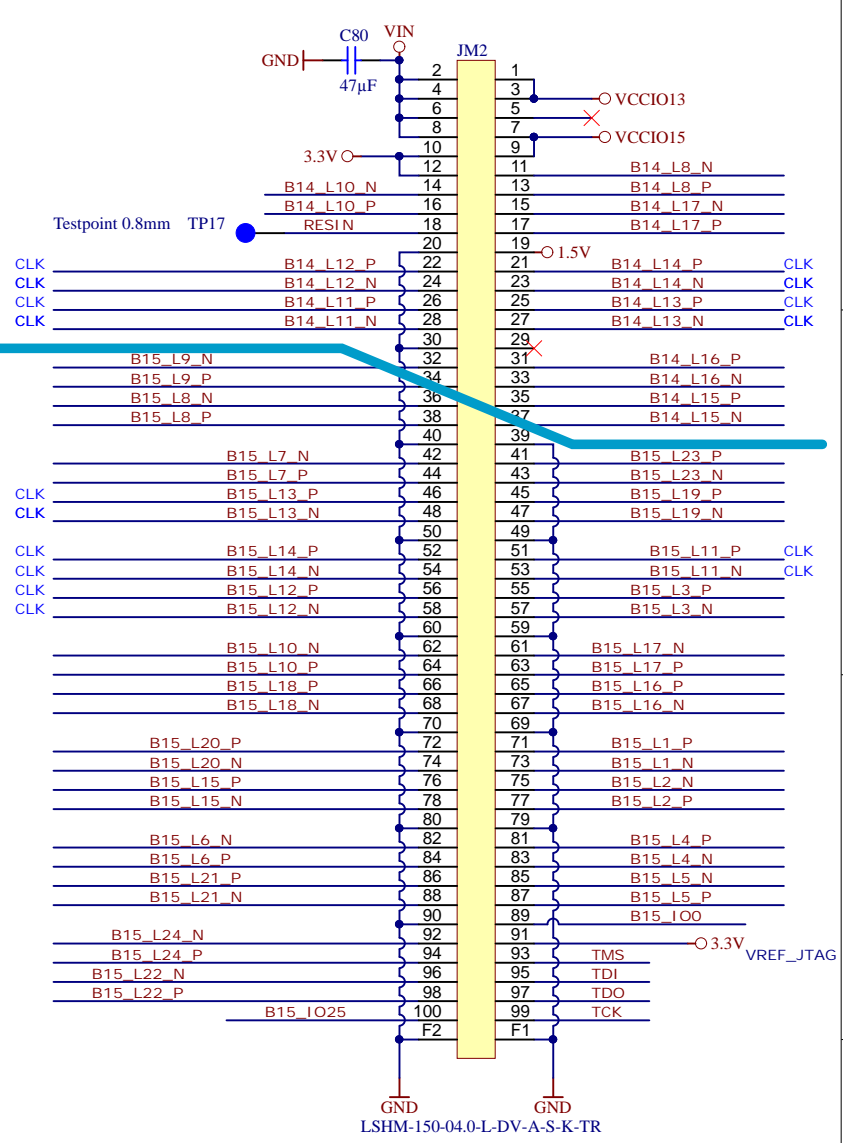
D



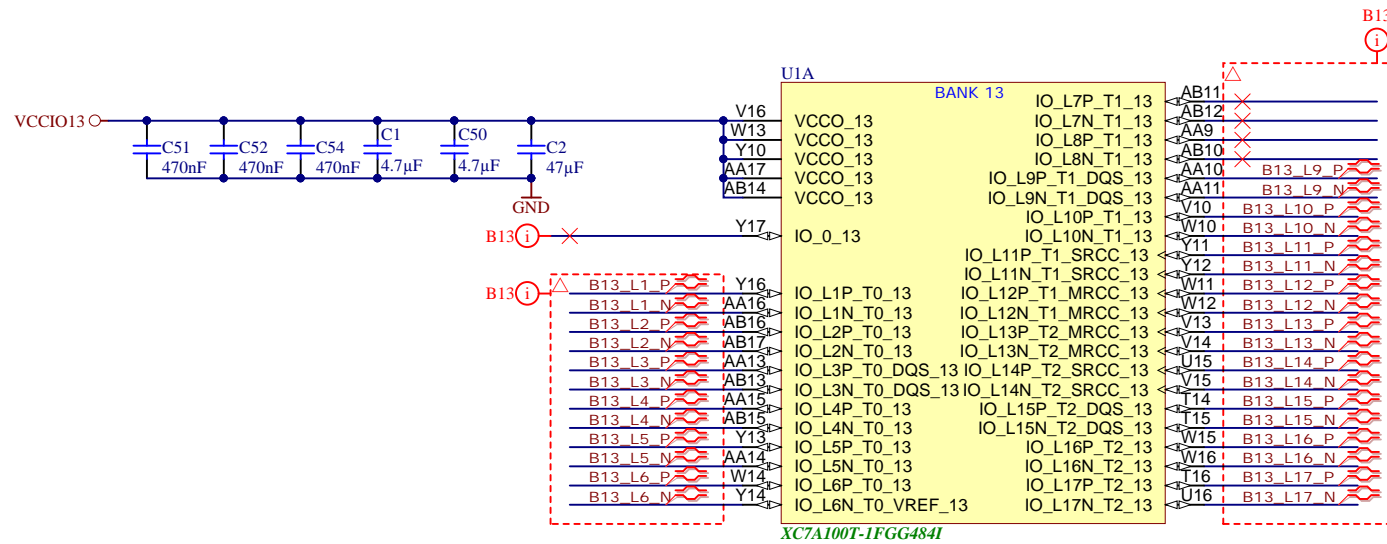
These IOs are on B13 Vcc not 1.8V!!!



- TMS ● TP19 Testpoint 0.8mm
- TDI ● TP20 Testpoint 0.8mm
- TDO ● TP21 Testpoint 0.8mm
- TCK ● TP22 Testpoint 0.8mm



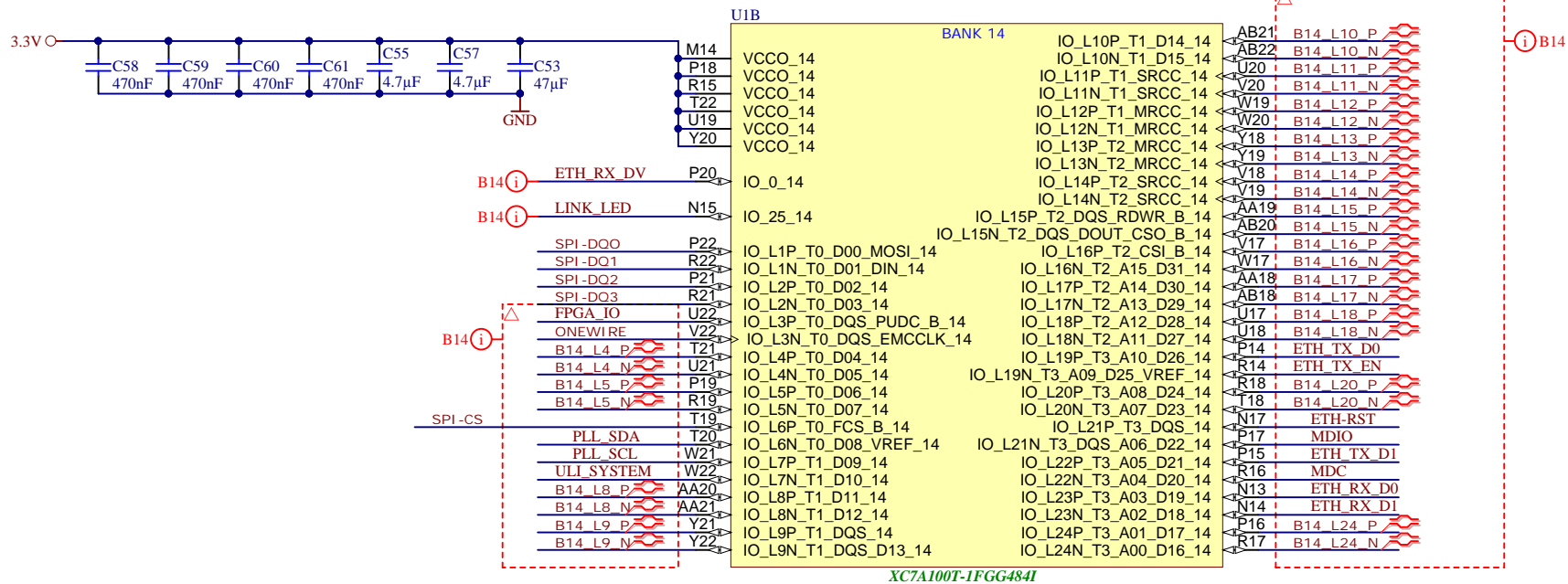
Title: B2B		
A4	Number: TE0712 100_11	Rev. 02
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Filename: B2B-Connectors.SchDoc		



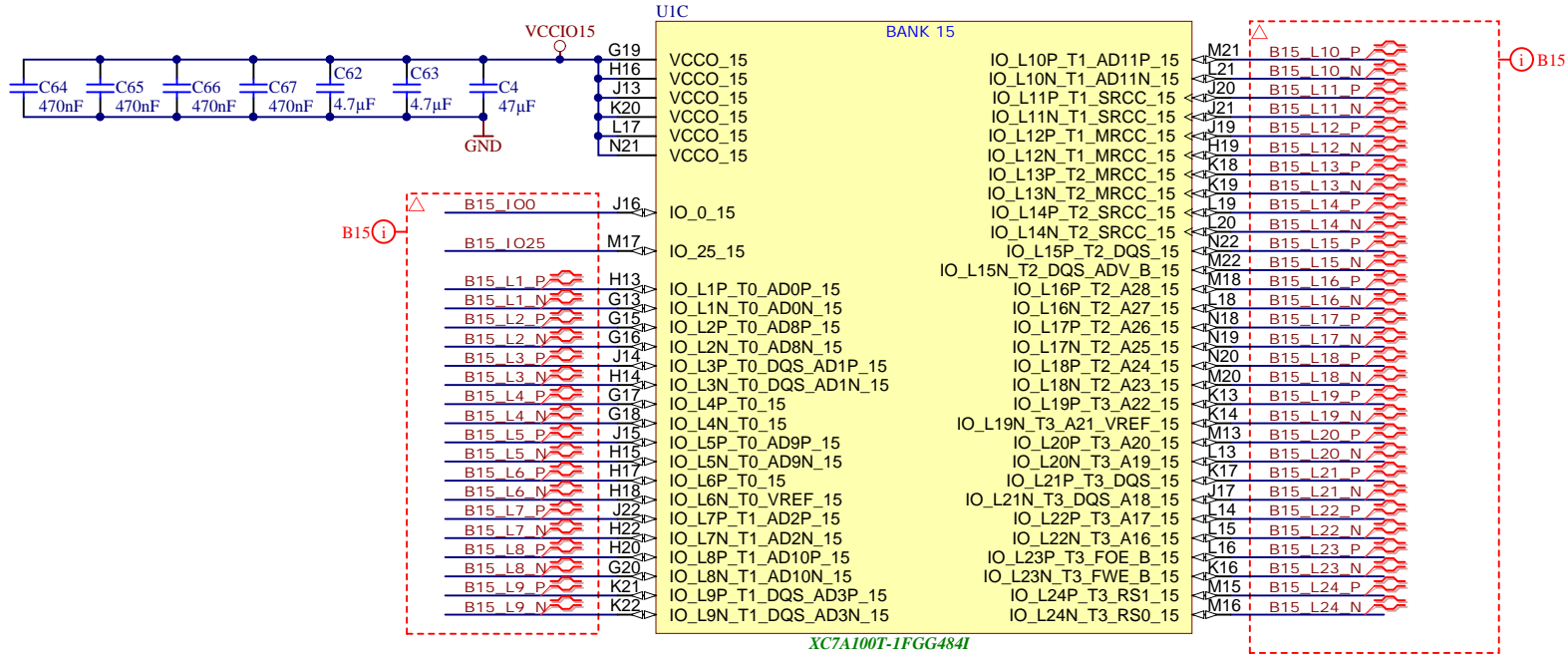
XC7A100T-IFGG484I



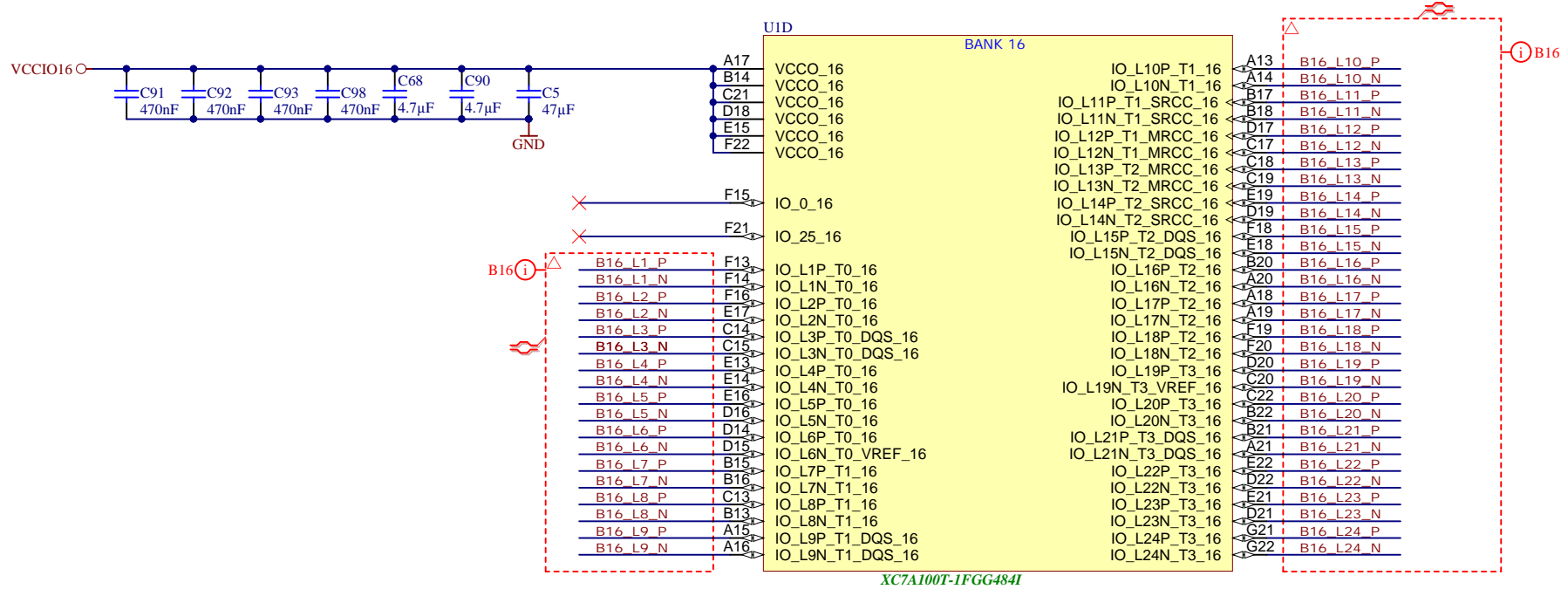
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A4	Number: <b>TE0712 100_11</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>3</b> of <b>16</b>
Filename: <b>B13.SchDoc</b>		



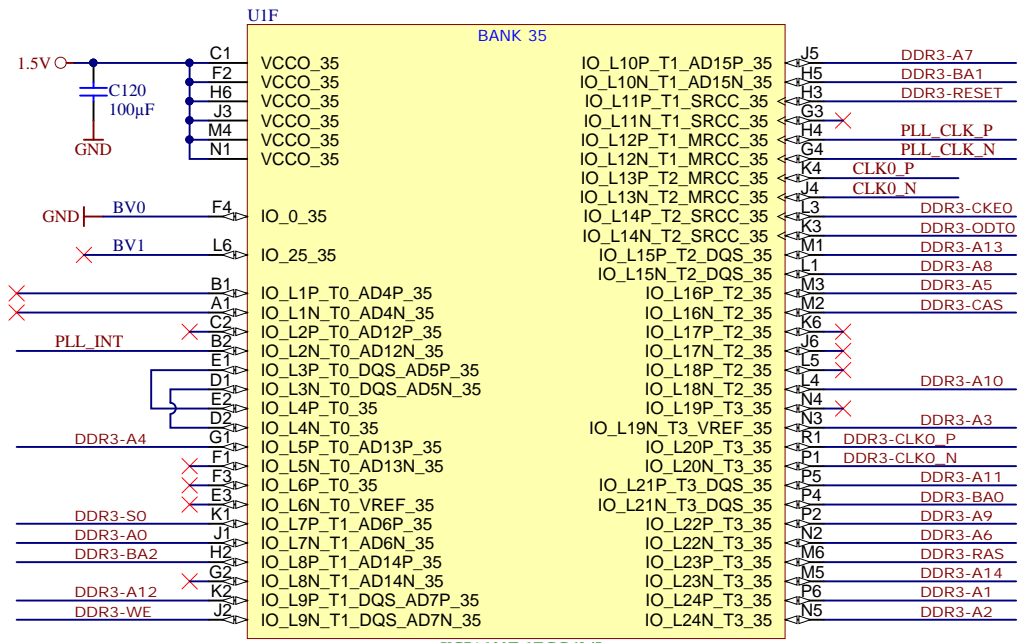
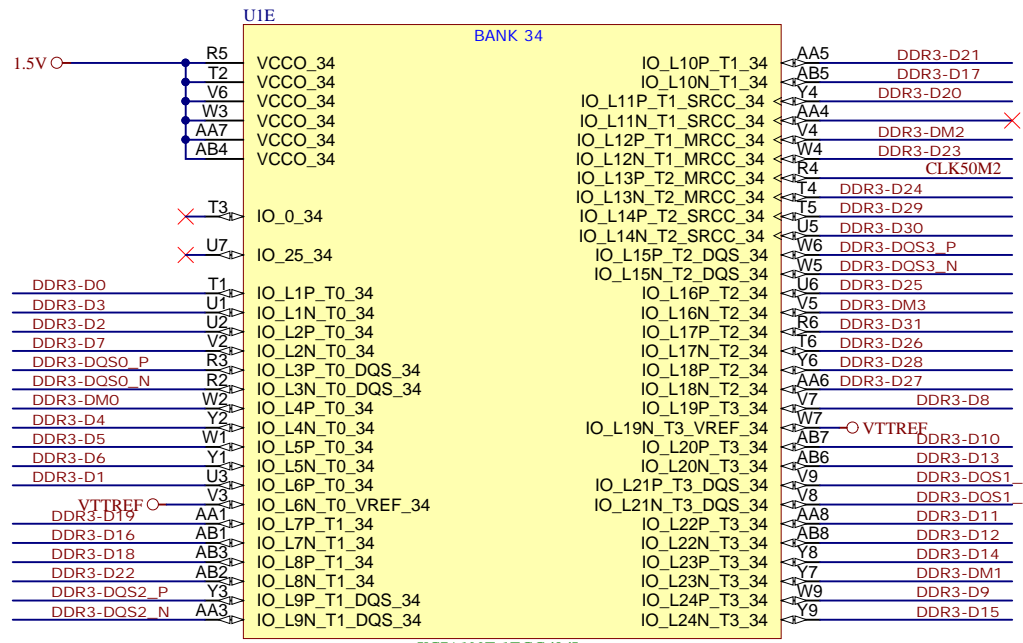
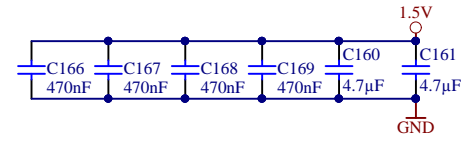
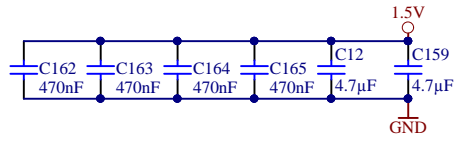
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A4	Number: <b>TE0712 100_11</b>	Rev. <b>02</b>
Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>4</b> of <b>16</b>
Filename: <b>B14.SchDoc</b>		



Title: <b>B15</b>		
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Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>5</b> of <b>16</b>
Filename: <b>B15.SchDoc</b>		

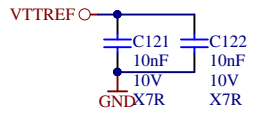
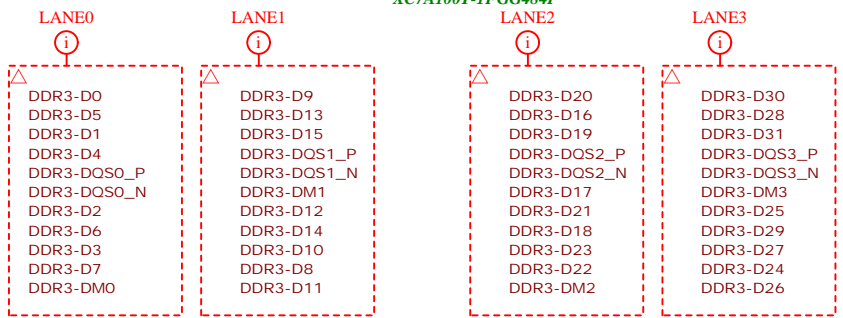


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	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>6</b> of <b>16</b>
	Filename: <b>B16.SchDoc</b>		

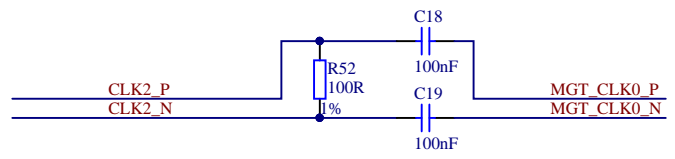
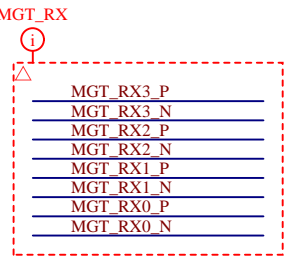
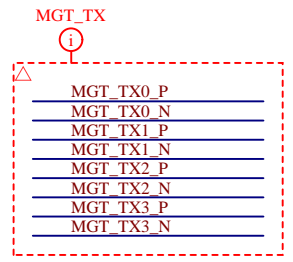
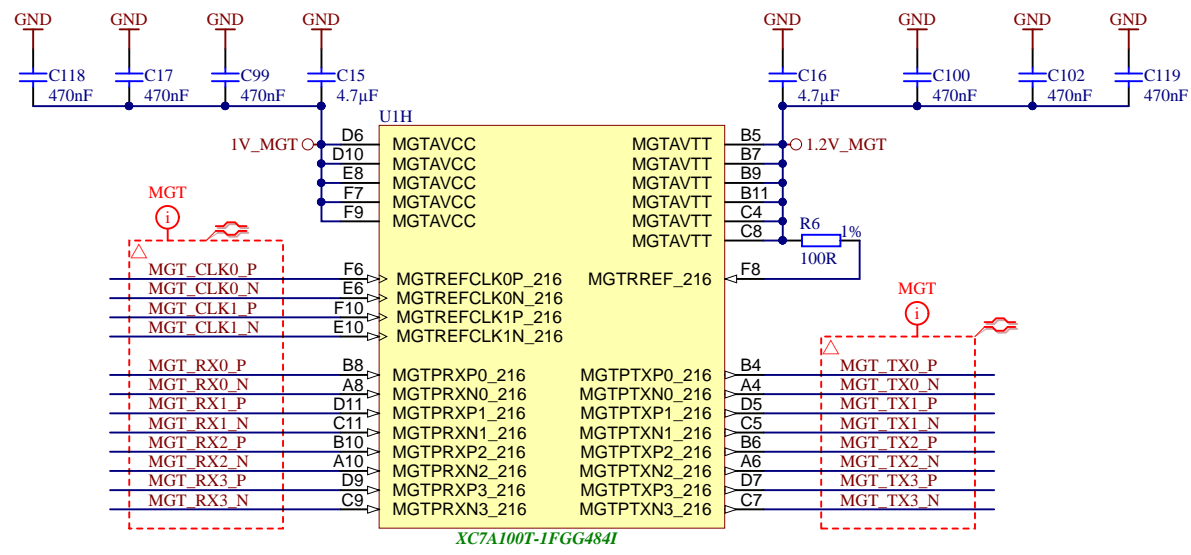


XC7A100T-1FGG484I

XC7A100T-1FGG484I

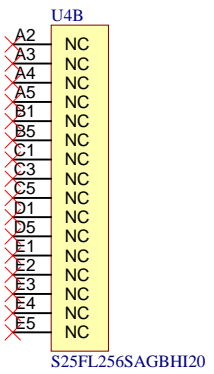
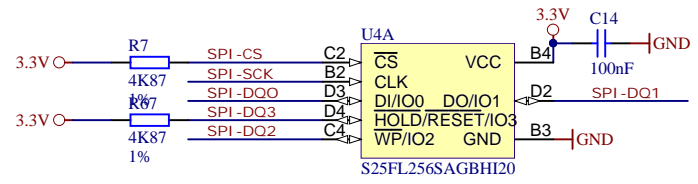
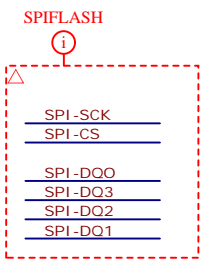
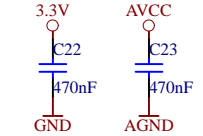
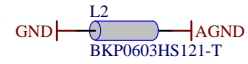
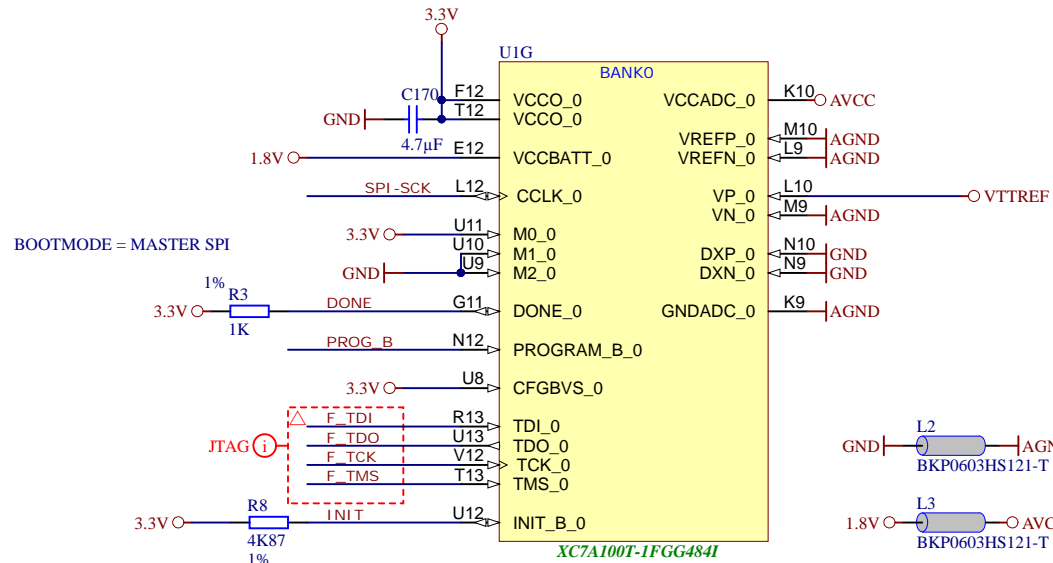


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A4	Number: TE0712 100_11	Rev. 02
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Filename: B34.SchDoc		

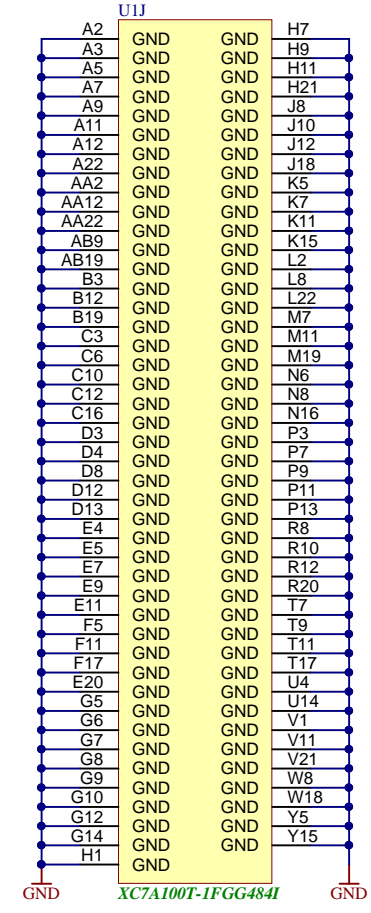
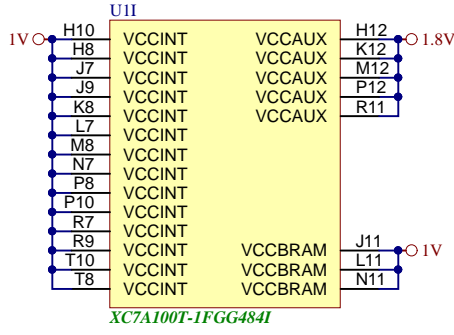
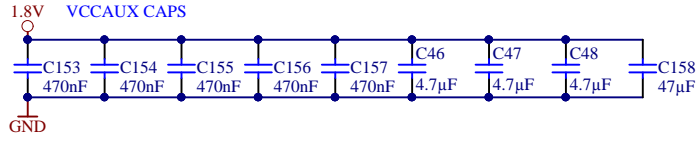
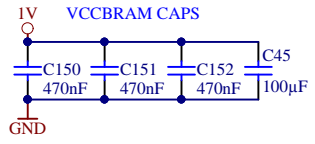
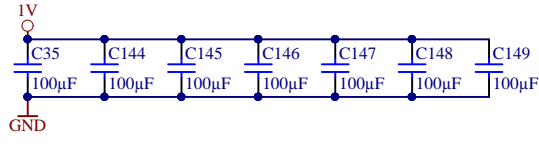
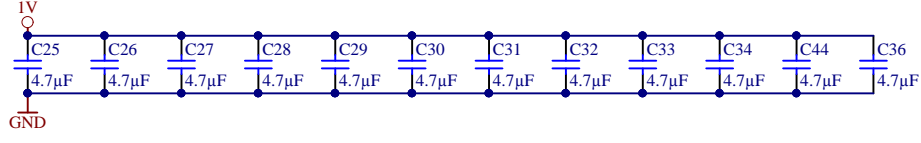
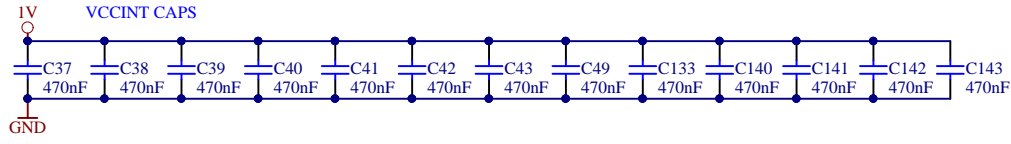


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A4	Number: TE0712 100_11	Rev. 02
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Filename: FPGA-MGT.SchDoc		

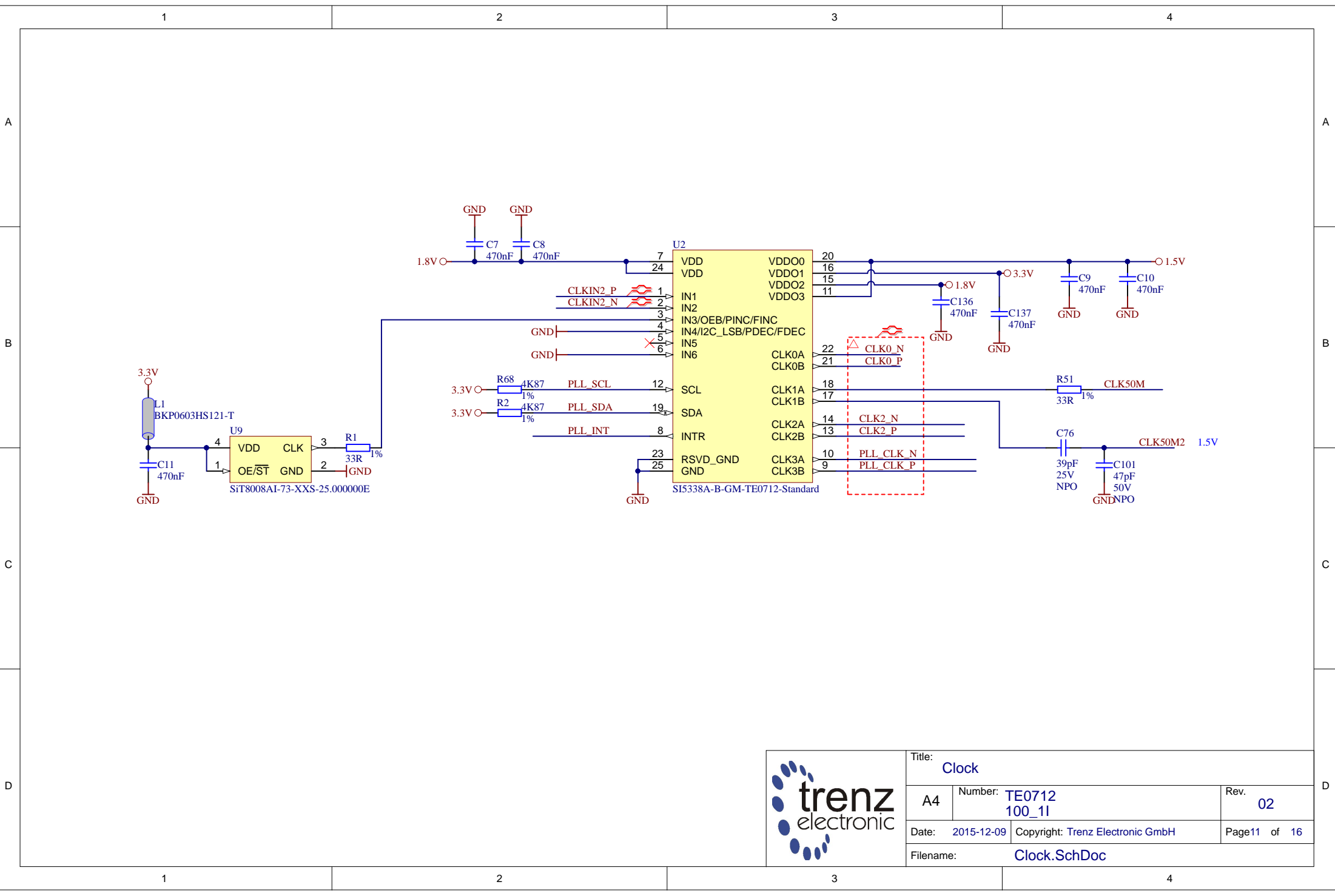





Title: CFG		
A4	Number: TE0712 100_11	Rev. 02
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Filename: FPGA-CFG.SchDoc		



Title: <b>PWR</b>		
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Filename: <b>FPGA-PWR.SchDoc</b>		



		Title: <b>Clock</b>	
		A4	Number: <b>TE0712 100_11</b>
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Filename: <b>Clock.SchDoc</b>		Page 11 of 16	

A

A

B

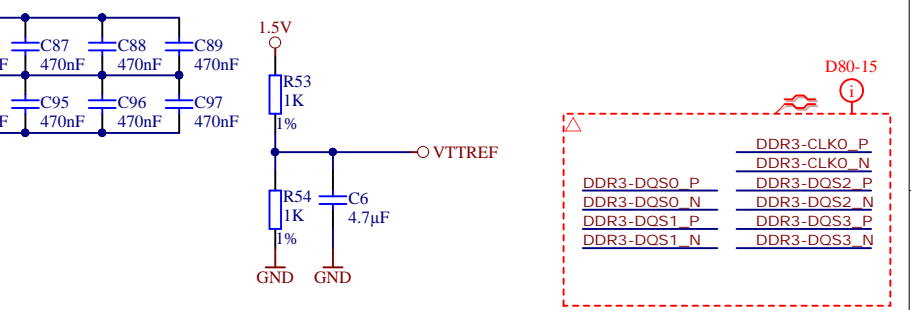
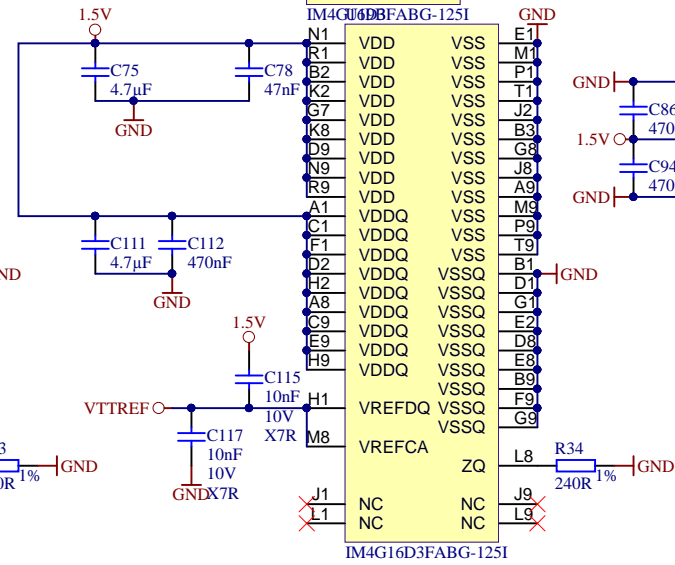
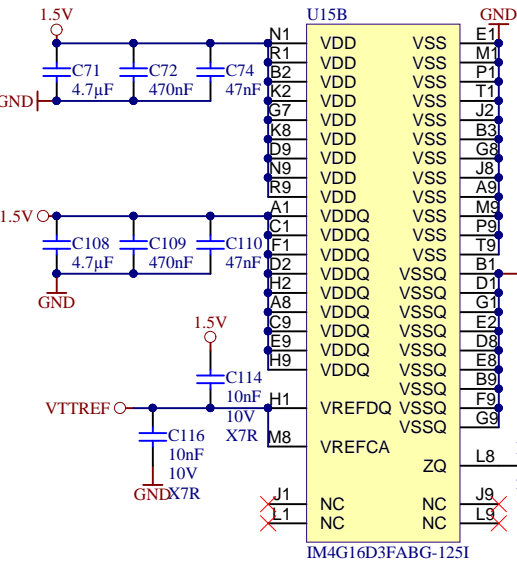
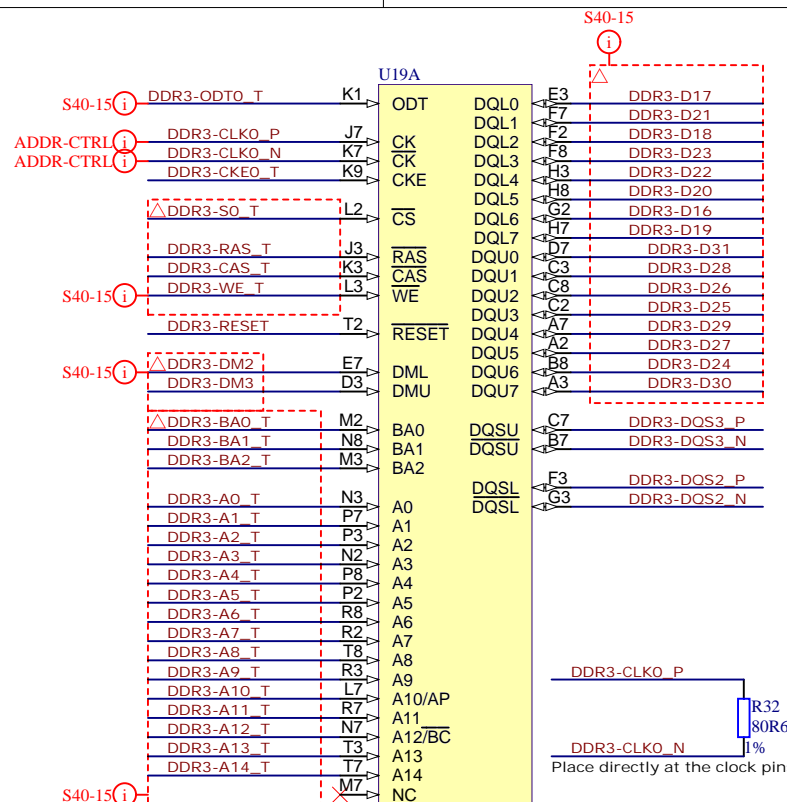
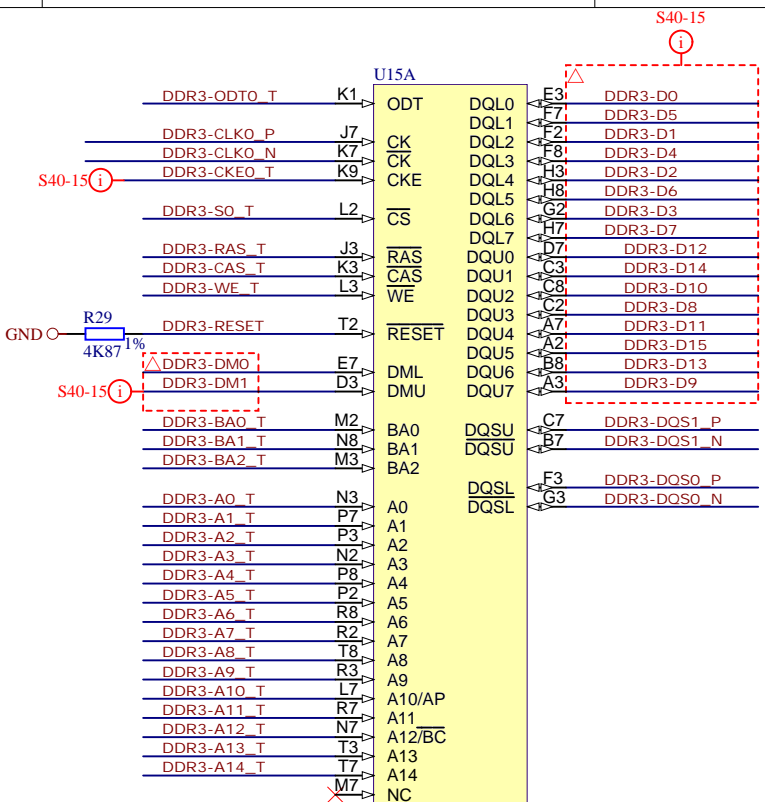
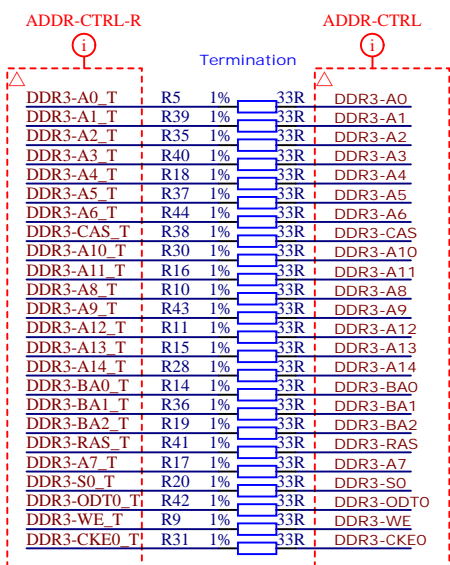
B

C

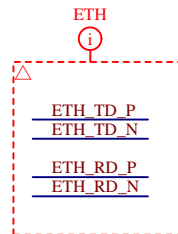
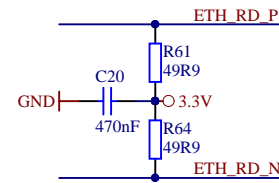
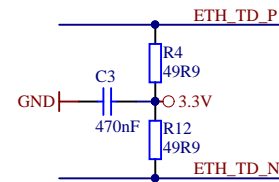
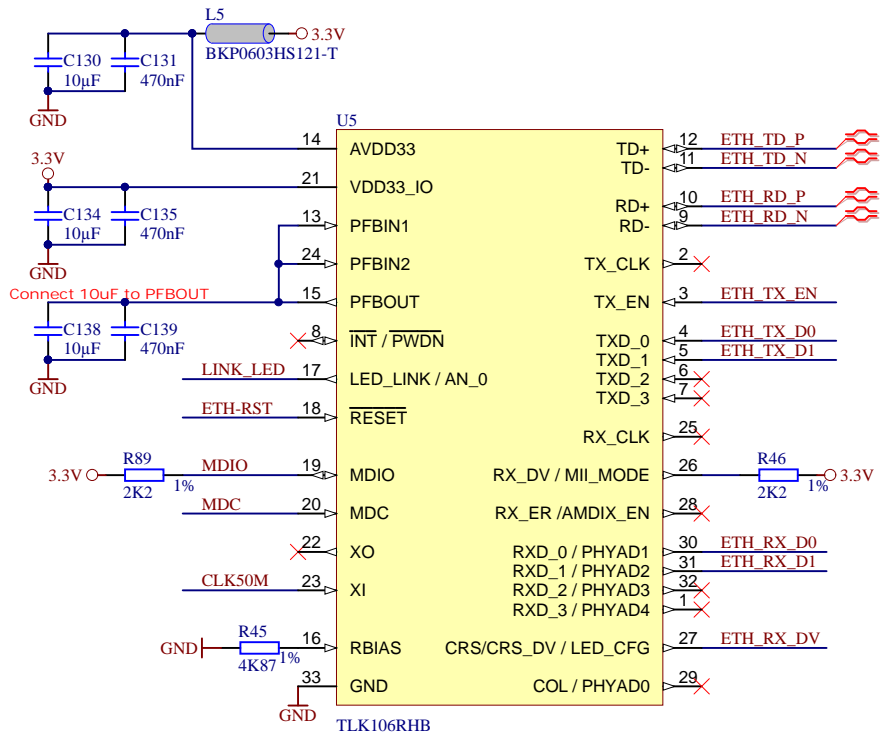
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D

D



Title: <b>DDR3</b>			
A4	Number: <b>TE0712 100_11</b>	Rev. <b>02</b>	
Date: 2015-12-09	Copyright: Trenz Electronic GmbH		Page 12 of 16
Filename: <b>DDR3-RAM.SchDoc</b>			



	Title: <b>ETH</b>		
	A4	Number: <b>TE0712 100_11</b>	Rev. <b>02</b>
	Date: <b>2015-12-09</b>	Copyright: <b>Trenz Electronic GmbH</b>	Page <b>13</b> of <b>16</b>
	Filename: <b>ETHERNET.SchDoc</b>		

1

2

3

4

A

A

B

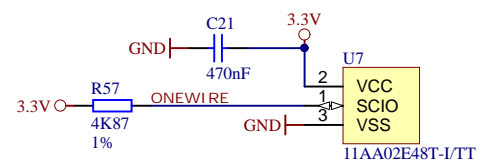
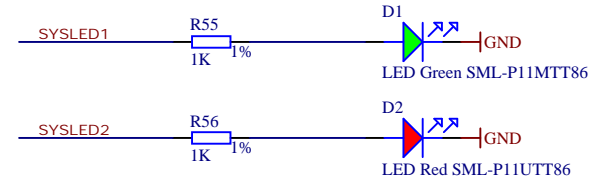
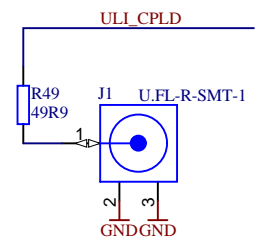
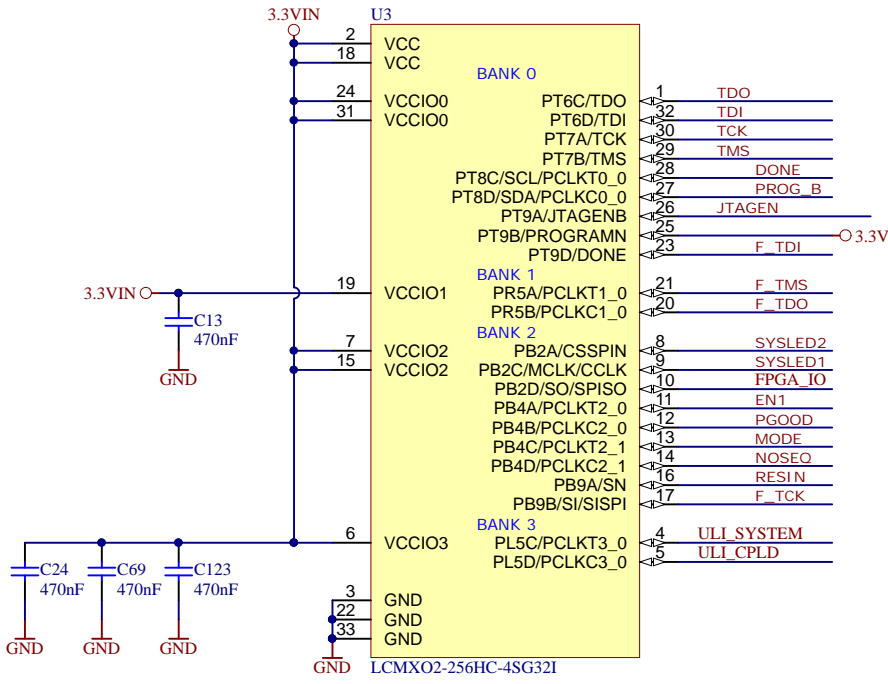
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C

C

D

D



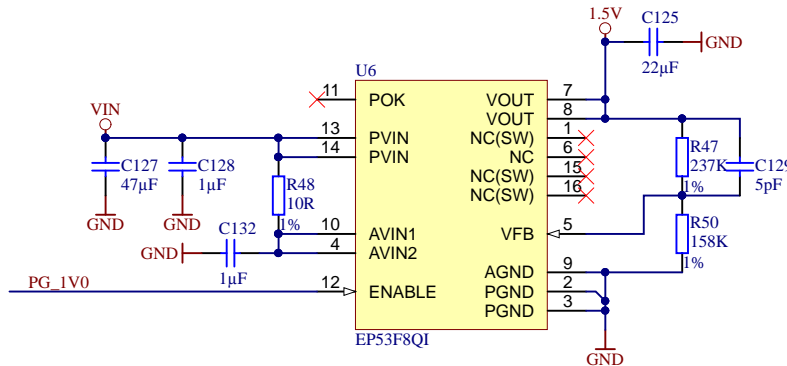
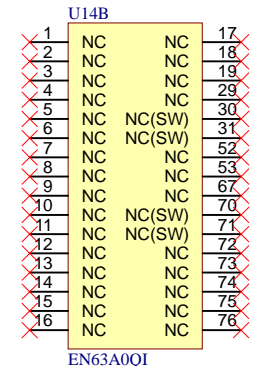
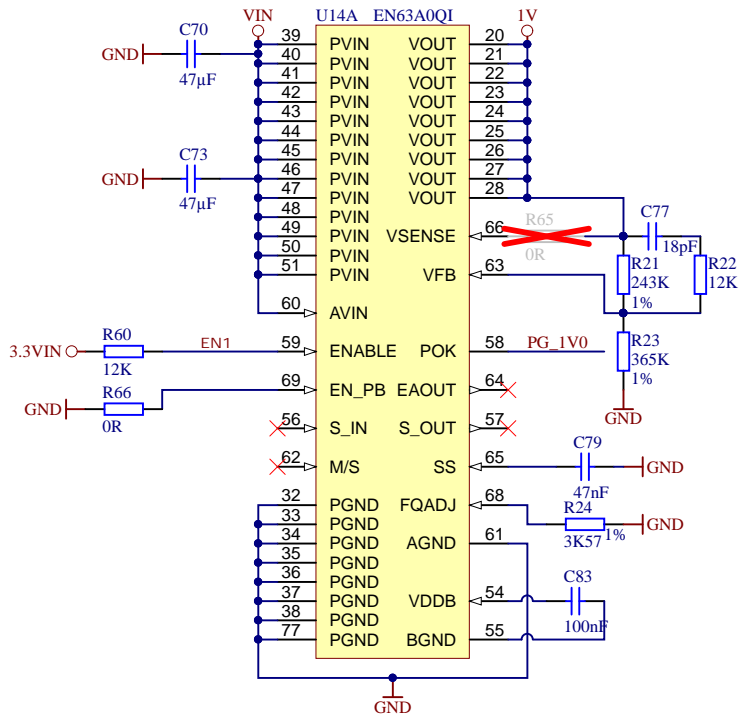
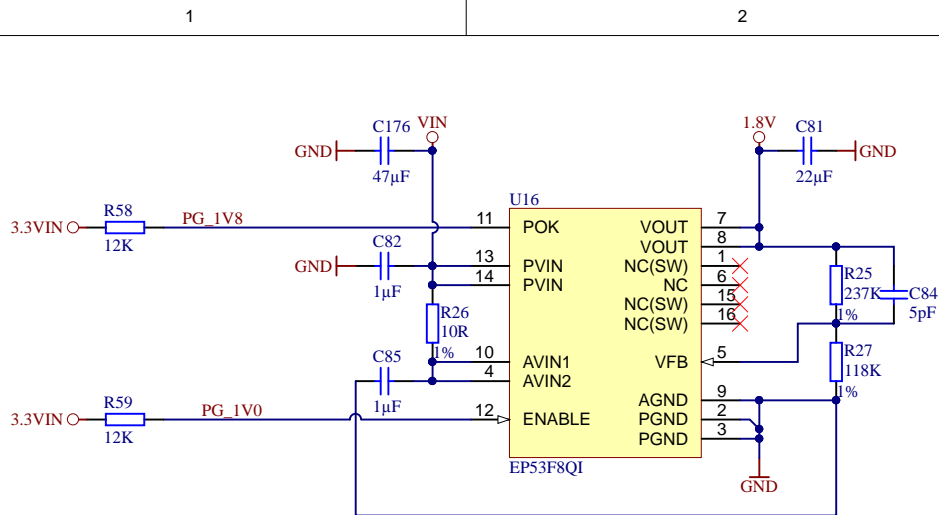
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A4	Number: TE0712 100_11	Rev. 02
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Filename: CPLD.SchDoc		

1

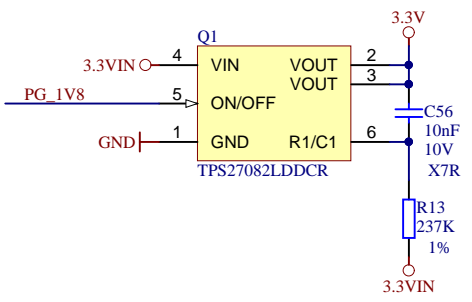
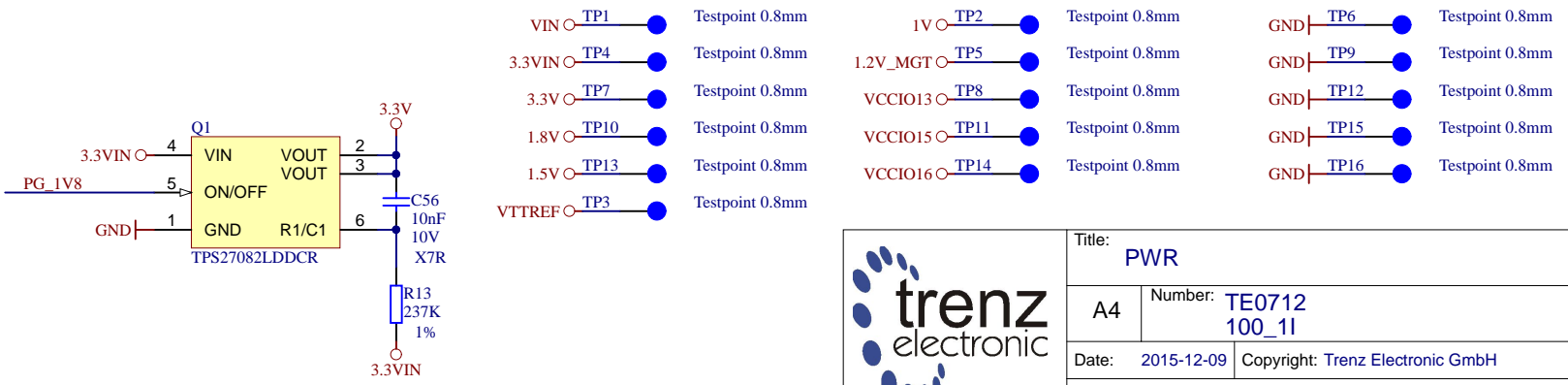
2

3

4



R65	R66	MODE	EN63A0QI
OK	X		enable pre-bias start-up
X	OK		disable pre-bias start-up



Title: PWR		
A4	Number: TE0712 100_11	Rev. 02
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1

2

3

4

A

A

B

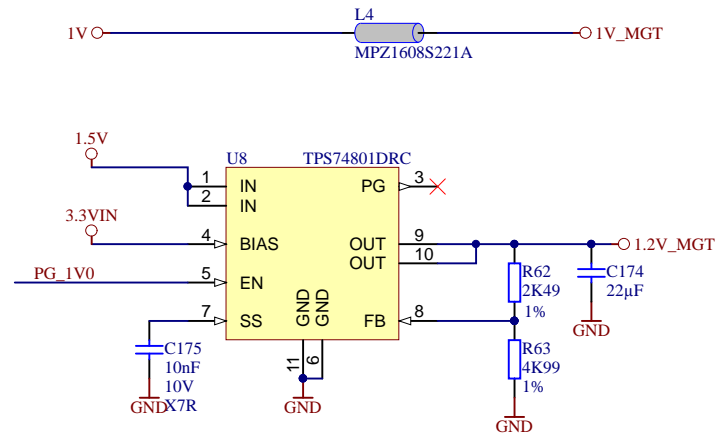
B

C

C

D

D



Title: PWR		
A4	Number: TE0712 100_11	Rev. 02
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1

2

3

4