User's Guide ADC364xEVM Evaluation Module

TEXAS INSTRUMENTS

Abstract

This user's guide describes the characteristics, operation, and use of the ADC364x evaluation module (EVM). This user's guide discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms evaluation board, evaluation module, and EVM are synonymous with the ADC364xEVM. In the following sections of this document, the ADC364x evaluation board is referred to as the EVM and the ADC364x device is referred to as the ADC device.

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1 Introduction

The ADC364xEVM is an evaluation board used to evaluate the ADC364x analog-to-digital converter (ADC) from Texas Instruments. The ADC364xEVM is a dual-channel, 14-bit ADC that can operate up to 125 Mega-samples per second (MSPS). The ADC364x uses a parallel or serial CMOS interface to output the digital data. The serialized CMOS interface supports output rates to 250 Mbps which translates to ~ 30 MSPS (2-wire) to ~ 10 MSPS (0.5-wire) output rates after complex decimation. Hence the ADC3643 can be operated in 'oversampling + decimating' mode using the internal decimation filter in order to improve the dynamic range and relax external anti-aliasing filter.

The ADC364xEVM is equipped with the following features:

- Transformer and FDA coupled analog inputs
- CDCE6214 clocking solution for on-board clocking
- Transformer coupled or single-ended clock inputs
- INA226 current shunt monitors for evaluating power consumption
- Power over mini-USB
- FMC connector



2 Equipment

This hardware setup procedure is written with the intent to use the onboard CDC clocking option, and therefore only requires an analog input for evaluation. Using an external sampling clock(s) is an option, and instructions are provided toward the end of this document.

2.1 Evaluation Board Feature Identification Summary



Figure 2-1. ADC364xEVM Feature Identification

Ensure that jumper J8 is shunted in the 2-3 position. This allows 5 V to be supplied to the ADC364xEVM through the mini-USB connector.

If an external 5-V supply is desired, J8 must be shunted in the 1-2 position, and the external 5 V can be connected to the test point labeled "+5 EXT".



Figure 2-2. CMOS FPGA Interposer Card

2.2 Required Equipment

- The following equipment is included in the EVM evaluation kit:
 - ADC364x Evaluation board (EVM)
 - CMOS FPGA Interposer Card
 - Power supply clips for Interposer Card
 - Mini-USB cable

The following equipment is **not** included in the EVM evaluation kit, but is required for evaluation of this EVM:

- TSW1400EVM data capture board and related items
- HSDC Pro software
- PC running Microsoft[®] Windows[®] 7, or 10
- One low-noise signal generators for the analog input (If using external clock option, additional signal generator is required).

TI recommends the following generators:

- Rohde & Schwarz SMA100A
- Rohde & Schwarz SMA100B

Bandpass filter for the analog input signal. The following recommended bandpass filter will have:

- Bandpass filter, greater than or equal to 60-dB harmonic attenuation, less than or equal to 5% bandwidth, greater than 18-dBm power, less than 5-dB insertion loss
- Signal-path cables, SMA



3 Setup Procedure

This Setup Procedure will detail how to setup the software GUIs and EVM hardware required for evaluation using the onboard clock (CDCE6214).

3.1 Install High-Speed Data Converter (HSDC) Pro Software

Download the most recent version of the HSDC Pro software. Launch the executable, and accept the default installation options.

Download and install the HSDC Pro Patch. This patch copies all the INI files required to the HSDC pro directory.

3.2 Install ADC35XXEVM GUI 1.0 Software

Download the ADC35XXEVM GUI 1.0 software from the EVM tool folder at ADC3643EVM.

Extract and run the executable file, and accept the default installation options.

3.3 Connect the ADC EVM and TSW1400EVM

Connect the ADC364xEVM FMC connector to J1 of the FPGA Interposer Card.

Connect J2 of the FPGA Interposer Card to J1 of the TSW1400EVM.



Figure 3-1. ADC3660EVM Full Setup



3.4 Connect the Power Supply and Mini-USB Connections

Use the following steps to connect the power supply and mini-USB connections:

- 1. Connect 3.3 VDC to TP2 of the FPGA Interposer card. Provide power supply ground to TP1, as required. J10 of the TSW1400EVM can be used to source this +3.3 VDC.
- 2. Connect the power cable to the TSW1400EVM at 5-V (minimum 3 A) power supply. Place the power switch (SW7) to the "On" position.
- 3. Connect the mini-USB cable to the TSW1400EVM (J2).
- 4. Connect the mini-USB cable to the ADC3643EVM (J14).



4 Device Configuration

A hardware reset should be performed before programming the ADC by toggling the push button switch S1.

A software reset may be performed at any time to reset the ADC registers to their default state.

👪 ADC35XX EVM GUI	-		×
REFB VREF AIN BIN CLK	ur Voltage VREF, Control and PDN Control & Power Down ur Output Digital Downconverter Durput ur Output Digital Features Digital Features ur Uput Digital Features Output Interface voltage is bit Digital Features Volta (mA) 65.6 voltage is bit Digital Features with 100F load with 100F load voltage is bit is bit is bit with 100F load with 100F load voltage is bit is bit is bit is bit with 100F load With 100F load		
Home Uvrite Data Ox00 Write Register Reset Reconnect U58	Address bx0000 Read Data 0x00 Read Register Connected Connected Connected Consol Connected Consol Consol Connected Consol Consol Connected Consol Con	× ×	

Figure 4-1. ADC35xx Software Reset

Replace this image

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4.1 Bypass Mode

The following steps show how to configure the ADC3643EVM in Bypass mode.

4.1.1 ADC35XX GUI: Bypass Mode (DDR) Configuration

By default, the ADC3643EVM is preconfigured for 14bit, DDR mode. When using this mode, the only required step in the ADC35XX GUI is to configure the onboard clock in order to select the desired sampling rate (10MHz, 25 MHz or 65 MHz).

Note: The following steps also apply to the ADC3642EVM and ADC3644EVM. However, the on board clocking device limits the ADC3642EVM to 25 MHz and 10 MHz clock frequencies, and the ADC3644EVM is limited to 125 MHz and 65 MHz. If different sampling frequencies are required, please connect an external clock source.

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select "14 bit".
- Select "65M" for Fs (sample clock).
- Ensure that "CDC Enable" is green (enabled).
- Click "Configure CDC" button.
- Click "Configure" button.



Figure 4-2. ADC35xx GUI settings for Bypass Mode



4.1.2 HSDC Pro: Bypass Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK

🚺 High Speed Data Converte	r Pro v5.10							_	
File Instrument Options D	ata Capture Option	s Test Options Device GUI Option:	s Help						
TEXAS INSTRUMENTS	1. 1.	ADC			∎ Ļ⊲		DAC		
Select ADC Capture Test Selection	8 65535- 0 - 0	5000 10000 15000	20000 25000 300	00 35000 40	000 45000	50000	55000 60	000 65000	2 + 1 1 1 1 1 1 1 1 1 1
Single Tone	F	Channel 1/2	Blackman	(Channel1	1)	1/1 Aver	ages	RBW	61.9888 Hz
SNR 90.027 dBFs	10.0-								,⊕ +
SFDR 105.588 dBFs	0.0 - Spu	r 🔣 Select Board			×				1
THD 110.102 dBFs	-10.0-				_				Q
ENOB 14.655 Bits	20.0-	Select The Serial num	ber of the Device						
Fund1.238 dBFs	-20.0-		Control Neuropean						
Phase 0.999 Rad	-30.0-		TUPOSET TSW1400		^				
HD2 -111.72 dBFs	-40.0-		TI4BOJET-T3W1400						
HD3 -129.289 dBFs	-50.0-								
HD4 -123.6 dBFs									
HD5 -125.4/2 dBFs NSD/Hz -153.087 dBFs/H:	-60.0- 0								
dBFs Hz	-70.0-								
M1 -135.164 0.00E+(-80.0-				¥				
M2 0 -4.09E+ *	00.0		Select/Enter ID Addres	- Dort Number					
Auto Calculation of	-90.0-		Select/Enter IP Addres	s - Port Number	1				
Coherent Frequencies	-100.0-		05	~					
Analysis Window (samples)	-110.0-			~					
ADC Output Data Bata	-120.0-	ок	· · · · · · · · · · · · · · · · · · ·	Cancel					
4 0625M	100.0			•					
ADC Input Target Frequency	-130.0-								
1.00000000M	-140.0-								
	-150.0-								
	Ó	200k 400k	600k 800k	1M	1.2M	1.4M	1.6M	1.8M	2.03125M
				Frequency (Hz)					
									/
Firmy	vare Ver= ""		TSW1400 Board = " "	1		Int	terface Type = '		
Device info details		9/22/2020	3:40:36 PM Build - 10/	18/2019 NOT C	ONNECTED			TEXAS	INSTRUMENTS

Figure 4-3. HSDC Pro: Connect to TSW1400

· Click OK for the no firmware loaded prompt.

• Select "ADC3643_7W_14bit_DDR" to load firmware, and click Yes.





Figure 4-4. HSDC Pro ini file selection for Bypass Mode

- Enter 65M within the box that says "ADC Output Data Rate"
- Enter the input frequency of the input signal in the box that says "ADC Input Target Frequency" (5 MHz used in this example).



Press Capture



Figure 4-5. Bypass Mode Capture

• The analog input signal power may need to be adjusted to reach -1 dBFS.



4.2 Real Decimation Mode

The following software configuration steps will program the ADC364xEVM in Real Decimation mode.

4.2.1 ADC35XX GUI: Real Decimation Mode Configuration

After launching the ADC35xx GUI perform the following steps:

- Under Resolution, select 16 bit.
- Under DDC, Select Real.
- For Decimation Factor, select 16.
- For Fs(MHz), select 60M.
- Click Configure CDC
- Click Configure



Figure 4-6. ADC35xx GUI settings for Real Decimation Mode



4.2.2 HSDC Pro: Real Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- Launch HSDC Pro
- Select the TSW1400 and click OK
- · Click OK for the no firmware loaded prompt.
- Select "ADC3643_2W_14bit_CMOS" to load firmware, and click Yes.



Figure 4-7. Real Decimation HSDC Pro INI File

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Click on the cog next to "ADC Output Data Rate".

🚺 Additional De	—		\times
Enable? Remo	ember fo	or this s	ession
ADC Sampling Rate			
60M			
ADC Input Frequen	cy		
1M	(Fout	t = Fin -	+ NCO)
ADC 2nd Input Freq	uency		
0	(Fout	t = Fin -	+ NCO)
NCO			
0			
# NCO Bits		11 #1	100
0		Bits?	NCO
Decimation			
16			
	ОК		

Figure 4-8. Real Decimation Mode HSDC Pro Parameters



- In the new dialogue box, enter 60M in "ADC Sampling Rate"
- Enter 1M in "ADC Input Frequency"
- Enter 16 in "Decimation".
- · Click Ok.
- Click the Capture button



Figure 4-9. HSDC Pro Cog Wheel



4.3 Complex Decimation Mode

The following software configuration steps will program the ADC364xEVM in Complex Decimation mode (16x) with a 10 MHz analog input and 9.9 MHz NCO.

4.3.1 ADC35XX GUI: Complex Decimation Configuration

After launching the ADC35xxEVM GUI perform the following steps:

- Under Resolution, select 14 bit.
- Under DDC, Select Complex.
- For Decimation Factor, select 16.
- For Fs(MHz), select 60M.
- Under "FNCO A (MHz)", enter "9.9" in the field. This field will then calculate to the nearest valid NCO value, and will auto-calculate the correct register values in the field next to it.
- Click Configure CDC



Figure 4-10. ADC35xx GUI settings for Complex Decimation Mode



4.3.2 HSDC PRO: Complex Decimation Mode

After pressing "Configure" within the ADC35xx GUI perform the following steps to setup HSDC pro:

- · Launch HSDC Pro.
- Select the TSW1400 and click "OK".
- Click OK for the "no firmware loaded" prompt.
- Select "ADC3643_2W_14bit_CMOS_Complex" to load firmware, and click Yes.



Figure 4-11. Complex Decimation HSDC Pro INI file



Click on the cog next to "ADC Output Data Rate".

- In the new dialogue box, check the "Enable?" box.
- Under "ADC Sampling Rate", enter "60M"
- Under "ADC Input Frequency", enter "10M"
- Under "NCO", enter "9.9M"
- Under "Decimation", enter "16".
- Click "OK".

🚺 Additional De	_		×
Enable? Remen	nber for	this se	ession
ADC Sampling Rate			
60M			
ADC Input Frequency	_		
10M	(Fout :	= Fin +	NCO)
ADC 2nd Input Frequ	ency		
0	(Fout :	= Fin +	NCO)
NCO			
9.9M			
# NCO Bits	1	lse # N	ICO
0		Bits?	
Decimation			
16			
	_		
 	Ж		

Figure 4-12. Complex Decimation Mode HSDC Pro Parameters

Select "Complex FFT"



· Press "Capture"



Figure 4-13. Complex Mode Capture

5 External Clocking Hardware Setup

The onboard CDC is useful for general evaluation and relieves the user requirment of needing additional signal generators. The following section shows how to configure and program the ADC364xEVM for external clock operation for Real Decimation Mode. This mode requires two external clock sources (must be frequency locked). If Bypass Mode or Complex Decimation Mode are to be used with an external clock source(s), use the steps outlined with the onboard clock for Bypass Mode and Complex Decimation mode for guidance on how the ADC35xx GUI should be configured (with the exception of using external clocks).

5.1 Hardware Modfications

The following hardware modifications must be made in order to operate the ADC364xEVM using an external sample and (if required) data clock .

External Sample Clock Modification:



- DNI R32, R40
- Install R36, R37 (0-Ω resistor)
- Connect sample clock to J8. Connect DCLKIN to J15.



Figure 5-1. ADC364xEVM Schematic Snippet: Sample Clock

External DCLKIN Modification:

• DNI R176



External Clocking Hardware Setup

• Replace C129 with 0-Ω resistor.



Figure 5-2. ADC364xEVM Schematic Snippet: DCKLIN



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5.2 Hardware Setup: Real Decimation 16x Mode

- Connect ADC sampling clock source (SMA100A used) to J8. Set signal power to +15 dBm. 65 MSPS used in this example.
- Connect DCLKIN clock source (SMA100A used) to J10. Set signal power to +13 dBm. 14.21875 MHz used in this example

ADC sampling clock source and DCLKIN source must be frequency locked. If this is not performed, the captured data will appear scrambled.

• If not already done, complete the remaining steps outlined in the section Setup Procedure.

5.3 External Clock: ADC35XX GUI Real Decimation Mode

To program the ADC364xEVM follow the steps written in the previous section titled "ADC35xx GUI: Real Decimation Configuration". The only difference that must be observed in the GUI is "CDC Clock Enable" button must be disabled (red) before selecting "Configure" in the ADC35xx GUI.

utput Info			
Device Variant	Resolution		
ADC3643 V	14 bit	\sim	
Mode	DDC		
2 Wire 🗸	Real	~	
Decimation Factor 16			

Figure 5-3. ADC35XX GUI: Disable CDC Clock Enable

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6 ADC364xEVM Power Monitor

The ADC364xEVM is equipped with on-board current shunt monitors that are able to measure the current consumption on the +1.8VD C rails (AVDD and IOVDD). The user has the ability to read the ADC364xEVM's power consumption on the front page of the ADC35XX GUI. Click the "Measure Power" button to refresh the current values. This feature is useful for determining what mode/sampling speed offers the best power consumption for your application needs.



Figure 6-1. ADC364xEVM Power Meter

7 Test Pattern

It is often useful to utilize test patterns to help verify the correct reciept of digital data at the microcontroller or FPGA. A ramp pattern can be enabled by following these steps:

- Click the yellow button "Analog Inputs and Clk"
- Next to "Test Pattern CHA", click the drop down menu, and select "RAMP CUSTOM". This can be done for "Test Pattern CHB" as well.
- In the field next to "Custom Pattern", enter the number "16".
- The digital ramp pattern is now enabled on the ADC. The output of the ADC is now a 14 bit, incrementing ramp pattern.



Figure 7-1. ADC35XXEVM GUI 1.0 Ramp Pattern



 In HSDC Pro, the ramp pattern can now be seen when data is captured. These same steps apply to any data output mode (Bypass, Real Decimation and Complex Decimation).



Figure 7-2. HSDC Pro Digital Ramp Pattern

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3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

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This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.
- 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

- 1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
- 2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
- 3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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- 3.3.3 Notice for EVMs for Power Line Communication: Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page 電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page
- 3.4 European Union
 - 3.4.1 For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 EVM Use Restrictions and Warnings:

- 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
- 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
- 4.3 Safety-Related Warnings and Restrictions:
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and inability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
- 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
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