

## ADF7030-1 Hardware Reference Manual

### SCOPE

This reference manual provides a description of the [ADF7030-1](#) radio functionality, hardware features, and application circuit requirements. It is intended as a resource for a hardware engineer designing a printed circuit board (PCB) that includes the [ADF7030-1](#).

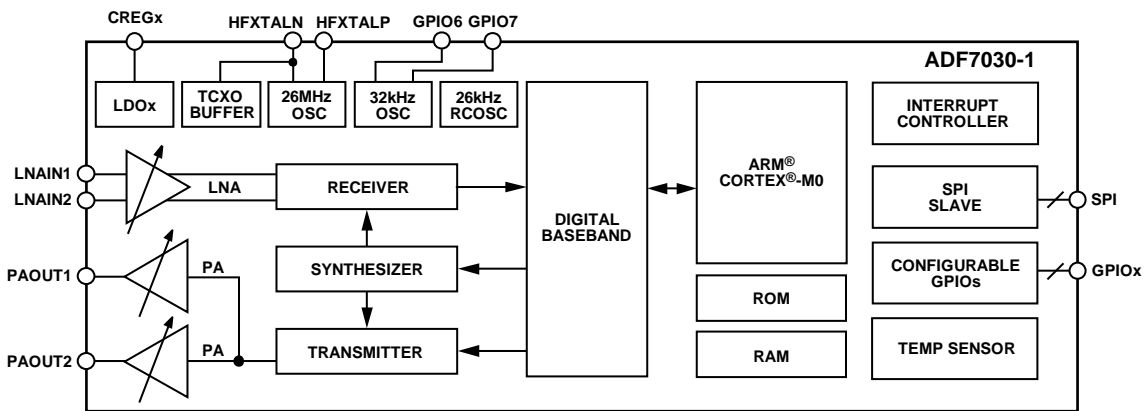
### ABOUT THE [ADF7030-1](#)

The [ADF7030-1](#) is a low power, high performance, fully integrated radio transceiver that supports a wide range of modulation scheme and channel widths in the sub GHz frequency range.

The [ADF7030-1](#) features an on-chip ARM® Cortex®-M0 processor that performs radio control and radio packet management.

### OTHER RELEVANT DOCUMENTATION

Complete specifications for the [ADF7030-1](#) device can be found in the [ADF7030-1](#) data sheet. The [ADF7030-1](#) software reference manual is the programming guide for the [ADF7030-1](#) and is available from Analog Devices, Inc. Both the [ADF7030-1](#) data sheet and software reference manual documents should be consulted in conjunction with this hardware reference manual.



NOTES  
1. CREGx, GPIOx, AND SPI CONTAIN MULTIPLE PINS.

Figure 1. Functional Block Diagram

14385-001

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**REVISION HISTORY**

**7/2020—Rev. A to Rev. B**

|   |    |
|---|----|
| Changes to Table 2 .....  | 3  |
| Changes to Table 3 .....  | 4  |
| Changes to Application Circuit Diagrams Section .....   | 7  |
| Added Figure 7; Renumbered Sequentially .....   | 9  |
| Changes to Table 6 and Table 7 .....  | 10 |
| Changes to Table 8 and Table 9 .....  | 11 |
| Changes to Table 10 and Table 11 .....  | 12 |
| Added Combined Matching Network Section, Figure 12, and Table 12; Renumbered Sequentially ..... | 12 |

**9/2017—Rev. 0 to Rev. A**

|  |    |
|--|----|
| Changes to Crystal Reference Section .....   | 5  |
| Changes to Application Circuit Diagrams Section .....                                    | 7  |
| Changes to PA1 Separate Matching Network Section, Figure 7, Figure 8, and Figure 9 ..... | 10 |
| Changes to Table 10 and Table 11 .....   | 13 |

**6/2016—Revision 0: Initial Version**

## GETTING STARTED

### EVALUATION AND DEVELOPMENT PLATFORM

The [ADF7030-1 EZ-KIT](#) is an evaluation and development systems for the [ADF7030-1](#) high performance, sub GHz radio transceiver IC.

The [ADF7030-1 EZ-KIT](#) allows fast and thorough evaluation of the [ADF7030-1](#) and provides a platform for host processor code development.

There are four models of the [ADF7030-1 EZ-KIT](#) available as described in Table 1, each covering one of the main industrial, scientific and medical (ISM) bands at 169 MHz, 433 MHz, 868 MHz, or 915 MHz.

**Table 1. ADF7030-1 EZ-KIT Kit Models**

| Model                             | Frequency (MHz) |
|-----------------------------------|-----------------|
| <a href="#">ADF70301-915EZKIT</a> | 902 to 928      |
| <a href="#">ADF70301-868EZKIT</a> | 863 to 876      |
| <a href="#">ADF70301-433EZKIT</a> | 433 to 434      |
| <a href="#">ADF70301-169EZKIT</a> | 169             |

The [ADF7030-1 EZ-KIT](#) kit models in Table 1 include RF daughter boards. Additional daughter boards covering different frequency ranges (for example, 450 MHz to 470 MHz) or with different matching topologies can be ordered individually and used with the [ADF7030-1 EZ-KIT](#) as described in Table 2.

**Table 2. ADF7030-1 Daughter Boards**

| Board Name                        | Match    | Frequency (MHz) | Reference Populated | Reference Connected | PA Connected |
|-----------------------------------|----------|-----------------|---------------------|---------------------|--------------|
| <a href="#">EV-ADF70301-915AZ</a> | Separate | 915             | XTAL                | XTAL                | Both         |
| <a href="#">EV-ADF70301-915CZ</a> | Combined | 915             | XTAL                | XTAL                | PA1          |
| <a href="#">EV-ADF70301-915DZ</a> | Combined | 915             | TCXO                | TCXO                | PA1          |
| <a href="#">EV-ADF70301-915EZ</a> | Combined | 915             | XTAL                | XTAL                | PA2          |
| <a href="#">EV-ADF70301-868BZ</a> | Separate | 868             | TCXO                | TCXO                | Both         |
| <a href="#">EV-ADF70301-868EZ</a> | Combined | 868             | XTAL                | XTAL                | PA2          |
| <a href="#">EV-ADF70301-460BZ</a> | Separate | 460             | TCXO                | TCXO                | Both         |
| <a href="#">EV-ADF70301-433AZ</a> | Separate | 433             | XTAL                | XTAL                | Both         |
| <a href="#">EV-ADF70301-433CZ</a> | Combined | 433             | XTAL                | XTAL                | PA1          |
| <a href="#">EV-ADF70301-169BZ</a> | Separate | 169             | TCXO                | TCXO                | Both         |

## ADF7030-1 PIN DESCRIPTIONS

### PIN FUNCTIONS

For all pins, do not exceed the absolute maximum ratings specified in the [ADF7030-1](#) data sheet.

#### Hardware Reset Pin

When the hardware reset pin ( $\overline{\text{RST}}$ ) is pulled low by a host microprocessor, the [ADF7030-1](#) undergoes a hardware reset. Timing requirements for this pull-down duration are given in the [ADF7030-1](#) data sheet.

To prevent unintended resets, a 100 k $\Omega$  pull-up resistor is recommended on the  $\overline{\text{RST}}$  pin. Refer to the digital input/output specifications in the [ADF7030-1](#) data sheet for information on logic level requirements.

#### SPI Interface

The serial peripheral interface (SPI) of the [ADF7030-1](#) consists of the  $\overline{\text{CS}}$ , SCLK, MISO, and MOSI pins. The [ADF7030-1](#) acts as an SPI slave to an external host microprocessor. If the device is in the PHY\_SLEEP state, pulling the  $\overline{\text{CS}}$  pin to change low wakes the [ADF7030-1](#). To prevent unintentional wake up of the [ADF7030-1](#), a 100 k $\Omega$  pull-up resistor is recommended on the  $\overline{\text{CS}}$  pin.

Refer to the digital input/output specifications in the [ADF7030-1](#) data sheet for information on logic level and timing requirements.

#### Regulator Stability Capacitors

A 220 nF capacitor connected to ground is required at each of the CREG1, CREG2, CREG3, CREG4, CREG5, CREG6, and CREG7 pins of the [ADF7030-1](#). Place each 220 nF capacitor as close to the pin as possible to ensure regulator stability and noise rejection.

In addition to the 220 nF capacitor, a second capacitor to ground is recommended at the CREG3 pin. The second capacitor reduces the amplitude of the power amplifier (PA) harmonics transmitted to the device. Place this second decoupling capacitor between the 220 nF regulator capacitor and the CREG3 pin, as close to the pin as possible. Recommended values for this second decoupling capacitor are listed in Table 3.

**Table 3. Recommended Capacitor Values at the CREG3 Pin for Harmonic Suppression**

| Frequency (MHz) | Value (pF) |
|-----------------|------------|
| 915             | 6.8        |
| 868             | 18         |
| 460             | 47         |
| 433             | 68         |
| 169             | 220        |

#### Voltage Supply Pins and Decoupling Capacitors

The [ADF7030-1](#) requires a supply voltage between 2.2 V and 3.6 V. However, the maximum transmit output power achievable is dependent on the programmable regulator voltage at the CREG3 pin, which supplies a voltage to the PA choke inductor.

As a result, the minimum supply voltage requirement increases with increased transmit power, as detailed in Table 4. Output powers in excess of 13 dBm apply to only Power Amplifier 2 (PA2).

The [ADF7030-1](#) software reference manual describes selecting the desired PA, programming the PA output level, and setting the CREG3 voltage.

**Table 4. Required Supply Voltage vs. Transmit Power Level**

| Tx Power Level (dBm) | Programmable Voltage atCREG3 (V) | Minimum Supply Voltage Required (V) |
|----------------------|----------------------------------|-------------------------------------|
| $\geq 17$            | 2.65                             | 2.85                                |
| 16                   | 2.4                              | 2.6                                 |
| 15                   | 2.2                              | 2.4                                 |
| 14                   | 2.0                              | 2.2                                 |
| 13                   | 1.85                             | 2.2                                 |
| <13                  | 1.85                             | 2.2                                 |

Place a 100 nF decoupling capacitor as close as possible to each of the six voltage supply pins of the [ADF7030-1](#) (VBAT1, VBAT2, VBAT3, VBAT4, VBAT5, and VBAT6). VBAT1 and VBAT6 can be tied together, as well as VBAT4 and VBAT5, and use a single decoupling capacitor for both sets of pins.

#### Off Chip Loop Filter Capacitor

The off chip loop filter capacitor (CLF) integrates the current pulses from the charge pump of the [ADF7030-1](#) to form a voltage that tunes the output of the voltage controlled oscillator (VCO) to the desired frequency. The off chip loop filter capacitor also attenuates spurious levels generated by the phase-locked loop (PLL). The loop filter bandwidth is set automatically by the [ADF7030-1](#) according to the programmed data rate. This loop filter is fully integrated except for an external 1.2 nF capacitor that must be connected between the CLF pin and CREG1 pin.

#### Exposed Pad (40-Lead LFCSP Version Only)

The [ADF7030-1](#) ground is provided through the exposed pad (EPAD). The EPAD must be soldered to the PCB ground. Use multiple vias from the EPAD, to which the pad is soldered, to the ground plane to minimize return path impedance for radio frequency (RF) signals and noise.

#### Ground Pins (48-Lead LQFP Version Only)

The ground pins (GND) must connect to a common ground plane. Take care to minimize return path impedance for RF signals and noise.

#### PA and Low Noise Amplifier (LNA) Connections

See the RF Matching Networks section for details about the LNAINx and PAOUTx pins.

**General-Purpose Input/Output (GPIO) Pins**

The ADF7030-1 has eight GPIOx pins. These pins are highly configurable and can provide the following functions:

- Control signals to external switches, PAs, and LNAs.
- Interrupts from the ADF7030-1 to a host microprocessor.
- Interrupts from a host microprocessor to the ADF7030-1.
- Streaming data test modes as described in the Test Mode Connections section and detailed in the ADF7030-1 software reference manual.

Unless otherwise configured by the user or following a reset condition, the default GPIOx pin configuration is as shown in Table 5.

**Table 5. Default GPIOx Pin Configuration Functions**

| GPIOx Pin | Default Function                     |
|-----------|--------------------------------------|
| GPIO0     | Reserved                             |
| GPIO1     | Reserved                             |
| GPIO2     | Interrupt input                      |
| GPIO3     | Interrupt output                     |
| GPIO4     | Interrupt input                      |
| GPIO5     | Interrupt output                     |
| GPIO6     | External low frequency crystal input |
| GPIO7     | External low frequency crystal input |

If the user configures GPIOx pins as input interrupts to the ADF7030-1, 100 kΩ pull-down resistors are recommended on those pins to prevent unwanted interrupts to the ADF7030-1.

The configuration of the GPIOx pins (either the default configuration or that set by the user) is maintained following a transition to PHY\_SLEEP state. Refer to the ADF7030-1 for possible GPIOx configurations that the user can set.

For information on GPIOx logic levels, refer to the ADF7030-1 data sheet.

**FREQUENCY REFERENCES**

Use either a standard crystal oscillator or a temperature compensated crystal oscillator (TCXO) as the main frequency reference for the ADF7030-1. Generally a TCXO is used for applications that demand high RF frequency accuracy, such as narrow-band systems where the RF channel width is less than 25 kHz.

The ADF7030-1 features real time clock (RTC) functionality for autonomous radio operation. Use either an internal 26 kHz low power RC oscillator or an external 32.768 kHz oscillator can be used as the clock source for this RTC. The external 32.768 kHz oscillator provides greater wake-up time accuracy while the internal 26 kHz RC oscillator has lower power consumption.

**TCXO Reference**

The ADF7030-1 requires a TCXO input of 26 MHz. DC couple the TCXO to the HFXTALN pin of the ADF7030-1. Leave the HFXTALP pin unconnected. The TCXO signal is 26 MHz with a clipped sine wave output. Refer to the ADF7030-1 data sheet for the voltage level requirements of the frequency reference.

**Crystal Reference**

If using a crystal to provide the high frequency reference, it must have a frequency of 26 MHz and be connected between the HFXTALP and HFXTALN pins of the ADF7030-1. The crystal must operate in parallel mode and two parallel loading capacitors are required for oscillation at the correct frequency. The values of the capacitors are dependent upon the crystal specification. In the ADF7030-1 reference design, C1 = 11 pF and C2 = 11 pF for a 12 pF load crystal (see Figure 2). Note that only 12 pF load crystals are supported.

Choose load capacitors that ensure the shunt capacitance value added to the PCB track capacitance and the input pin capacitance of the ADF7030-1 equal the specified load capacitance of the crystal (see Equation 1). Track capacitance values typically vary from 2 pF to 5 pF, depending on board layout. Ensure the lengths of the PCB traces from the crystal to the HFXTALP and HFXTALN pins are as close to equal as possible to minimize the PCB capacitance. Also, keep the distance between the HFXTALP PCB trace and the HFXTALN PCB trace as large as possible to reduce the capacitive coupling between the HFXTALP and HFXTALN pins.

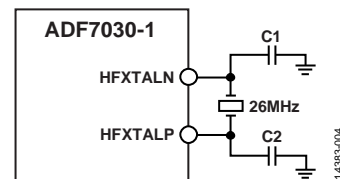


Figure 2. 26 MHz Crystal Reference Connections

The total load capacitance is described by Equation 1.

$$C_{LOAD} = \frac{1}{\frac{1}{C1} + \frac{1}{C2}} + C_{PIN} + C_{PCB} \tag{1}$$

where:

$C_{LOAD}$  is the total load capacitance

$C1$  is the external crystal load capacitor connected to the HFXTALN pin.

$C2$  is the external crystal load capacitor connected to the HFXTALP pin.

$C_{PIN}$  is the capacitance between the HFXTALN and HFXTALP pins (refer to the ADF7030-1 data sheet).

$C_{PCB}$  is the PCB track capacitance and capacitive coupling between the HFXTALN and HFXTALP traces.

To ensure stable frequency operation over all conditions, choose capacitors that have a very low temperature coefficient.

**32.768 kHz Wake-Up Crystal (Optional)**

If a greater wake-up accuracy is needed than the accuracy provided by the internal 26 kHz oscillator, the user can connect an external 32.768 kHz crystal oscillator between the GPIO6 and GPIO7 pins.

The crystal oscillator must be operated in parallel mode; two parallel loading capacitors are required for oscillation at the correct frequency. The values of the capacitors are dependent upon the crystal specification. The capacitors must be chosen to ensure the shunt value of capacitance added to the PCB track capacitance and the input pin capacitance of the [ADF7030-1](#) equals the specified load capacitance of the crystal. Track capacitance values typically vary from 2 pF to 5 pF, depending on board layout. Ensure the lengths of the PCB traces from the crystal to the pins are as close to equal as possible.

The total load capacitance can be calculated using the following equation:

$$C_{LOAD} = \frac{1}{\frac{1}{C1} + \frac{1}{C2}} + \frac{C_{PIN}}{2} + C_{PCB} \quad (2)$$

where:

$C_{LOAD}$  is the total load capacitance.

$C1$  and  $C2$  are the external crystal load capacitors.

$C_{PIN}$  is the [ADF7030-1](#) input capacitance of the GPIO6 and GPIO7 pins (refer to the [ADF7030-1](#) data sheet).

$C_{PCB}$  is the PCB track capacitance.

To ensure stable frequency operation over all conditions, choose capacitors that have a very low temperature coefficient.

## APPLICATION CIRCUIT DIAGRAMS

This section details some of the application circuits that are possible with the [ADF7030-1](#). The presence of two transmit power amplifiers allows flexibility in the choice of the impedance matching networks, as appropriate for a given application.

For example, if the desired transmit is at <13 dBm, Power Amplifier 1 (PA1) is the most efficient choice. As described in the RF Matching Networks section, the topology of the PA matching networks at 169 MHz differs from those at other frequencies (see Figure 5).

For applications where a single antenna connection is required, it is recommended to use an external switch, as shown in Figure 4. The GPIO pins of the [ADF7030-1](#) can be configured to automatically control external circuitry, such as switches and amplifiers. The matching network of the PA and LNA can also be combined as shown in Figure 7. The combined RF matching network is suboptimal, and there is performance loss in both transmission and reception.

Note that Figure 3 to Figure 6 are diagrams of the 40-lead LFCSP package but are transferable to the 48-lead LQFP package.

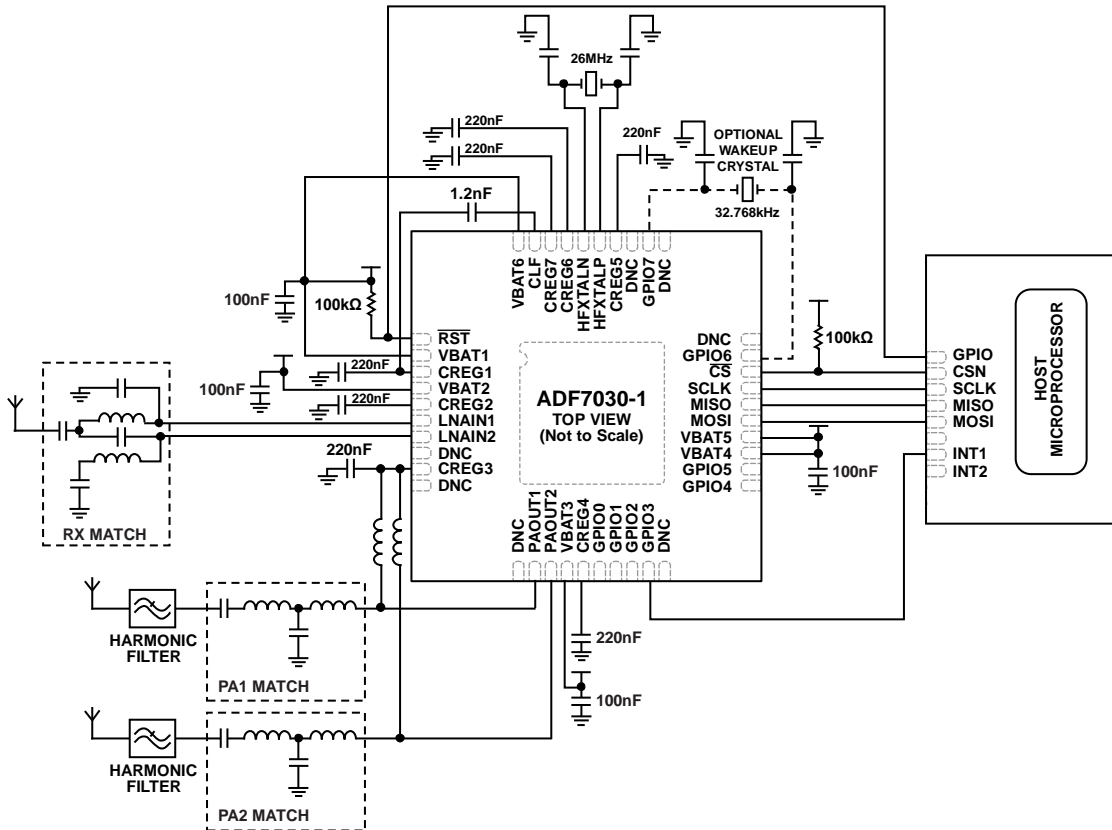


Figure 3. Application Circuit with Both PAs and LNA Matched and a Crystal Reference

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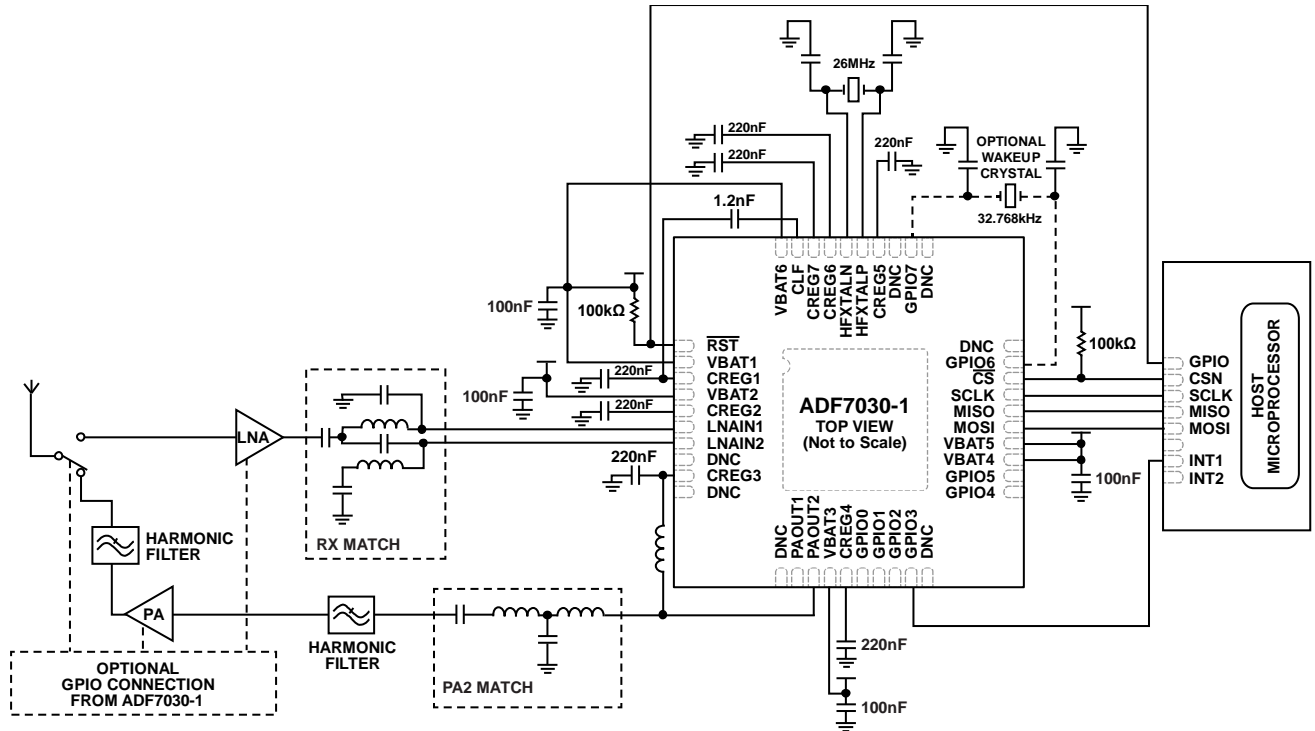


Figure 6. Application Circuit with External PA, External LNA, and a Crystal Reference

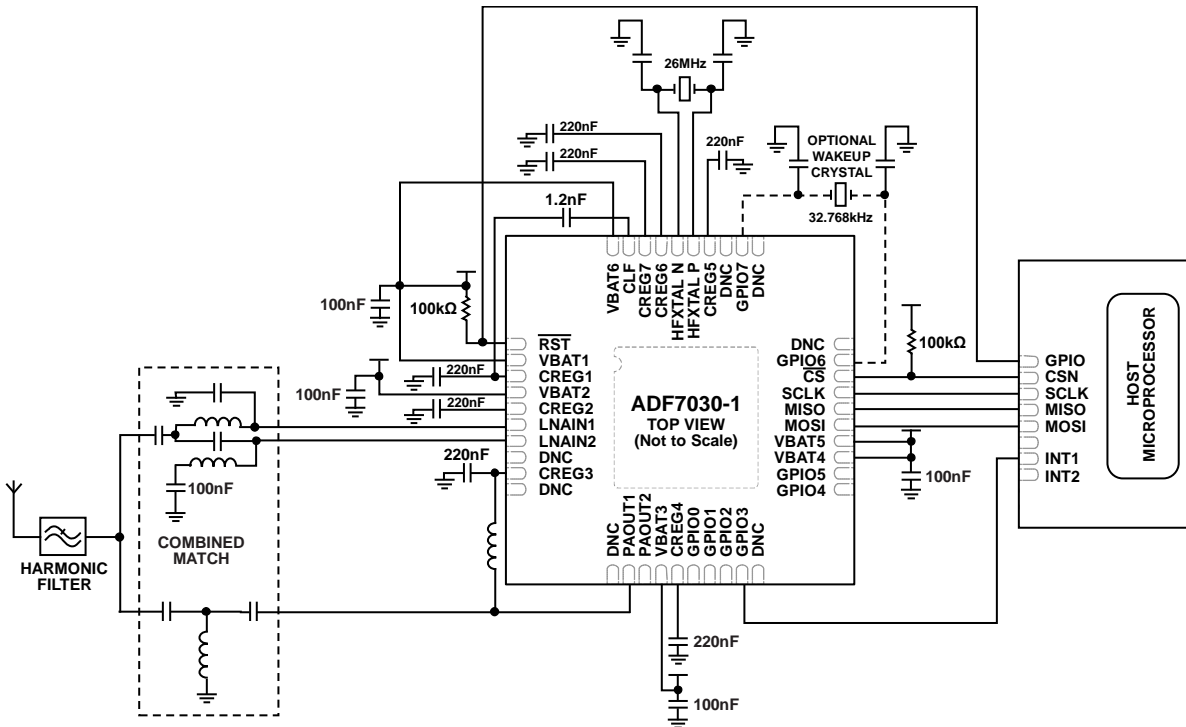


Figure 7. Application Circuit with Combined PA1 and LNA Matched and a Crystal Reference

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## RF MATCHING NETWORKS

The purpose of the matching networks is to maximize power transfer from the relevant PA to the antenna, from the antenna to the LNA, and to minimize reflections due to impedance mismatch. With separate matches, each PA or LNA has an individual matching network to a switch or antenna.

### PA1 SEPARATE MATCHING NETWORK

A shunt capacitor and two series inductors match consisting of L14, L6, and C21 is used for all PA1 matching networks. Additionally, when operating at 169 MHz, a harmonic termination circuit consisting of L16, C41, and R7 is required. The other components, L11 and C20, are a choke inductor and a dc blocking capacitor, respectively.

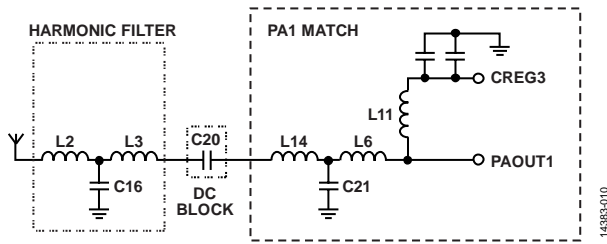


Figure 8. 862 MHz to 928 MHz Harmonic Filter and Matching Network for PA1

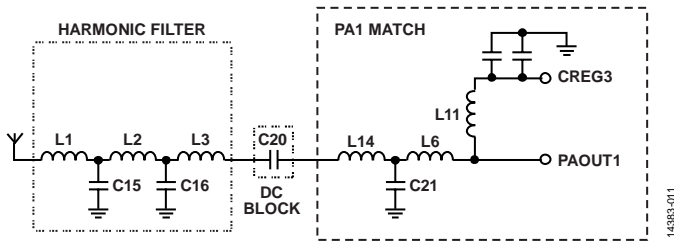


Figure 9. 433 MHz to 470 MHz Harmonic Filter and Matching Network for PA1

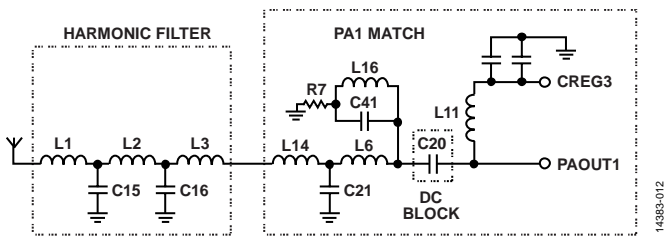


Figure 10. 169 MHz Harmonic Filter and Matching Network for PA1

The PA is matched to 50 Ω and the input and output impedances of the harmonic filter are also 50 Ω. Table 6 (LFCSP) and Table 7 (LQFP) list the matching components for PA1.

Table 6. PA1 Matching Components for 40-Lead LFCSP Variant

| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C15       | 27 pF            | 6.8 pF                        | Not applicable                |
| C16       | 27 pF            | 6.8 pF                        | 2.7 pF                        |
| C20       | 100 nF           | 270 pF                        | 56 pF                         |
| C21       | 15 pF            | 6.8 pF                        | 2.7 pF                        |
| C41       | 33 pF            | Not applicable                | Not applicable                |
| L1        | 12 nH            | 19 nH                         | Not applicable                |
| L2        | 47 nH            | 33 nH                         | 11 nH                         |
| L3        | 12 nH            | 19 nH                         | 11 nH                         |
| L6        | 82 nH            | 23 nH                         | 13 nH                         |
| L11       | 470 nH           | 82 nH                         | 40 nH                         |
| L14       | 82 nH            | 19 nH                         | 13 nH                         |
| L16       | 27 nH            | Not applicable                | Not applicable                |
| R7        | 50 Ω             | Not applicable                | Not applicable                |

Table 7. PA1 Matching Components for 48-Lead LQFP Variant

| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C15       | 27 pF            | 6.8 pF                        | Not applicable                |
| C16       | 27 pF            | 6.8 pF                        | 2.7 pF                        |
| C20       | 100 nF           | 270 pF                        | 56 pF                         |
| C21       | 15 pF            | 6.8 pF                        | 3.3 pF                        |
| C41       | 33 pF            | Not applicable                | Not applicable                |
| L1        | 12 nH            | 19 nH                         | Not applicable                |
| L2        | 47 nH            | 33 nH                         | 11 nH                         |
| L3        | 12 nH            | 19 nH                         | 11 nH                         |
| L6        | 82 nH            | 23 nH                         | 11 nH                         |
| L11       | 470 nH           | 82 nH                         | 40 nH                         |
| L14       | 82 nH            | 19 nH                         | 9 nH                          |
| L16       | 27 nH            | Not applicable                | Not applicable                |
| R7        | 50 Ω             | Not applicable                | Not applicable                |

**PA2 SEPARATE MATCHING NETWORK**

A shunt capacitor and two series inductors match consisting of the L10 and L13 inductors and C25 capacitor is used for all PA matching networks. Additionally, when operating at 169 MHz, a harmonic termination circuit consisting of L15, C40, and R8 resistor is required.

The other components, L12 and C24, are a choke inductor and a dc blocking capacitor, respectively. The PA is matched to 50 Ω and the input and output impedances of the harmonic filter are also 50 Ω.

Table 8 (40-lead LFCSP) and Table 9 (48-lead LQFP) list the matching components for PA2.

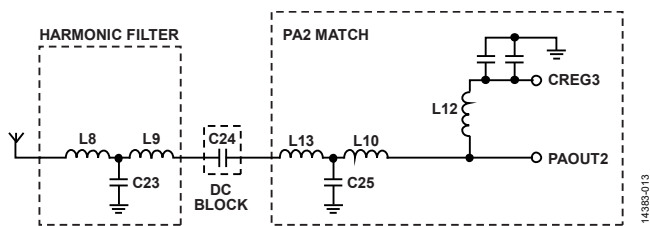


Figure 8. 862 MHz to 928 MHz Harmonic Filter and Matching Network for PA2

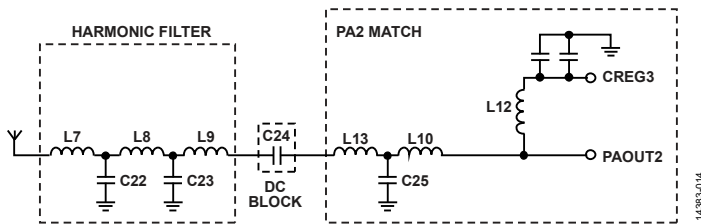


Figure 9. 433 MHz to 470 MHz Harmonic Filter and Matching Network for PA2

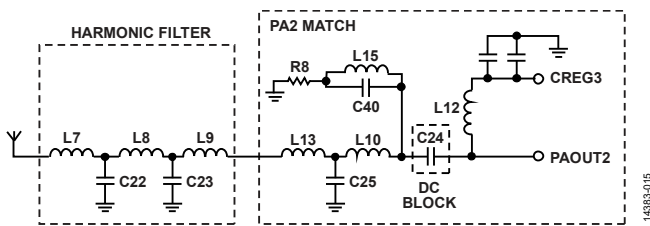


Figure 10. Harmonic Filter and Matching Network for PA2

**Table 8. PA2 Matching Components for 40-Lead LFCSP Variant**

| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C22       | 18 pF            | 6.8 pF                        | Not applicable                |
| C23       | 18 pF            | 6.8 pF                        | 2.7 pF                        |
| C24       | 100 nF           | 270 pF                        | 56 pF                         |
| C25       | 18 pF            | 6.8 pF                        | 3.3 pF                        |
| C40       | 33 pF            | Not applicable                | Not applicable                |
| L7        | 43 nH            | 20 nH                         | Not applicable                |
| L8        | 82 nH            | 40 nH                         | 11 nH                         |
| L9        | 43 nH            | 20 nH                         | 11 nH                         |
| L10       | 56 nH            | 18 nH                         | 9 nH                          |
| L12       | 470 nH           | 82 nH                         | 40 nH                         |
| L13       | 68 nH            | 11 nH                         | 8.2 nH                        |
| L15       | 27 nH            | Not applicable                | Not applicable                |
| R8        | 38 Ω             | Not applicable                | Not applicable                |

**Table 9. PA2 Matching Components for 48-Lead LQFP Variant**

| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C22       | 18 pF            | 6.8 pF                        | Not applicable                |
| C23       | 18 pF            | 6.8 pF                        | 2.7 pF                        |
| C24       | 100 nF           | 270 pF                        | 56 pF                         |
| C25       | 18 pF            | 8.2 pF                        | 3.9 pF                        |
| C40       | 33 pF            | Not applicable                | Not applicable                |
| L7        | 43 nH            | 20 nH                         | Not applicable                |
| L8        | 82 nH            | 40 nH                         | 11 nH                         |
| L9        | 43 nH            | 20 nH                         | 11 nH                         |
| L10       | 56 nH            | 19 nH                         | 7.5 nH                        |
| L12       | 470 nH           | 82 nH                         | 40 nH                         |
| L13       | 68 nH            | 11 nH                         | 5.6 nH                        |
| L15       | 27 nH            | Not applicable                | Not applicable                |
| R8        | 38 Ω             | Not applicable                | Not applicable                |

**LNA SEPARATE MATCHING NETWORK**

The LNA matching circuit performs both a differential to single-ended conversion and an impedance transformation to 50 Ω. The matching components consist of Inductors L4 and L5 and Capacitors C18 and C19.

Use Capacitors C17 and C14 to block dc levels. See Table 10 and Table 11 for more information on the matching LNA components.

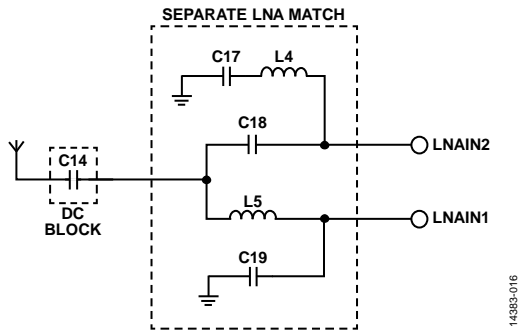


Figure 11. Matching Network for the LNA

Table 10. LNA Matching Components for 40-Lead LFCSP Variant

| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C14       | 2.2 nF           | 270 pF                        | 56 pF                         |
| C17       | 2.2 nF           | 270 pF                        | 56 pF                         |
| C18       | 12 pF            | 4.7 pF                        | 2.7 pF                        |
| C19       | 12 pF            | 2.7 pF                        | 1 pF                          |
| L4        | 56 nH            | 13 nH                         | 5.1 nH                        |
| L5        | 56 nH            | 19 nH                         | 8.7 nH                        |

Table 11. LNA Matching Components for 48-Lead LQFP Variant

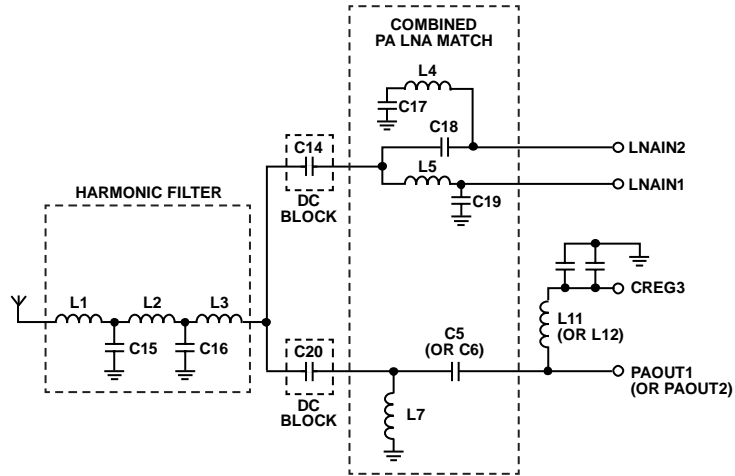
| Component | Value at 169 MHz | Value from 426 MHz to 470 MHz | Value from 863 MHz to 960 MHz |
|-----------|------------------|-------------------------------|-------------------------------|
| C14       | 2.2 nF           | 270 pF                        | 56 pF                         |
| C17       | 2.2 nF           | 270 pF                        | 56 pF                         |
| C18       | 12 pF            | 4.7 pF                        | 2.7 pF                        |
| C19       | 12 pF            | 2.7 pF                        | 1.2 pF                        |
| L4        | 56 nH            | 13 nH                         | 5.1 nH                        |
| L5        | 56 nH            | 18 nH                         | 7.5 nH                        |

**COMBINED MATCHING NETWORK**

Although suboptimal, the combined matching circuit allows the PA and LNA to share a single antenna. The LNA matching circuit is similar to the separate LNA match. The PA matching circuit is composed of a series capacitor and a shunt inductor. A harmonic filter is placed between the antenna and the combined matching. Only the matching components for the 40-lead LFCSP are shown in Table 12.

Table 12. LNA Matching Components for 40-Lead LFCSP Variant

| Component | Value at 433 MHz with PA1 Connected | Value at 868 MHz with PA2 Connected | Value at 915 MHz with PA1 Connected | Value at 915 MHz with PA2 Connected |
|-----------|-------------------------------------|-------------------------------------|-------------------------------------|-------------------------------------|
| C5        | 270 pF                              | Do not install                      | 56 pF                               | Do not install                      |
| C6        | Do not install                      | 56 pF                               | Do not install                      | 56 pF                               |
| C14       | 12 pF                               | 10 pF                               | 6.8 pF                              | 10 pF                               |
| C15       | 6.8 pF                              | 2.7 pF                              | 2.7 pF                              | 2.7 pF                              |
| C16       | 6.8 pF                              | 2.7 pF                              | 2.7 pF                              | 2.7 pF                              |
| C17       | 270 pF                              | 56 pF                               | 56 pF                               | 56 pF                               |
| C18       | 4.7 pF                              | 1.8 pF                              | 1.5 pF                              | 1.5 pF                              |
| C19       | 1.5 pF                              | 1.8 pF                              | 1.8 pF                              | 1.5 pF                              |
| C20       | 12 pF                               | 3.3 pF                              | 3.3 pF                              | 3.3 pF                              |
| L1        | 19 nH                               | 11 nH                               | 11 nH                               | 11 nH                               |
| L2        | 33 nH                               | 22 nH                               | 22 nH                               | 22 nH                               |
| L3        | 24 nH                               | 18 nH                               | 16 nH                               | 18 nH                               |
| L4        | 11 nH                               | 9 nH                                | 10 nH                               | 9 nH                                |
| L5        | 20 nH                               | 12 nH                               | 12 nH                               | 12 nH                               |
| L7        | 39 nH                               | 11 nH                               | 15 nH                               | 11 nH                               |
| L11       | 82 nH                               | Do not install                      | 40 nH                               | Do not install                      |
| L12       | Do not install                      | 40 nH                               | Do not install                      | 40 nH                               |



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Figure 12. Combined Matching Network

## BILL OF MATERIALS COUNT

The [ADF7030-1](#) bill of materials count for a typical application circuit is detailed in Table 13. For a complete bill of materials, see the design package available on the [ADF7030-1](#) product page.

## REFERENCE DESIGN

The [ADF7030-1](#) reference design schematic, layout files, and bill of materials are included in the [ADF7030-1](#) design package.

**Table 13. Typical Bill of Materials Count for 915 MHz Separate Matching Network Reference Design**

| Application Circuit Element                  | No. of Capacitors | No. of Inductors | No. of Resistors | No. of Crystals/TCXOs |
|--|-------------------|------------------|------------------|-----------------------|
| Separate PA Matching Network (PA1 or PA2)    | 2                 | 3                | 0                | 0                     |
| Harmonic Filter                              | 1                 | 2                | 0                | 0                     |
| Separate LNA Matching Network                | 4                 | 2                | 0                | 0                     |
| Decoupling Capacitors                        | 4                 | 0                | 0                | 0                     |
| Regulator Capacitors                         | 8                 | 0                | 0                | 0                     |
| CS Pull-Up Resistor                          | 0                 | 0                | 1                | 0                     |
| RST Pull-Up Resistor                         | 0                 | 0                | 1                | 0                     |
| CLF Capacitor                                | 1                 | 0                | 0                | 0                     |
| 26 MHz Reference Crystal and Load Capacitors | 2                 | 0                | 0                | 1                     |
| Total Component Count by Component Type      | 22                | 7                | 2                | 1                     |

**LAYOUT AND STACK UP**

The ADF7030-1 reference design uses a 4-layer stack up, the minimum number of layers recommended for ADF7030-1 designs. Employ ground stitching at least every tenth of a wavelength of the fundamental operating frequency across the board and around the edges. When using the LFCSP variant, solder the EPAD of the ADF7030-1 to ground. Use multiple vias from the PCB pad, to which the EPAD is soldered, to the ground plane to minimize return path impedance for RF signals and noise (see Figure 13).

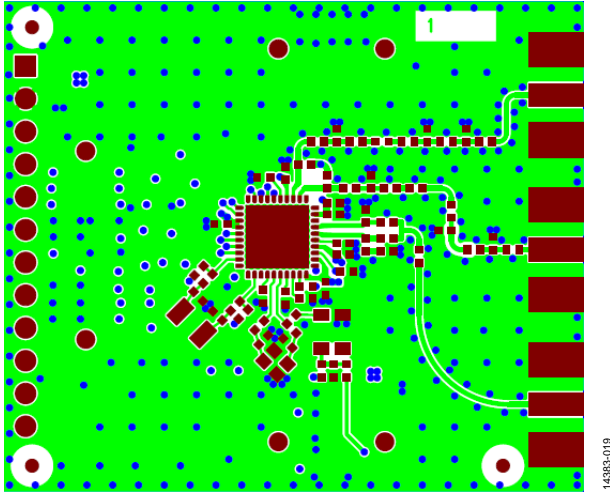


Figure 13. Layer 1, Signal Layer

A solid ground plane is recommend on Layer 2 (see Figure 14).

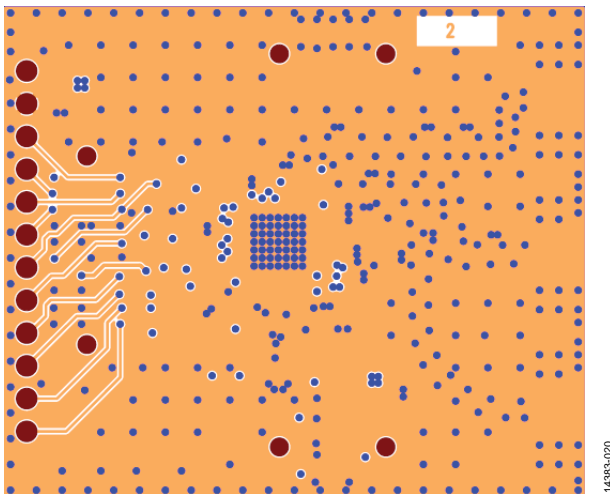


Figure 14. Layer 2, Ground Plane

A power plane is recommend on Layer 3 (see Figure 15). The power plane is sandwiched between the ground planes on Layer 2 and Layer 4 to minimize unwanted radiation. Provide low impedance paths from a battery or power supply connection to the six power pins of the ADF7030-1. Alternatively, use a power island or star connections to supply the power pins of the ADF7030-1.

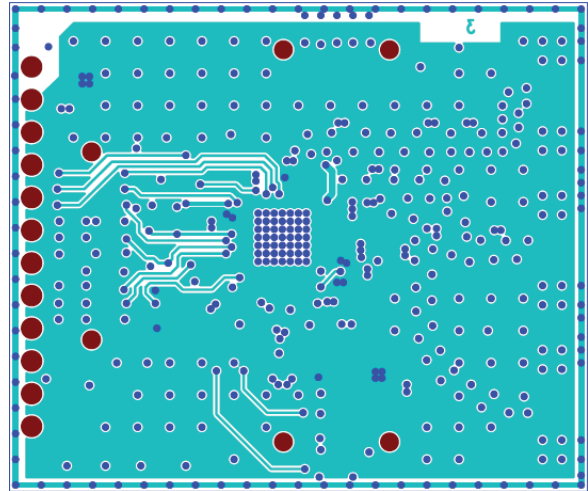


Figure 15. Layer 3, Power and Buried Signals

A ground plane is also recommend on Layer 4 (see Figure 16). On the reference design, there are some tracks to enable an EEPROM on the bottom of the board for identification of the daughter card.

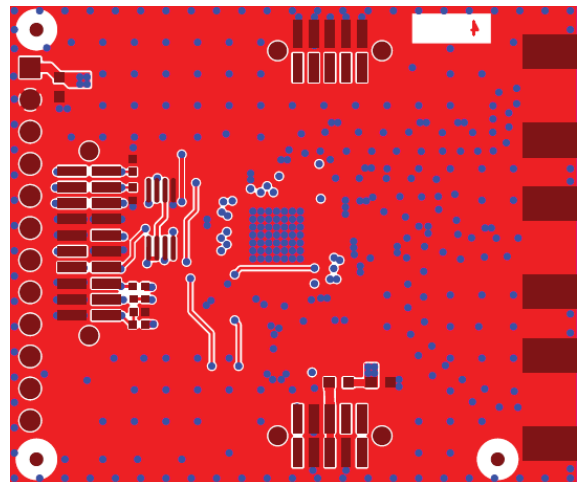


Figure 16. Layer 4, Ground Plane

## TEST MODE CONNECTIONS

The [ADF7030-1](#) has several test modes that can simplify the evaluation and debugging of applications.

### TRANSMIT TEST MODE CONNECTIONS

The [ADF7030-1](#) provides transmitter test modes that can transmit a carrier signal, preamble, or random data. These are useful for determining the output power level, harmonics, or modulation bandwidth. Configuration of these test modes are described in the [ADF7030-1](#) software reference manual.

### RELATED LINKS

| Resource  | Description  |
|---|--|
| <a href="#">ADF7030-1</a> data sheet                | Data sheet, <i>High Performance, Sub GHz Radio Transceiver IC</i>  |
| <a href="#">ADF7030-1</a> software reference manual | Software reference manual  |
| <a href="#">ADF7030-1</a> design package            | Contains all the <a href="#">ADF7030-1</a> documentation, firmware modules, configuration files, header files, and reference design information. |

### RECEIVE TEST MODE CONNECTIONS

For the purpose of receiver bit error rate measurement, the [ADF7030-1](#) provides a test mode to map the receive data and the receive clock to two GPIOx pins. Configuration of this mapping is described in the [ADF7030-1](#).



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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